Controller IC Evaluation of High Radix Parity Check Code

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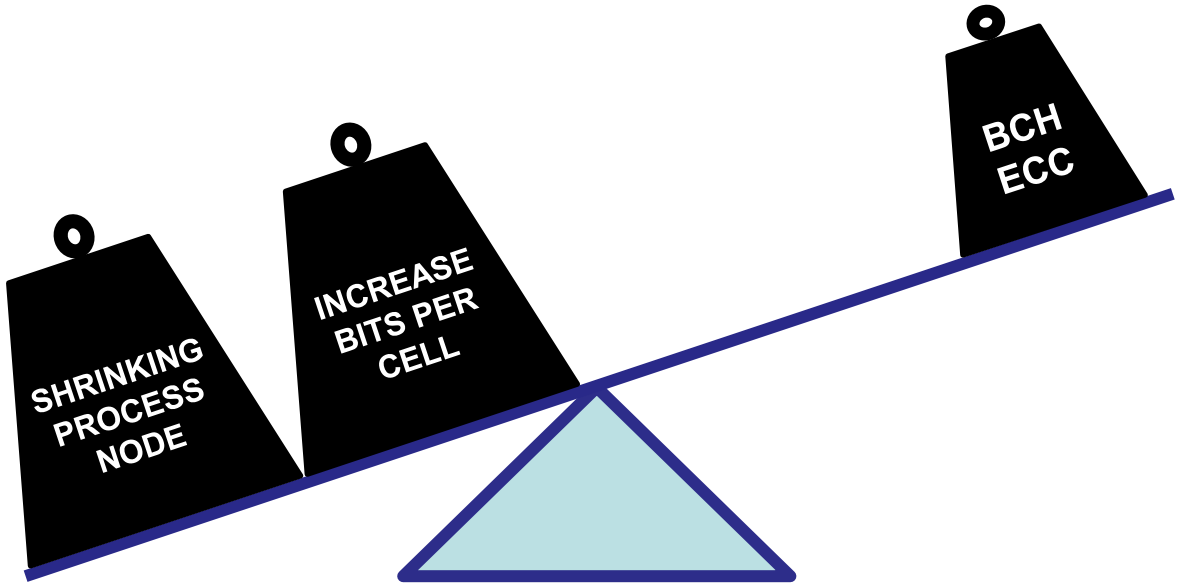
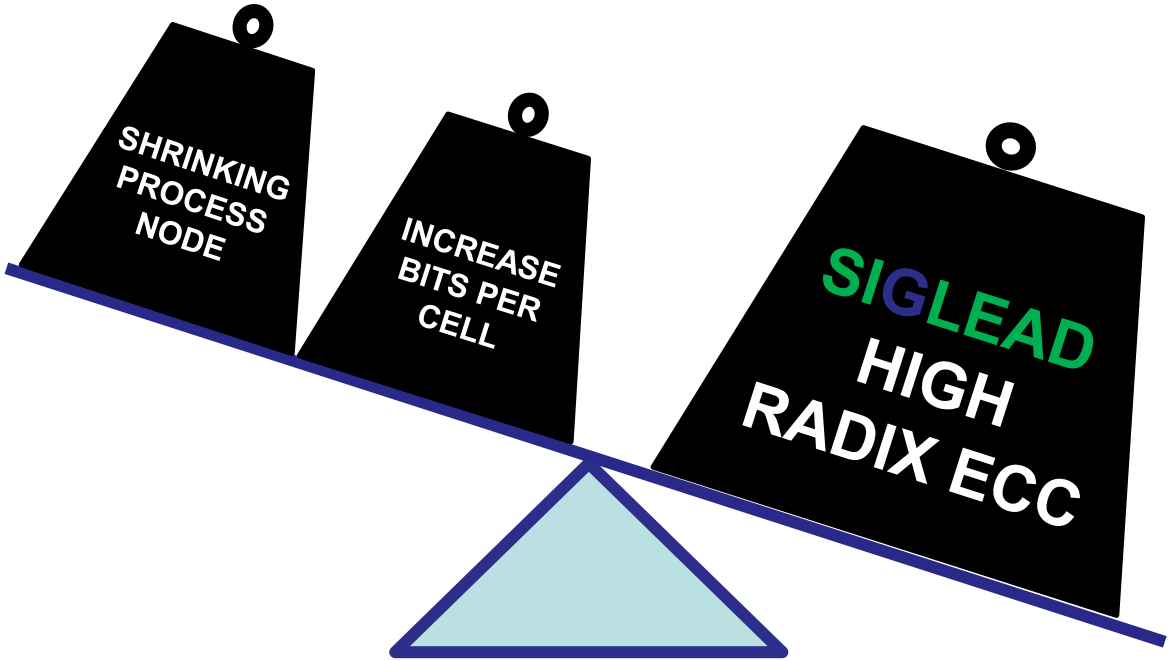
NAND vs Error Correction (1)



NAND raw bit error rate increases.

Conventional BCH ECC cannot protect data.

NAND vs Error Correction (2)



A stronger ECC will protect the data.

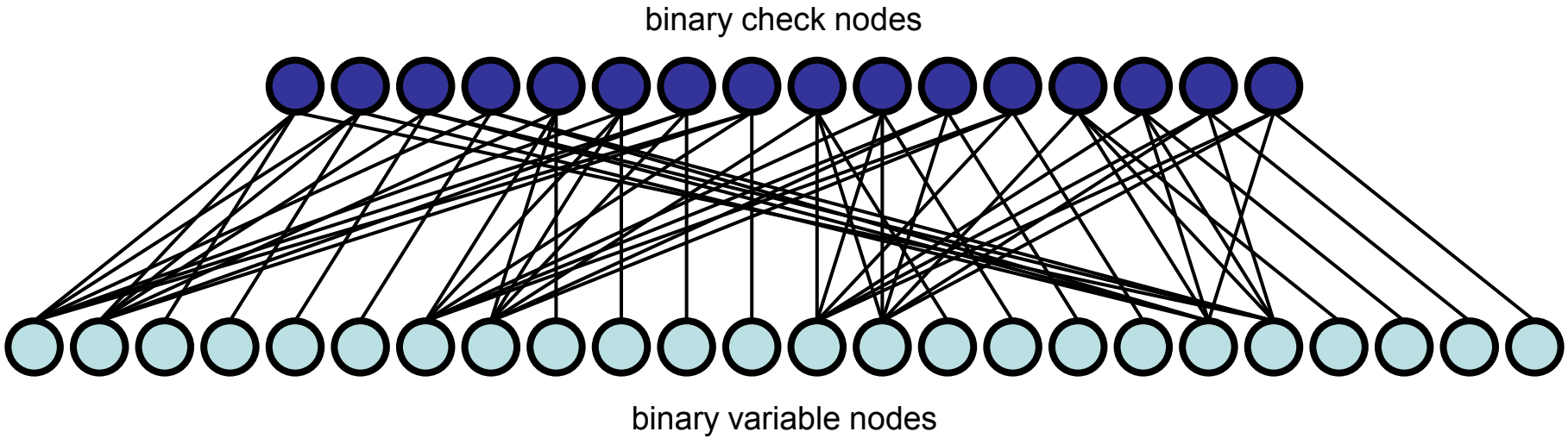
The balance is tipped in our favor!

Siglead's High Radix ECC

- High Radix ECC is in our SATAIII Controller IC
- Significantly stronger than BCH ECC
  - typically delivering at least 2x improvement in SSD endurance even on sub 20nm TLC nodes
- No significant compromise in power consumption and throughput

High Radix ECC Example (1)

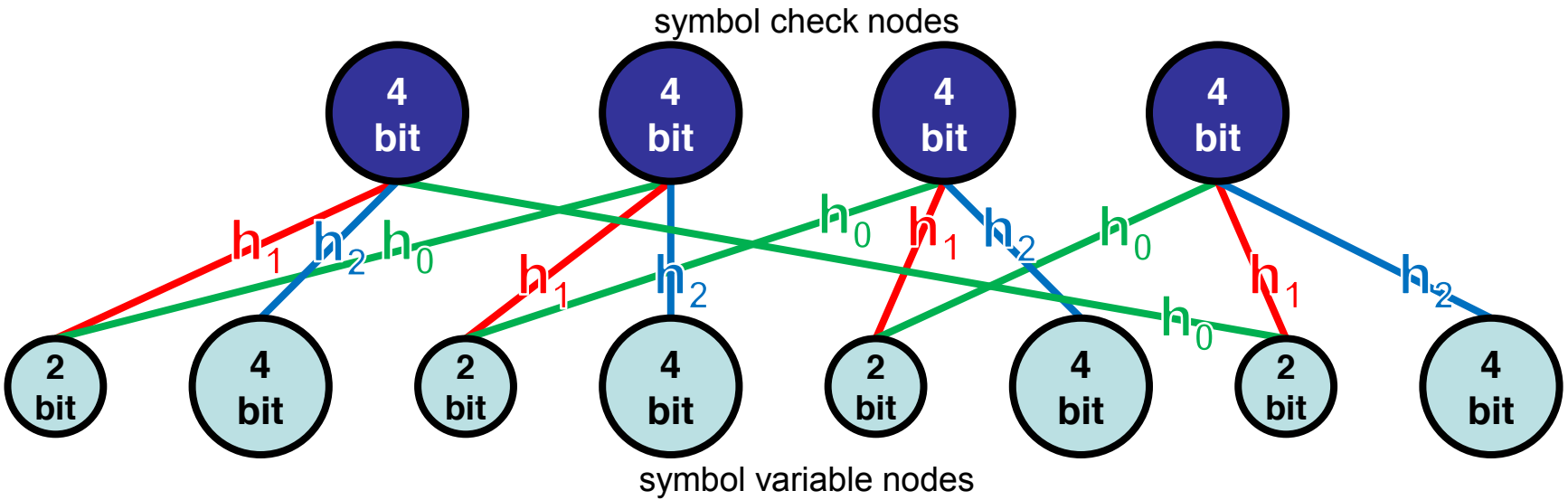
- Merge binary variable/check nodes of a binary ECC



High Radix ECC Example (2)

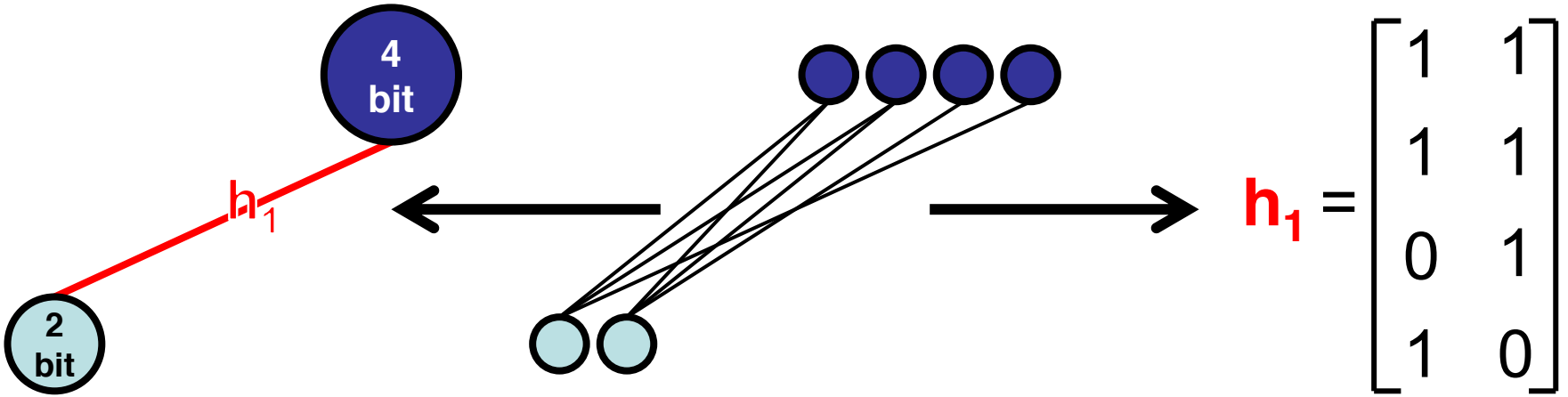
- Merge binary variable/check nodes of a binary ECC…

…to get variable/check node SYMBOLS + **EDGE LABELS**



High Radix ECC Example (3)

- Edge label is matrix representation of merged edges of binary ECC



High Radix ECC Example (4)

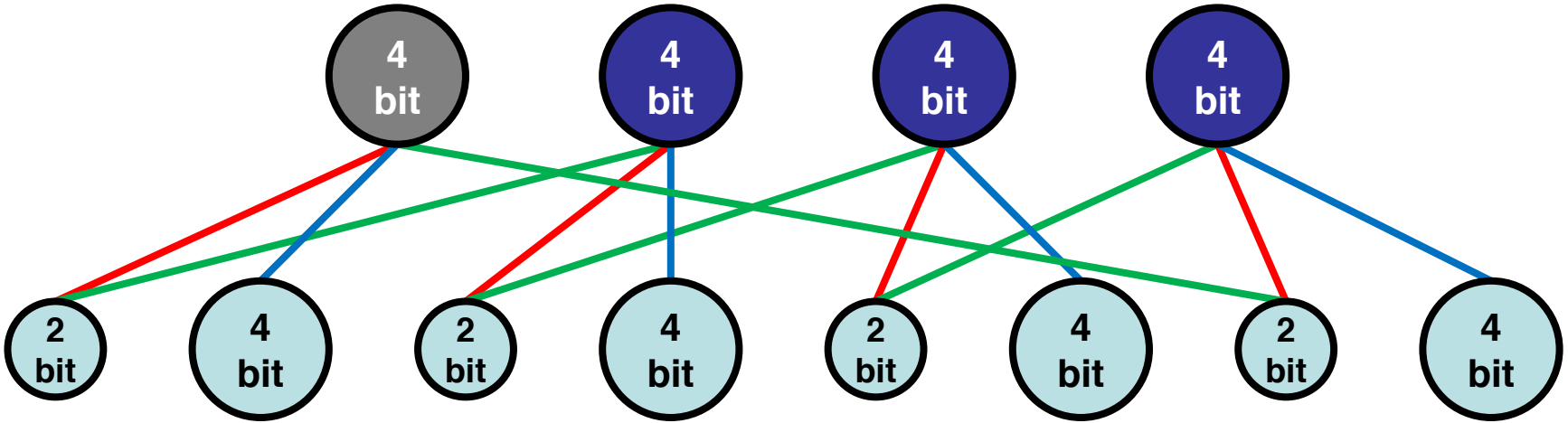
- High Radix ECC parity check matrix is a matrix of sub-matrices

$$H = \begin{bmatrix} h_1 & h_2 & 0 & 0 & 0 & 0 & h_0 & 0 \\ h_0 & 0 & h_1 & h_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & h_0 & 0 & h_1 & h_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & h_0 & 0 & h_1 & h_2 \end{bmatrix}$$

where $h_0 = \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 1 & 1 \\ 1 & 1 \end{bmatrix}$, $h_1 = \begin{bmatrix} 1 & 1 \\ 1 & 1 \\ 0 & 1 \\ 1 & 0 \end{bmatrix}$ and $h_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$

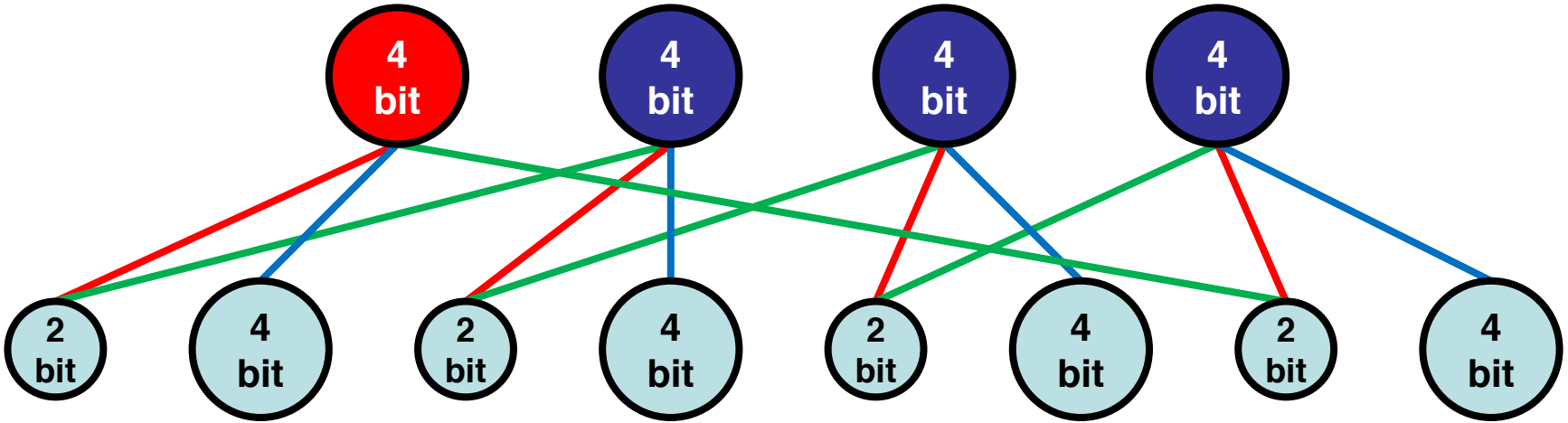
Decoding High Radix ECC (1)

- Start with 1st check node (highlighted grey)



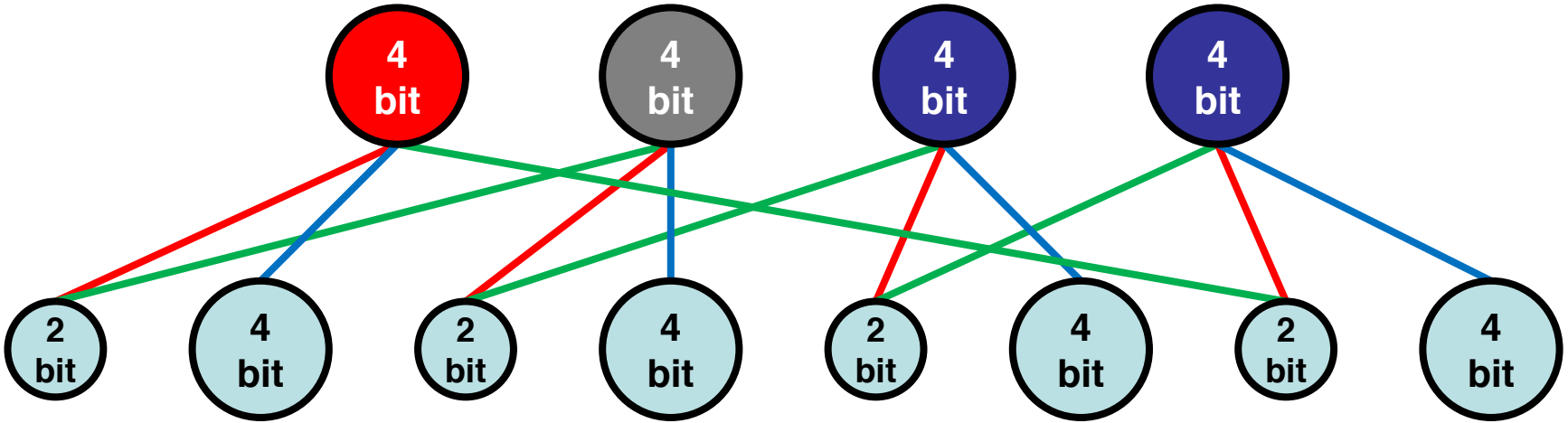
Decoding High Radix ECC (2)

- 1st check node ECC uncorrectable (highlight red)



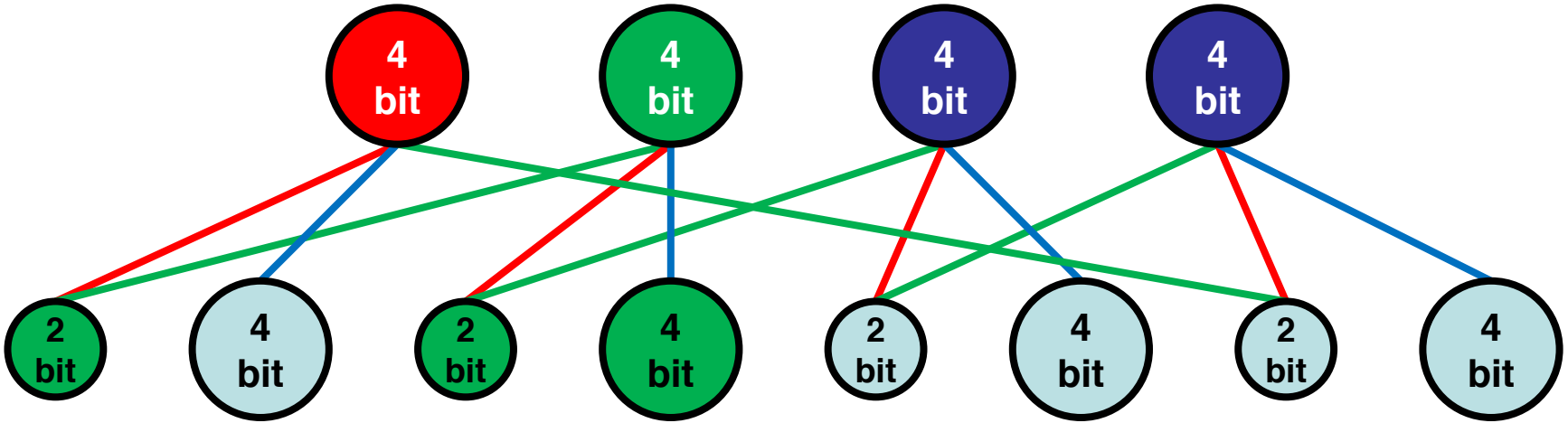
Decoding High Radix ECC (3)

- Move to 2nd check node (highlighted grey)



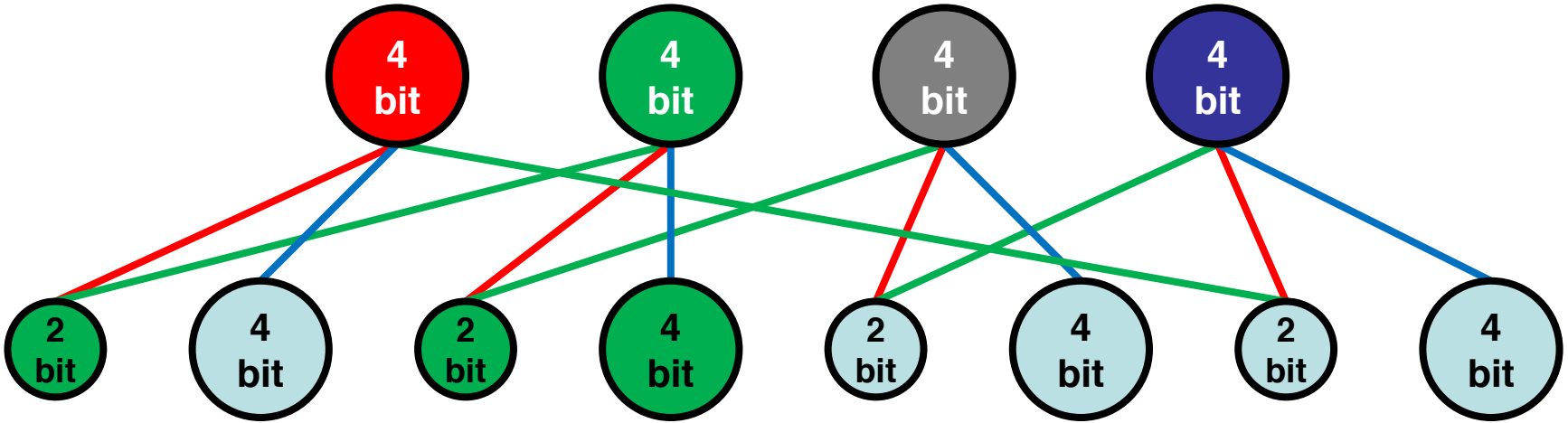
Decoding High Radix ECC (4)

- 2nd check node ECC correctable (highlight green)
- Attached variable nodes are corrected (highlighted green)



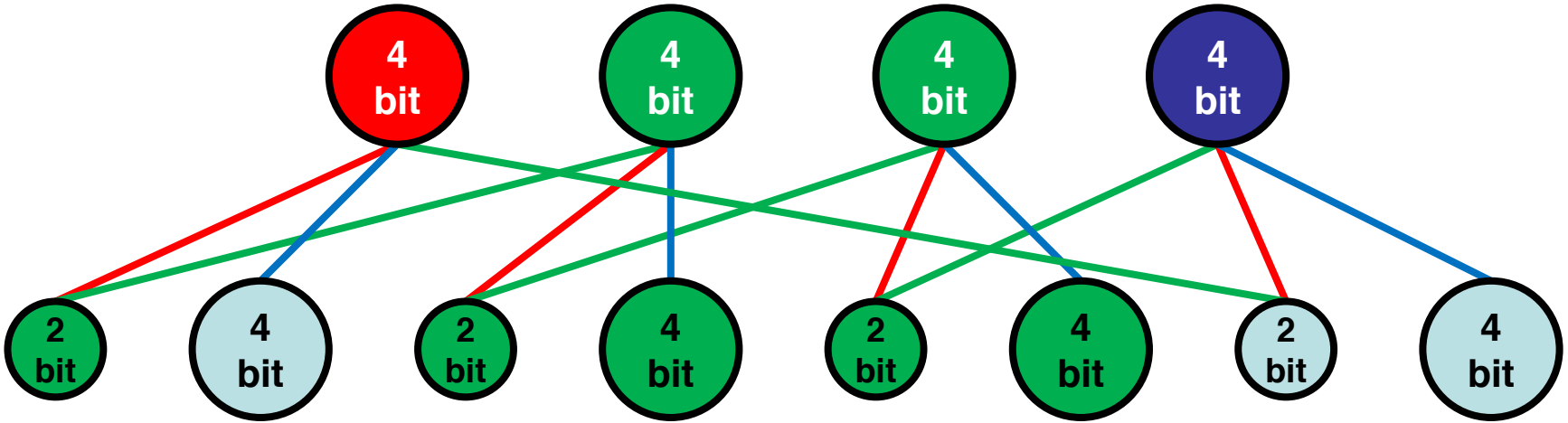
Decoding High Radix ECC (5)

- Move to 3rd check node (highlighted grey)



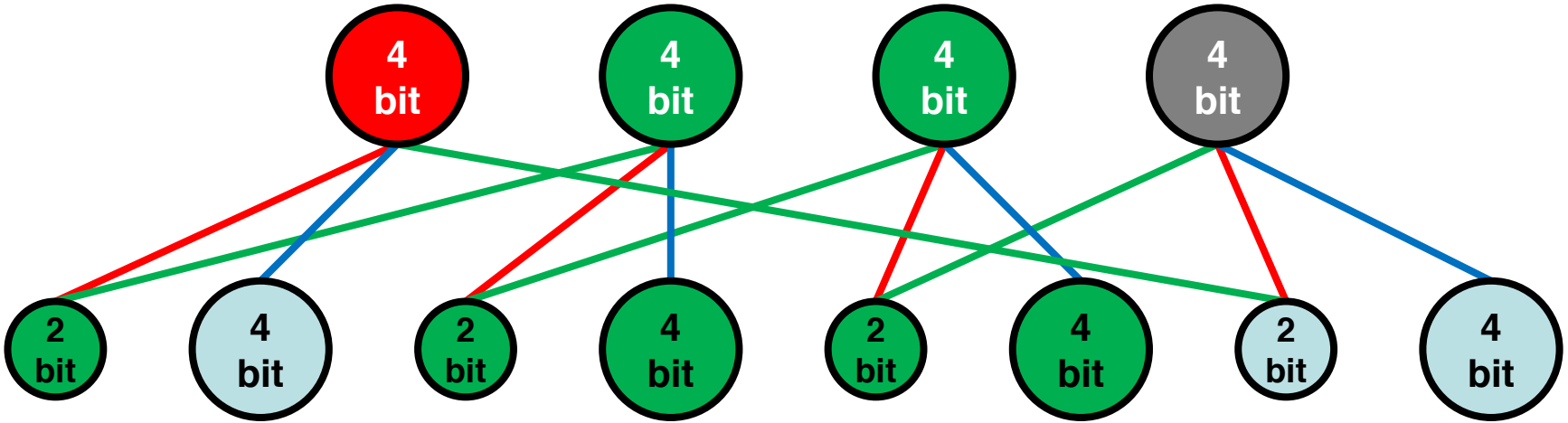
Decoding High Radix ECC (6)

- 3rd check node ECC correctable (highlight green)
- Attached variable nodes are corrected (highlighted green)



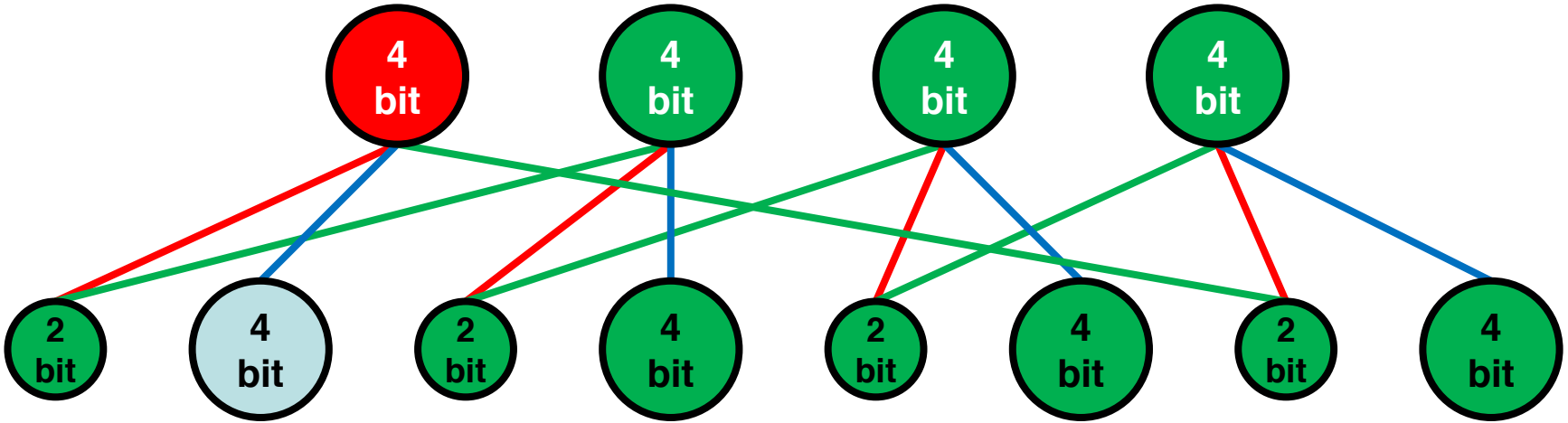
Decoding High Radix ECC (7)

- Move to 4th check node (highlighted grey)



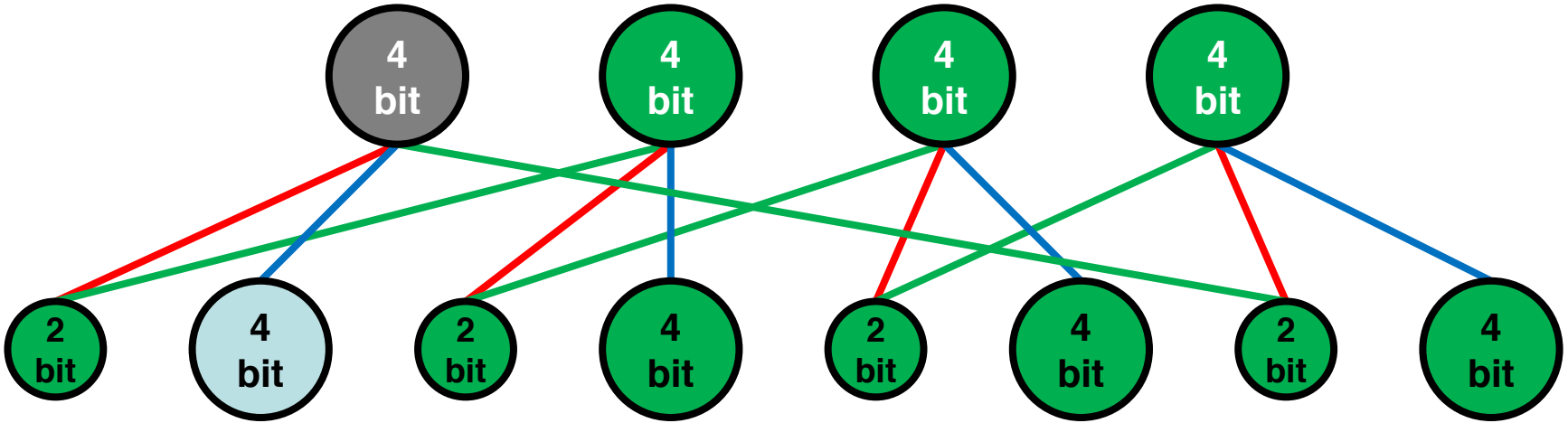
Decoding High Radix ECC (8)

- 4th check node ECC correctable (highlight green)
- Attached variable nodes are corrected (highlighted green)



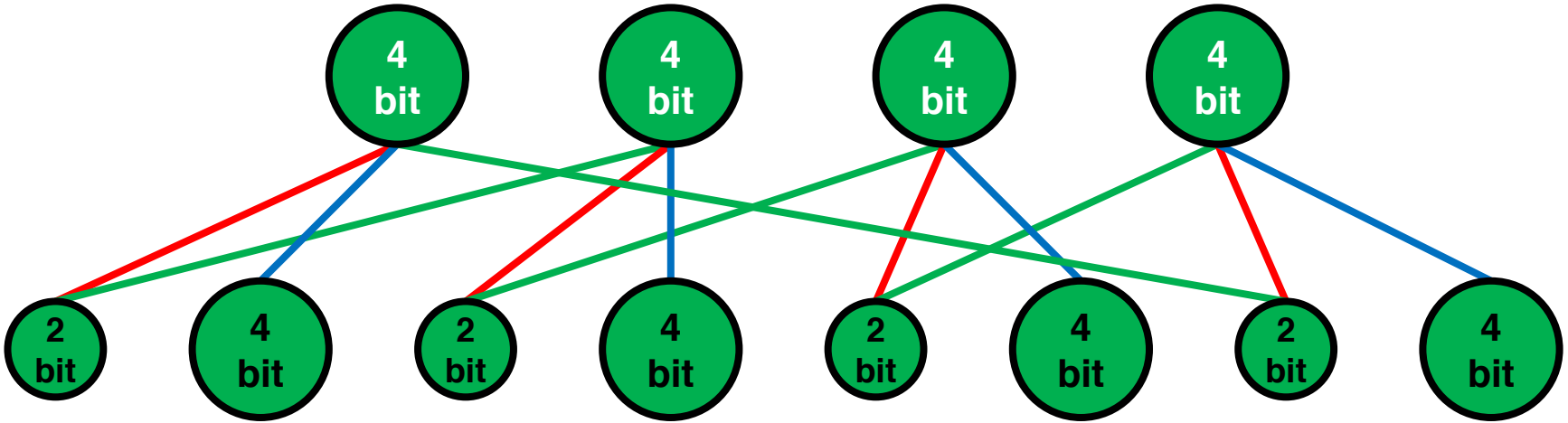
Decoding High Radix ECC (9)

- Return to 1st check node (highlighted grey)



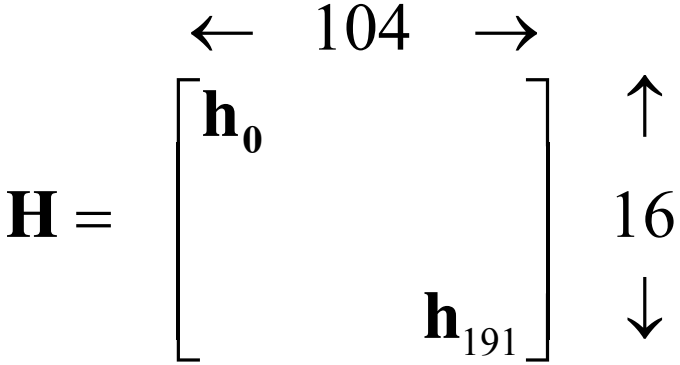
Decoding High Radix ECC (10)

- 1st check node ECC is now correctable (highlight green)
- Attached variable nodes are corrected (highlighted green)



High Radix ECC in SSD Controller IC

Outline of High Radix ECC parity check matrix in SL2007D

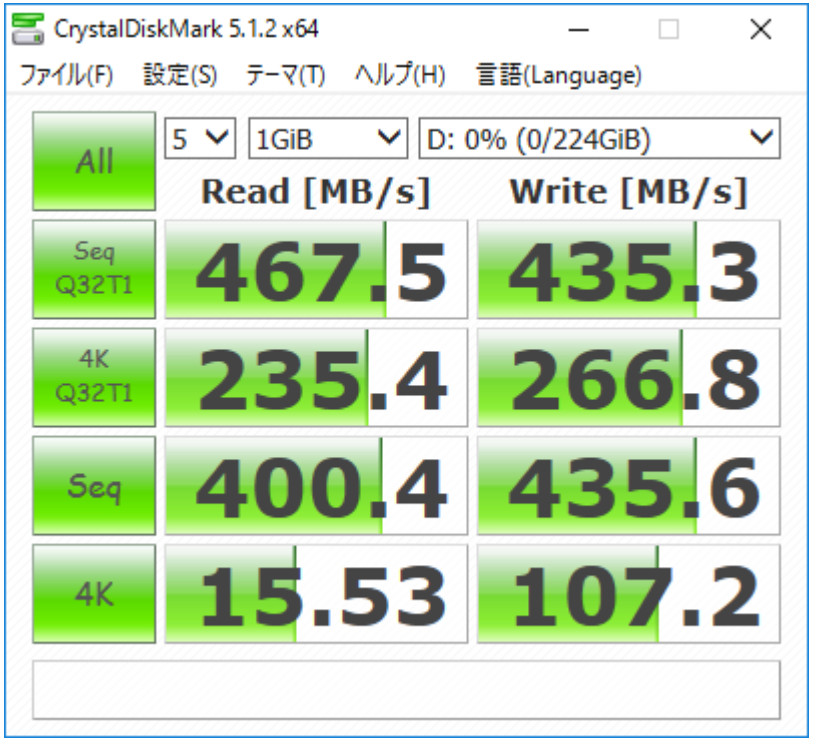


edge matrix:16x104 containing 192 non-zero sub matrices

- **Highly programmable**
  - variety of code rates are possible to suit different NAND processes/vendors/bits per cell
  - many different configurations of High Radix ECC parity check matrix are possible
- **Typical Example for 16kB NAND page:**
  - 16 High Radix check nodes
  - encodes a least 1kB of user data per check node

Controller IC Throughput Performance

- Throughput performance of Siglead's controller IC with High Radix ECC enabled
- **INTERFACE:** SATAIII
- No significant drop down in performance when using High Radix ECC



Controller ECC Performance on Sub 20nm TLC NAND

- Controller IC evaluation of High Radix ECC
- **NAND:** sub 20nm TLC
- **ENDURANCE:** 300P/E cycles using "LDPC achieving RBER=10^{-2}"
- High Radix ECC achieves endurance of up to 600P/E cycles

SIGLEAD'S High Radix ECC achieved 2x ENDURANCE on sub 20nm TLC node

SUB 20nm TLC NAND		
P/E CYCLES	BCH CODE ONLY	SIGLEAD HIGH RADIX ECC
150	FAIL	PASS
300	FAIL	PASS
450	FAIL	PASS
600	FAIL	PASS
750	FAIL	FAIL

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Live demo of SL2007D – our SSD controller IC

Live Demo of our NAND analyzer platforms
SigNASII and SigNAS3

BOOTH 900