# Advanced Controller Technology for 3D NAND Flash

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# Outline

- The Reliability Issues of 3D NAND Flash
- The Architecture of Error Handling Technology
- Error Correction Technology
- Comparison between ECC engines
- Reliability of SSD with 3D NAND Flash memory
- Conclusion

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# The Reliability Issues of 3D NAND

- Fast de-trapping of programmed electron
- Layer Dependency
- Different erase mechanism from 2D NAND
- Different retention behavior from 2D NAND
- Weak read disturb immunity
- Weak program disturb immunity

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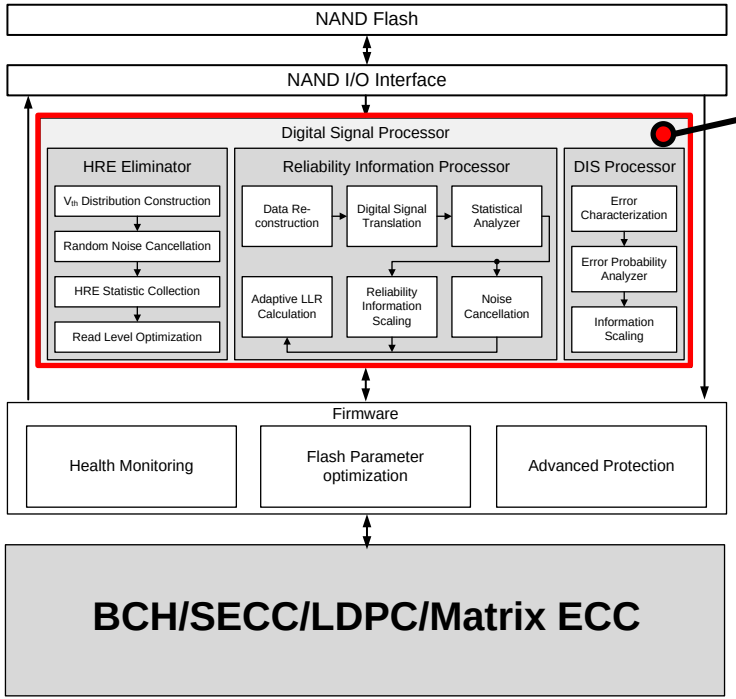
# Error Handling Tech. in Controller




- **Digital Signal Processors:**
  - **Reduce Error.**
  - **Collect/transfer the channel info.**

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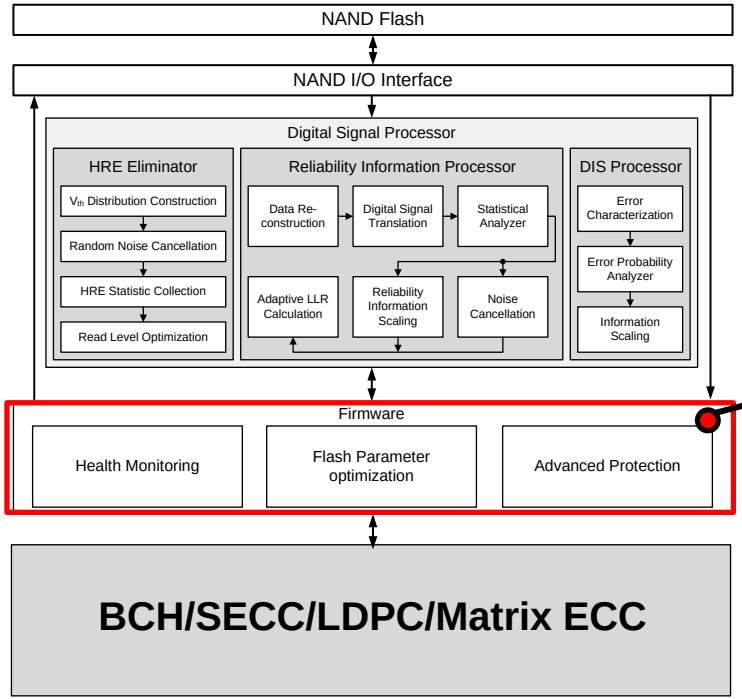


- **Firmware:**
  - **Judge the info. form DSP/ECC.**
  - **Adaptively control ECC engine.**
  - **Adaptively control NAND Flash.**
  - **Adaptively change the data Structure.**

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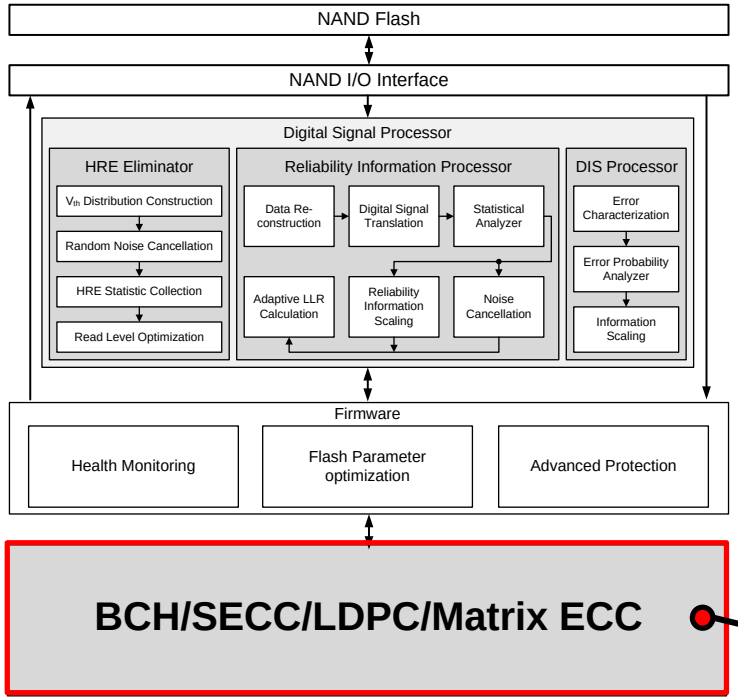


- **ECC Engine:**
  - **Low Power.**
  - **Low Cost.**
  - **Excellent Correction Strength.**

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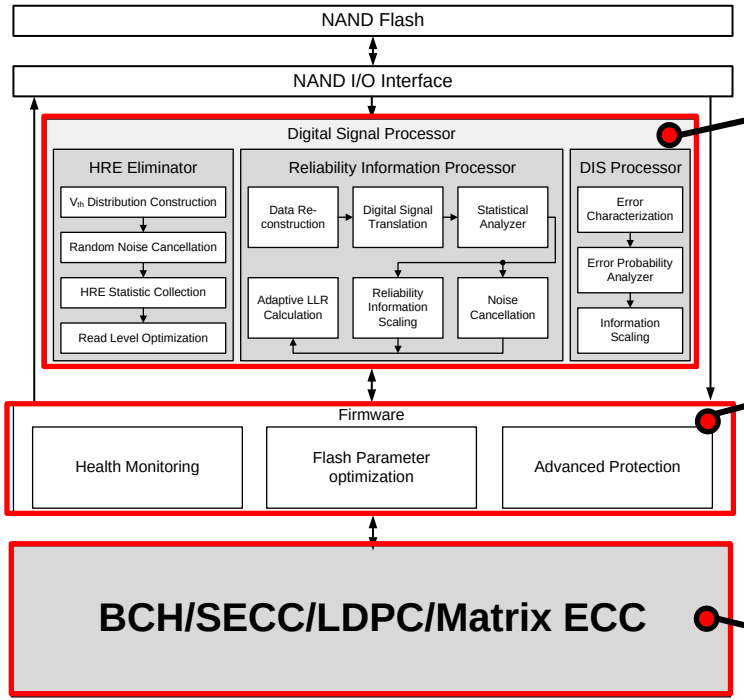


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**Power consumption**

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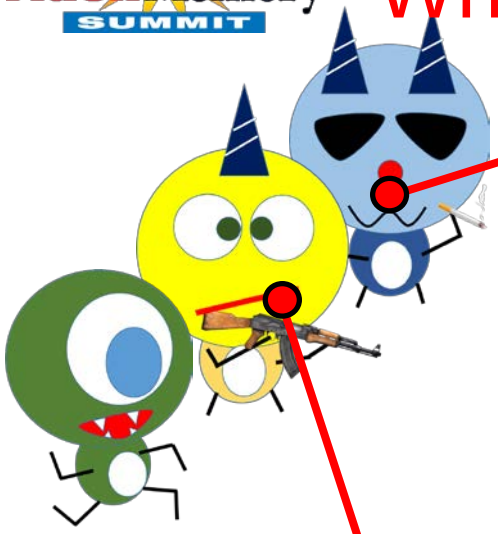

Power consumption

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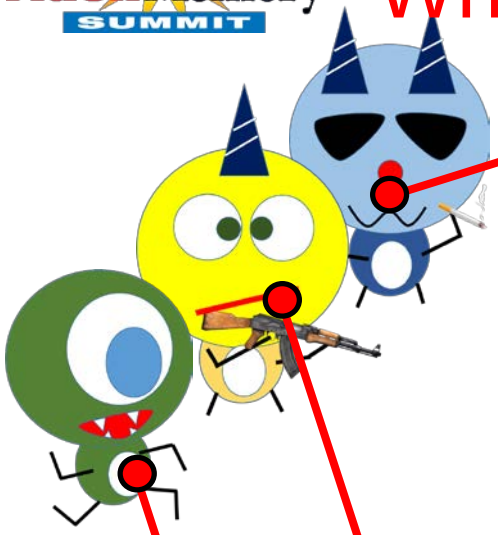

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HRE

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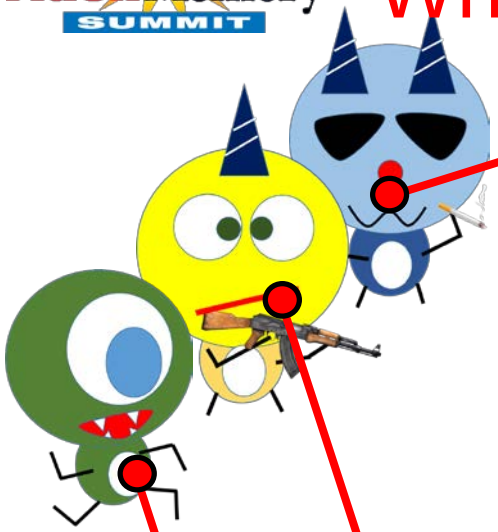

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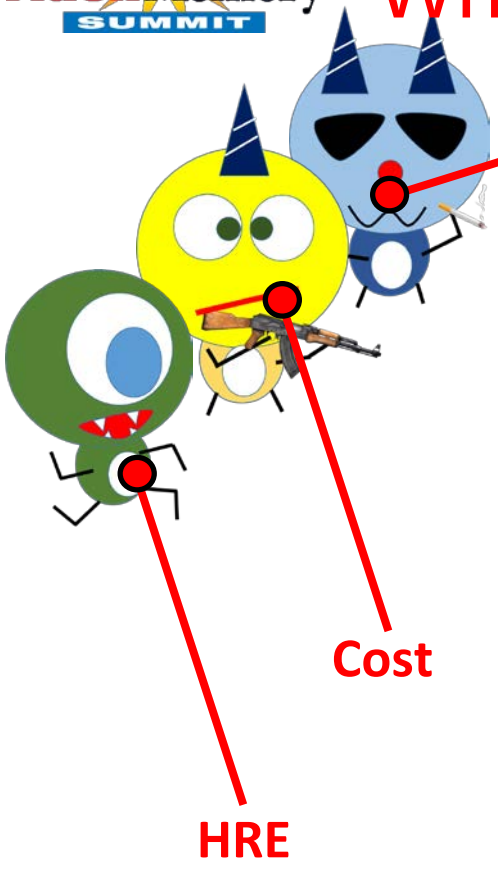
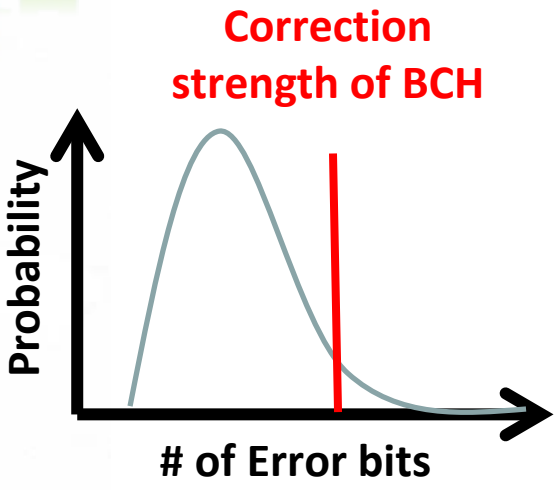
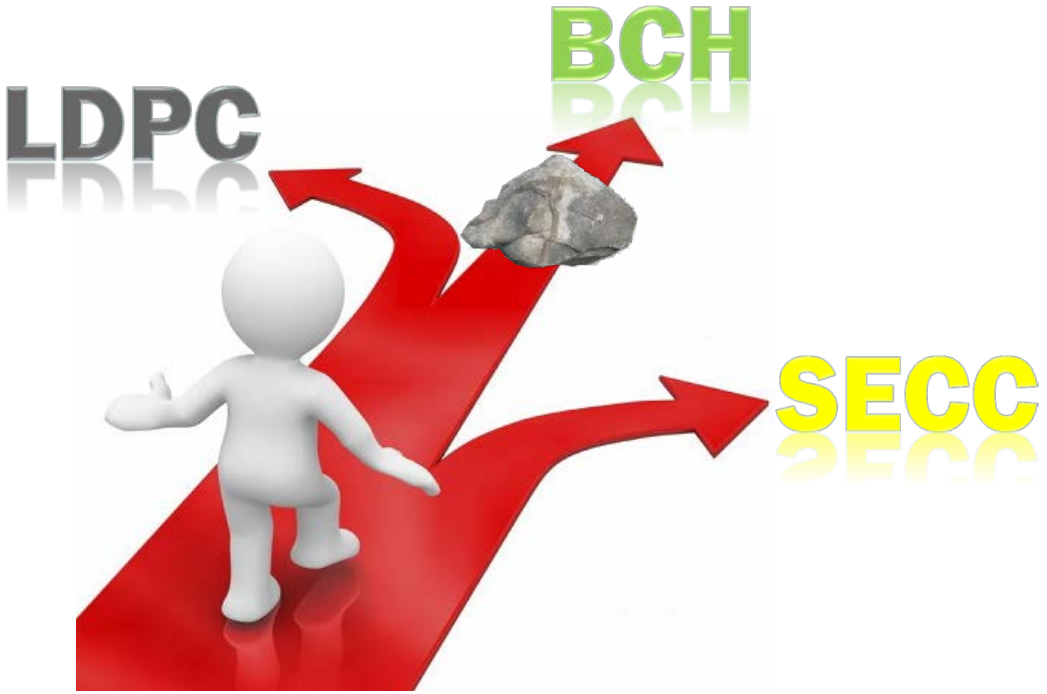






# Phison Provides a NEW WAY for ECC



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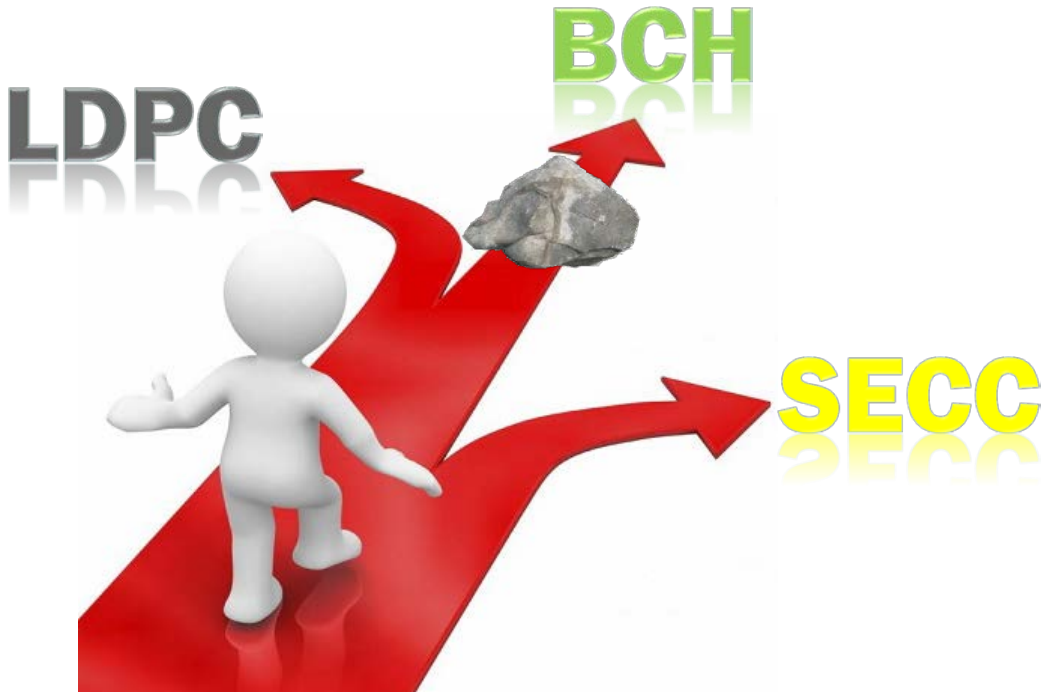
# Novel Design of LDPC Technology

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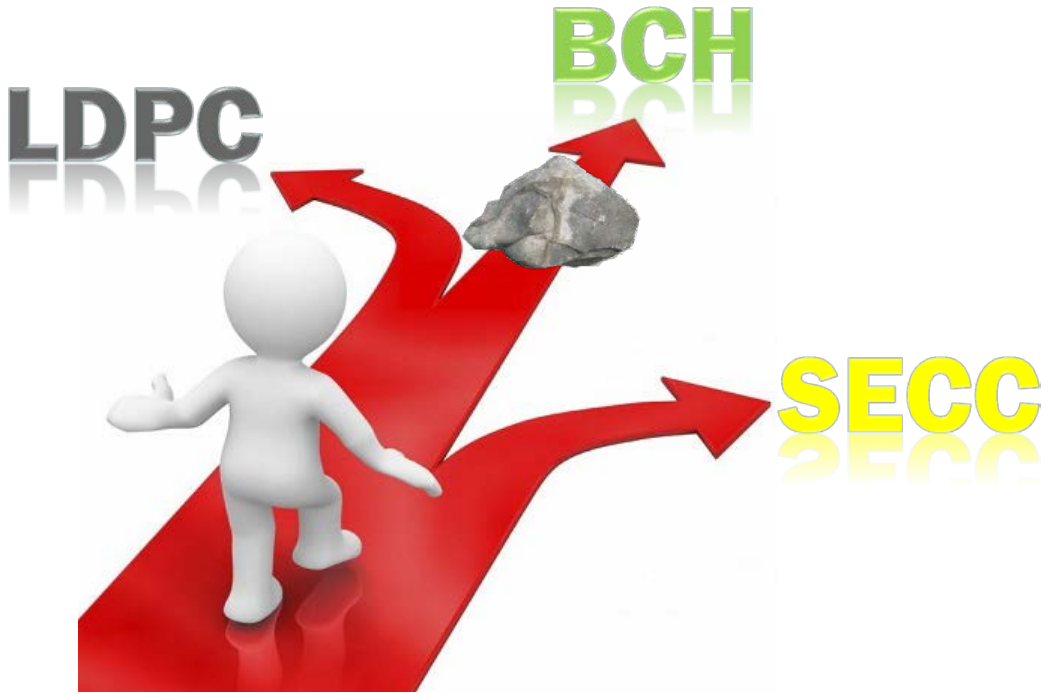

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# Comparison between ECC tech

| | Conventional LDPC | BCH |
|---|---|---|
| Decoding Algorithm | Probability Based | Algebraic Based |
| Guaranteed Correction Strength | No | Yes |
| Soft Bit Decoding | Easy | Hard |
| Performance of Hard Decoding | Similar to BCH | $\frac{\text{Code Length} * (1-\text{code rate})}{\text{Degree of polynomial}}$ |
| Performance of Soft Decoding | 2X than BCH | - |
| Decoding Complexity | High | Low |
| Power consumption | High | Mid |
| Cost | High | Low |

# Comparison between ECC of Phison

| | 4K LDPC | 4K LDPC Lite | SECC | BCH |
|---|---|---|---|---|
| Decoding Algorithm | Probability Based | Probability Based | Probability Based | Algebraic Based |
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| Performance of Soft Decoding | 2X-3X than HB | 2X than BCH | 1.7X than BCH | - |
| Decoding Complexity | Mid | Mid | Low | Low |
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# ECC Technology of Phison

| | Correction Strength | Gate Count | Technology node (nm) | Support NAND | Q3' 2016 | Q4' 2016 | 2017 |
|---|---|---|---|---|---|---|---|
| 1K BCH | 72/1K | 260K | 55/40/28 | 2D/3D MLC/TLC | Applied for USB/SD/eMMC/SSD | | |
| 2K BCH | 120/2K | 540K | 55 | 2D/3D MLC/TLC | Applied for SSD | | |
| SECC | 95&135/1K | 300K | 40 | 2D/3D MLC/TLC/QLC | Applied for SD/eMMC/UFS/SSD | | |
| 4K LDPC Lite | 72&150/1K | 0.7M | 40 | 2D/3D MLC/TLC/QLC | Applied for SSD | | |
| 4K LDPC | 85&200/1K | 1M | 28 | 2D/3D MLC/TLC/QLC | | Applied for SSD | |
| Matrix ECC | - | 300K | 55/40/28 | 2D/3D MLC/TLC/QLC | Applied for SSD/UFS | | |

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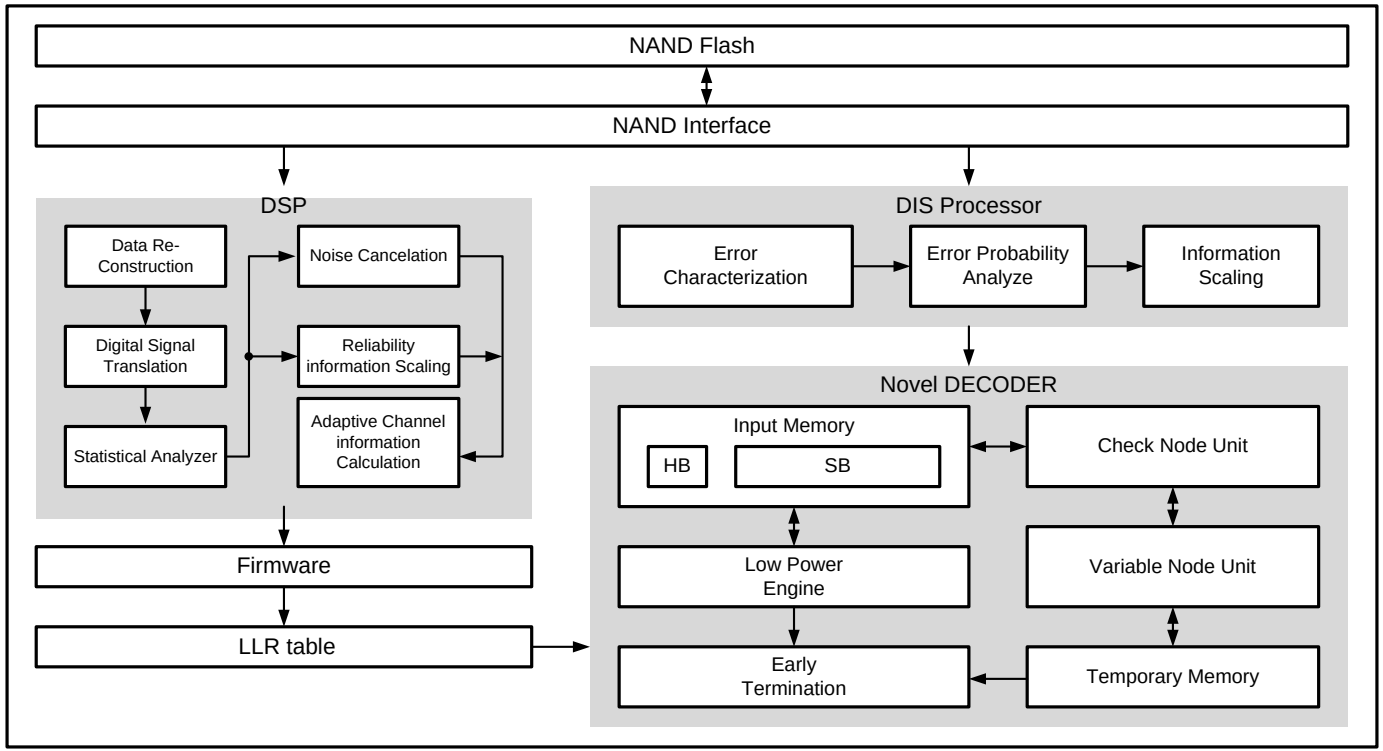
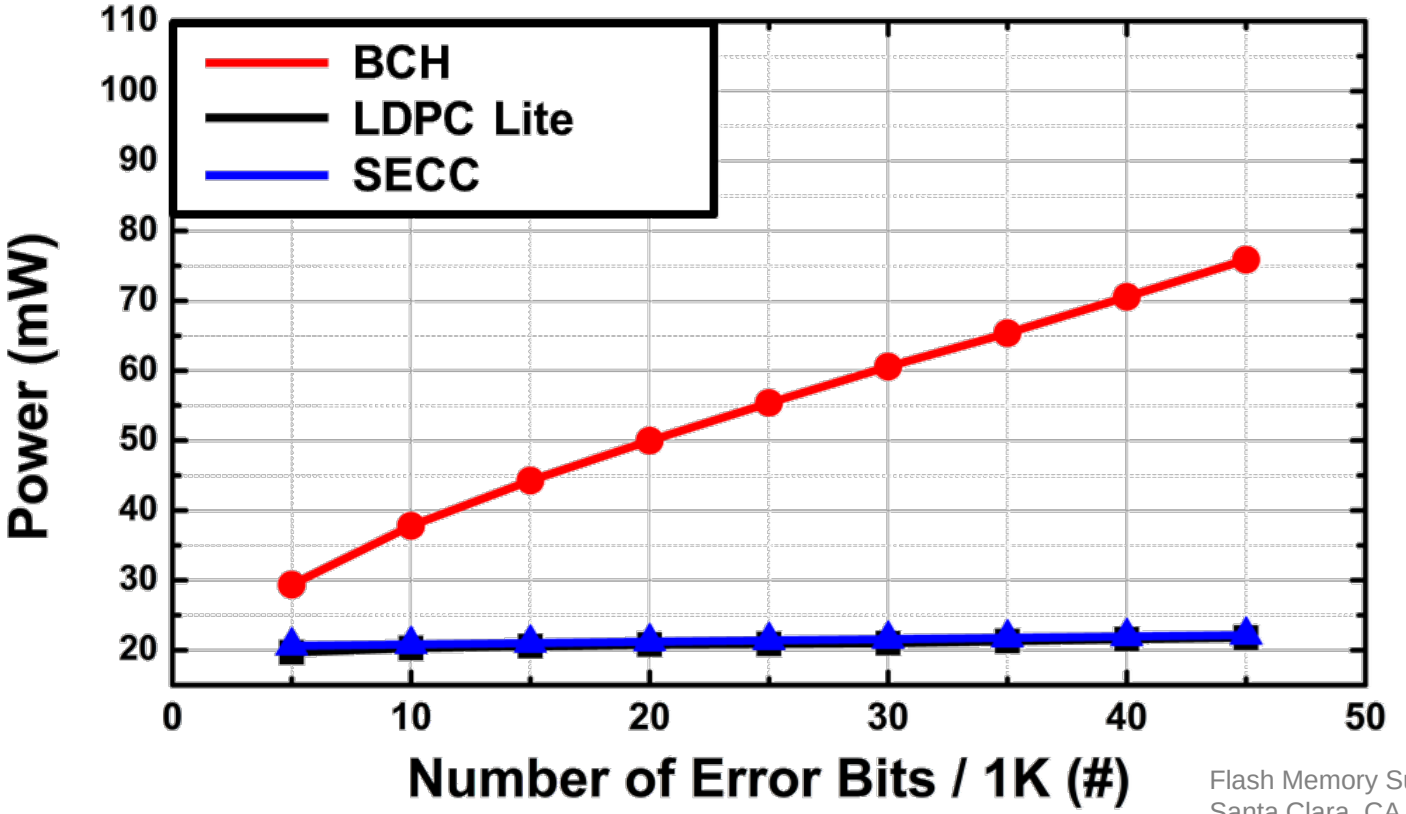
# Hardware Architecture of LDPC Lite



# Ultra Low Power Consumption



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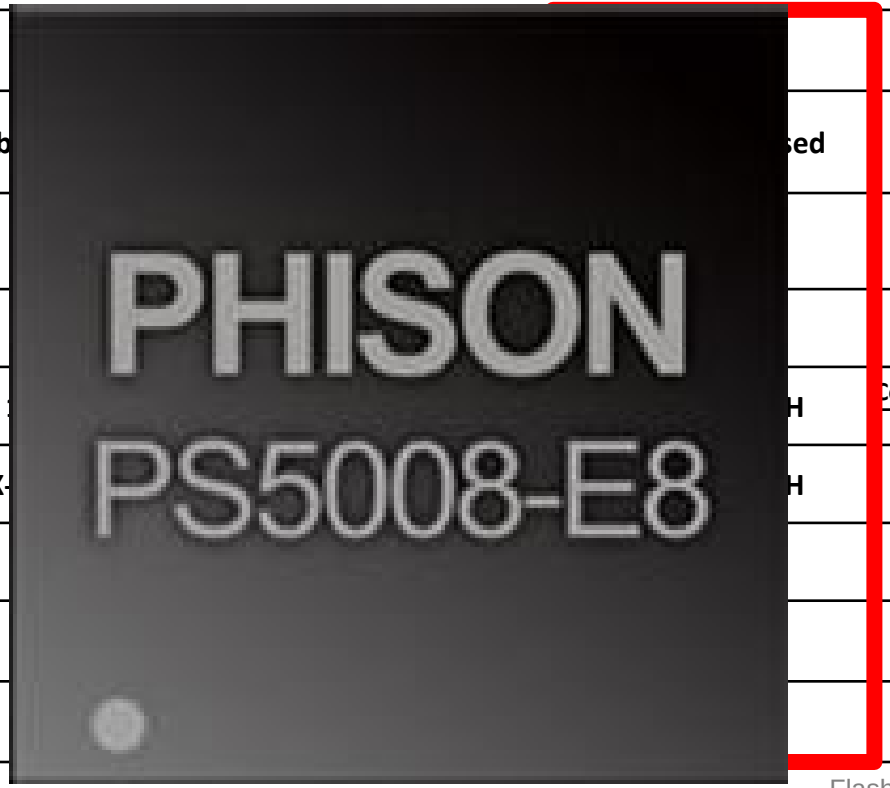

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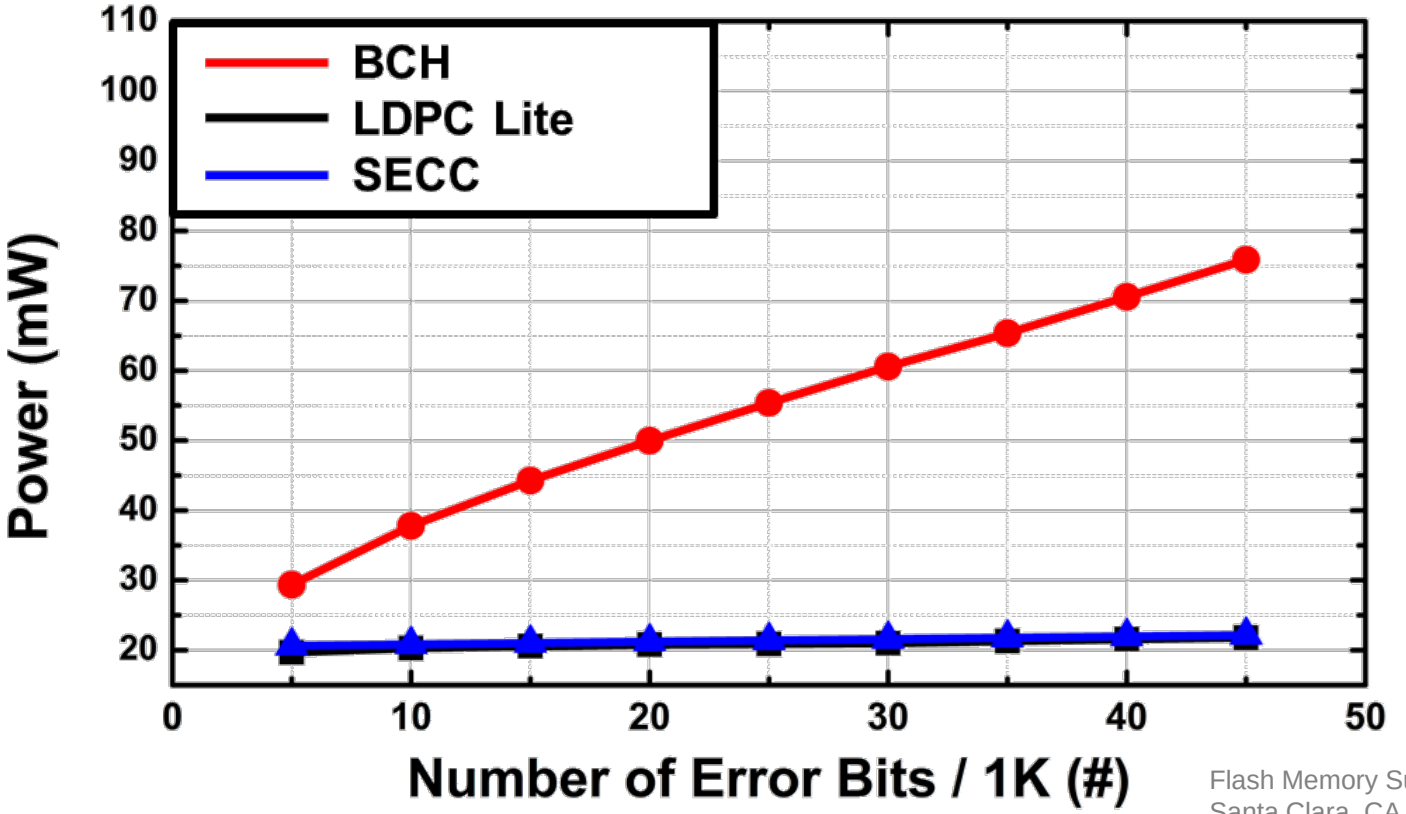
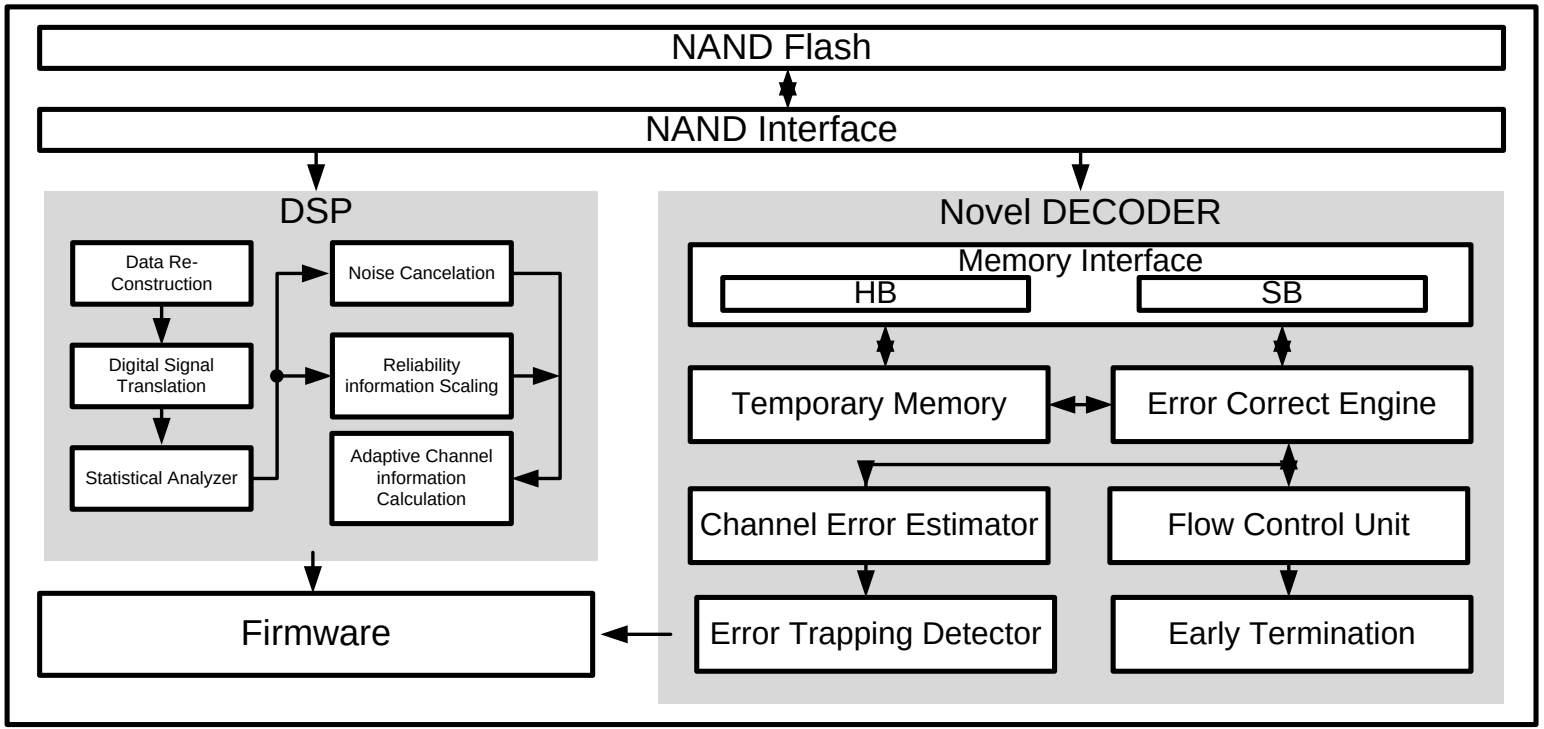
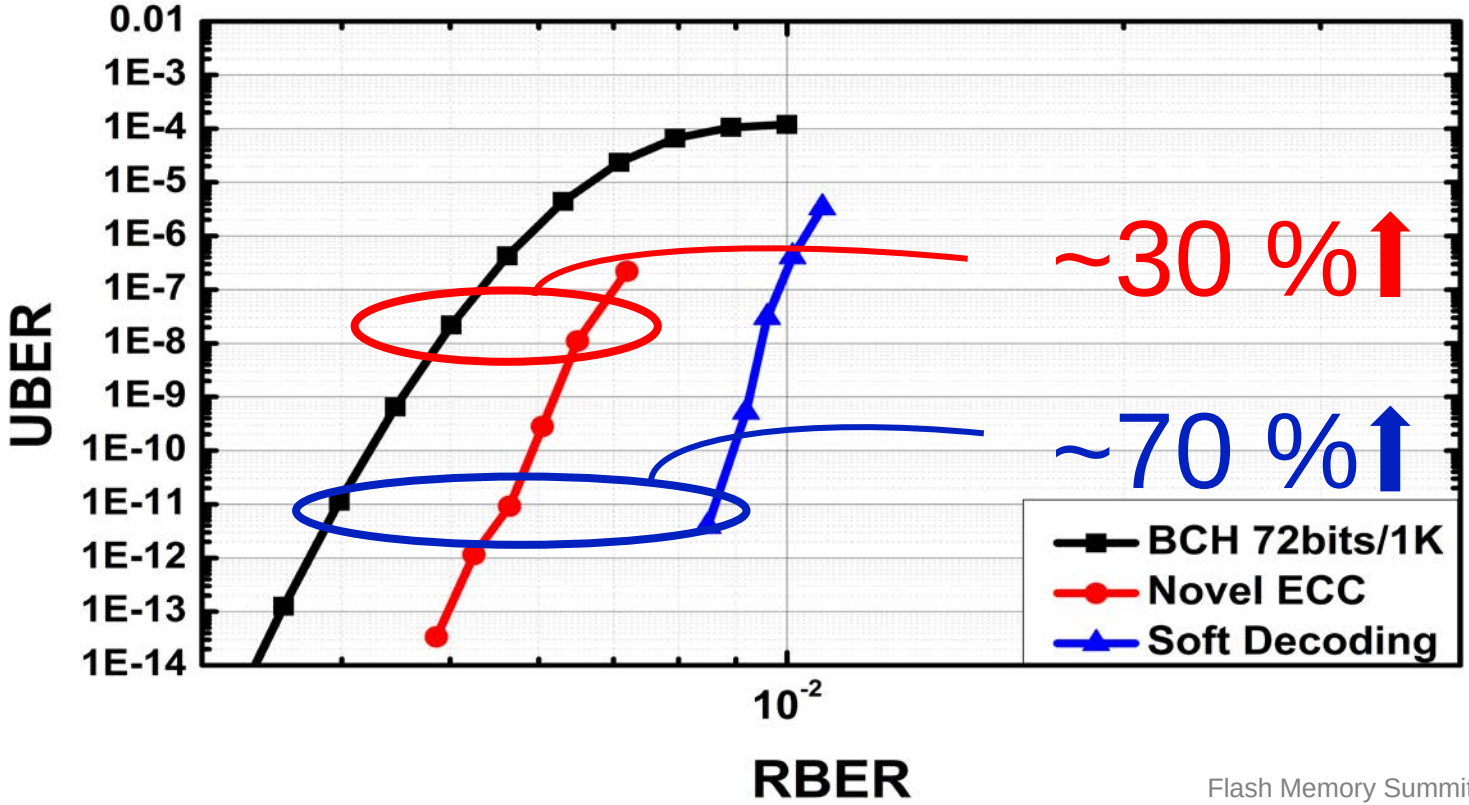


# Hardware Architecture of SECC



# Correction Capability of SECC



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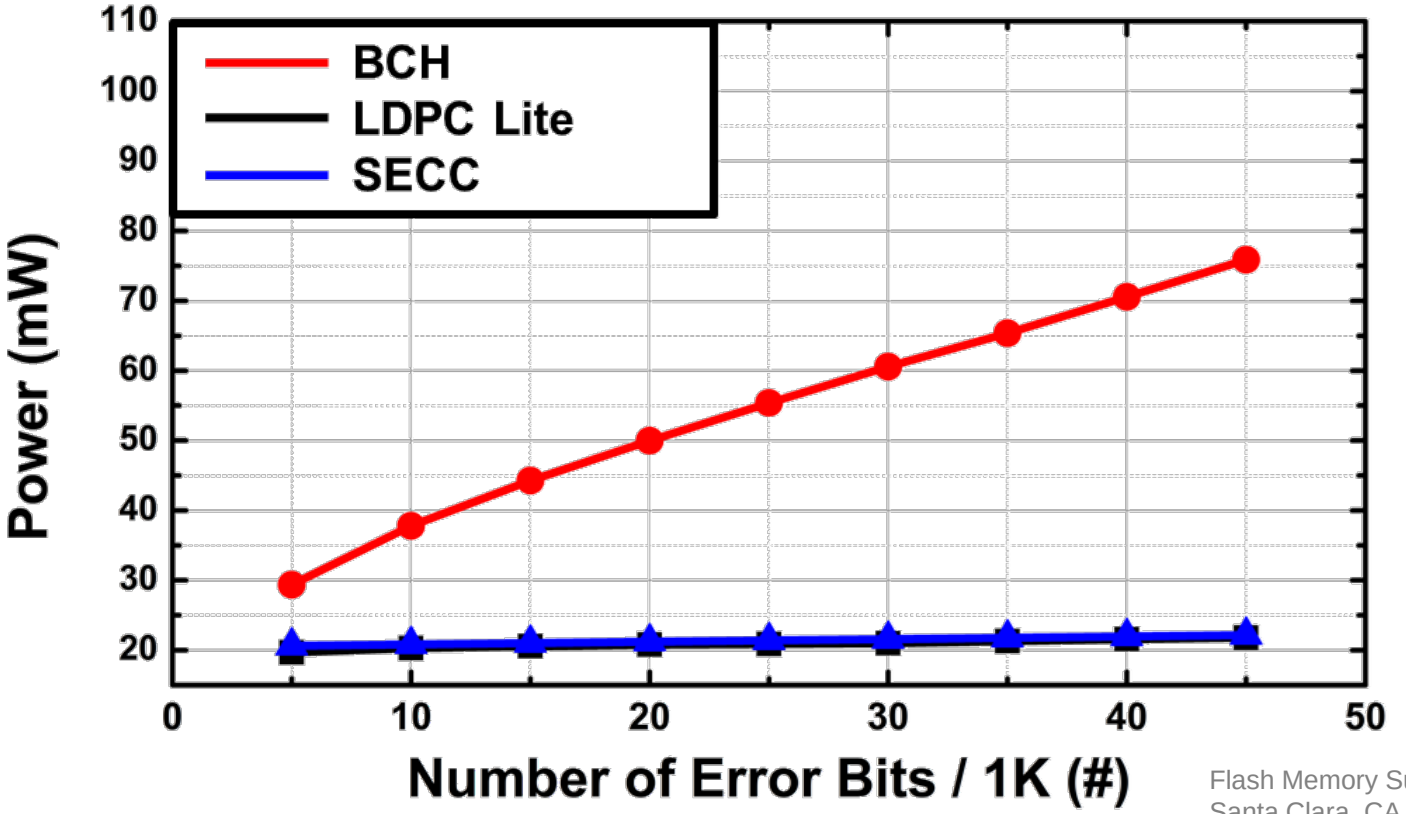

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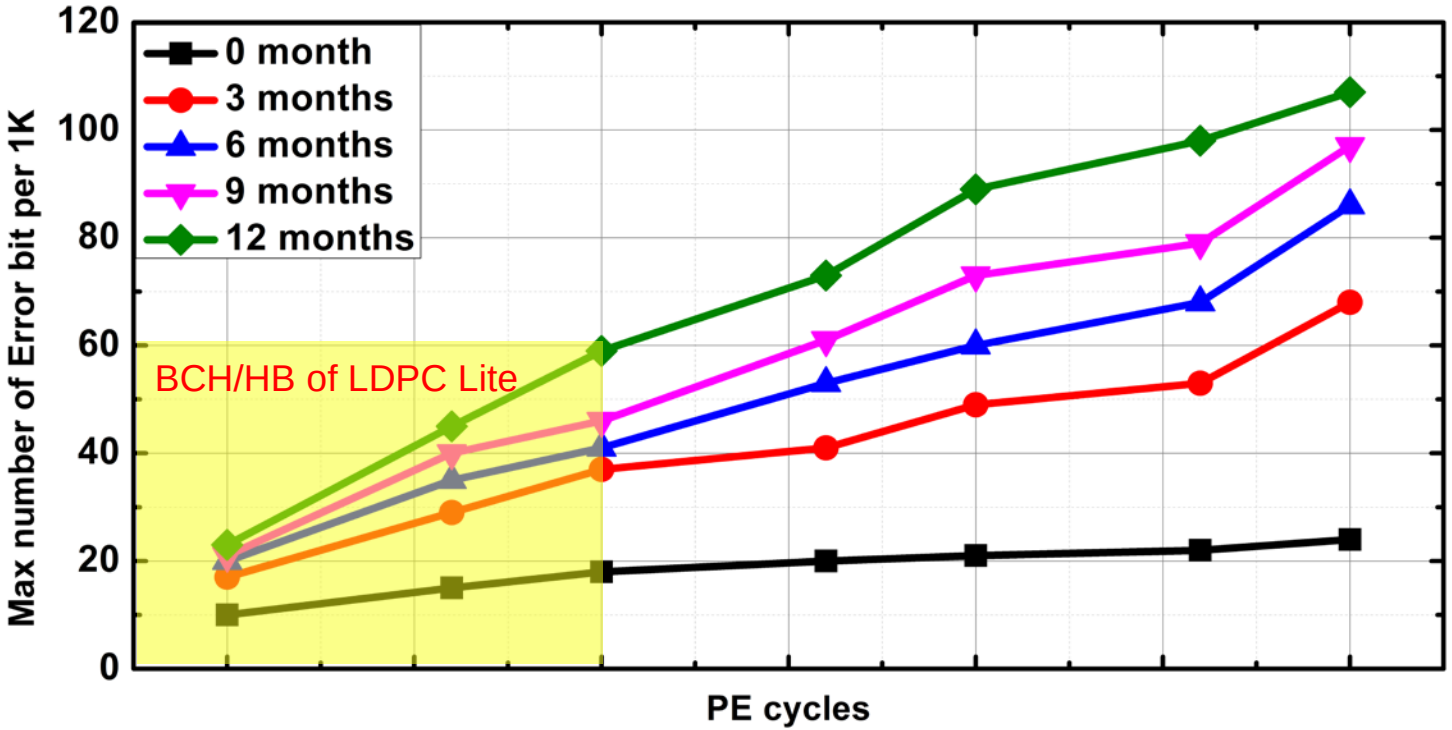

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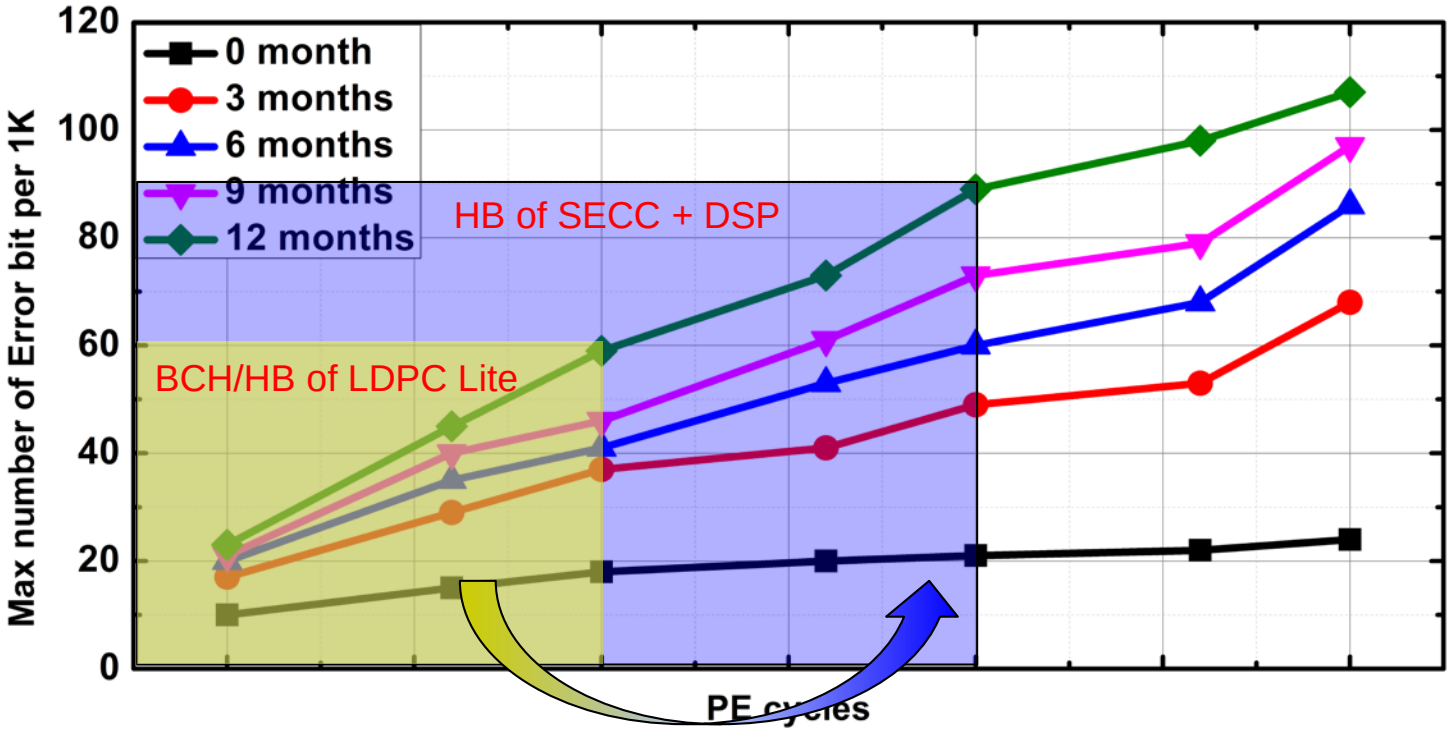


2X Extended

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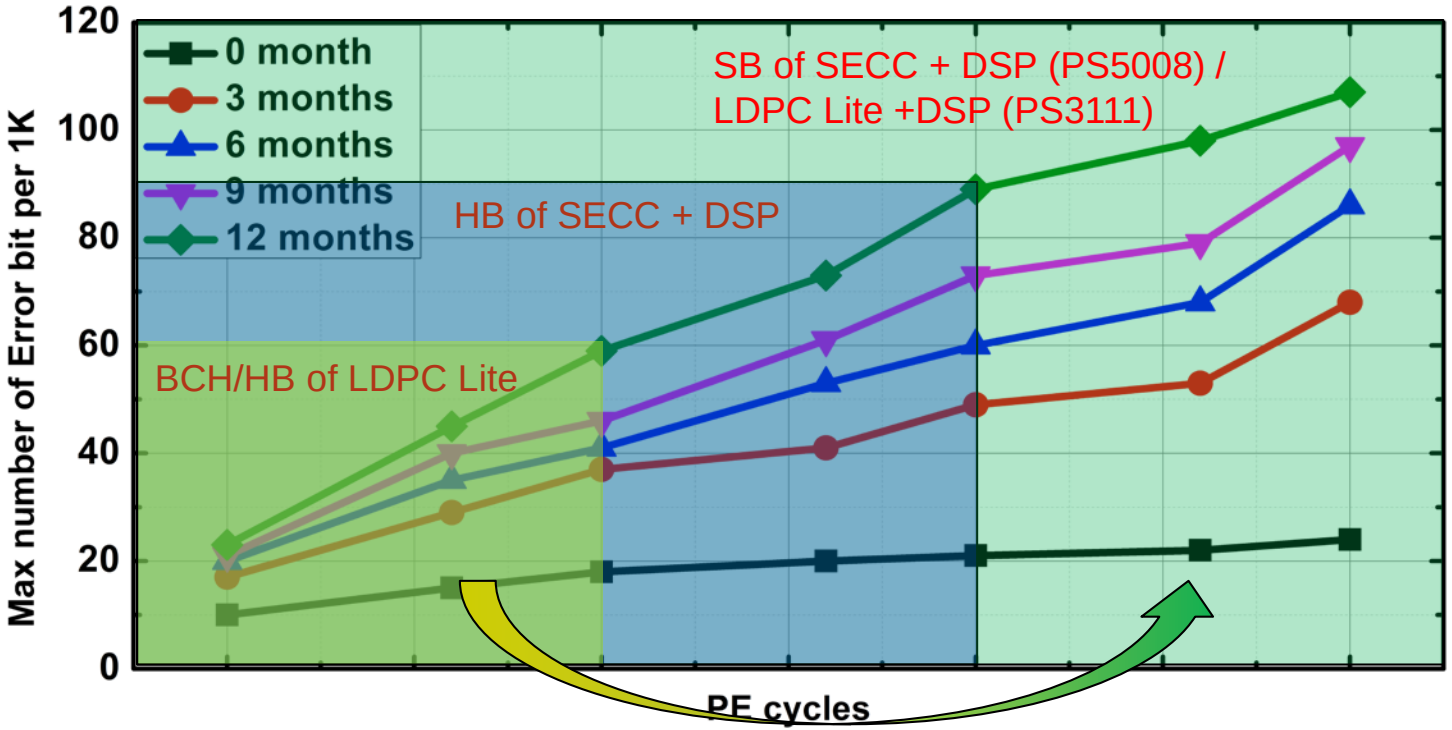


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# Conclusion

- The power consumption of the LDPC lite and SECC engine are only 1/3 than the convention BCH.
- With the novel design of decoding algorithm, the cost of LDPC can be reduced effectively.
- The endurance of 3D NAND Flash can be 3X more extended by SECC and LDPC lite with DSP engine.

# Meet us at booth 714 & 716


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