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Comparison of NAND Flash Functionality with Internal Probing and Waveform Analysis

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TechInsights Inc.

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Overview

- NAND flash SSD overview and logical vs. physical addressing
- Important test and analysis points
- NAND flash internal waveform analysis
  - Jet-etching and probing
  - Internal waveforms and states
- SSD controller to NAND flash interface
  - Interposing for testing
  - Standards (ONFI, Toggle) and customizations
- VNAND

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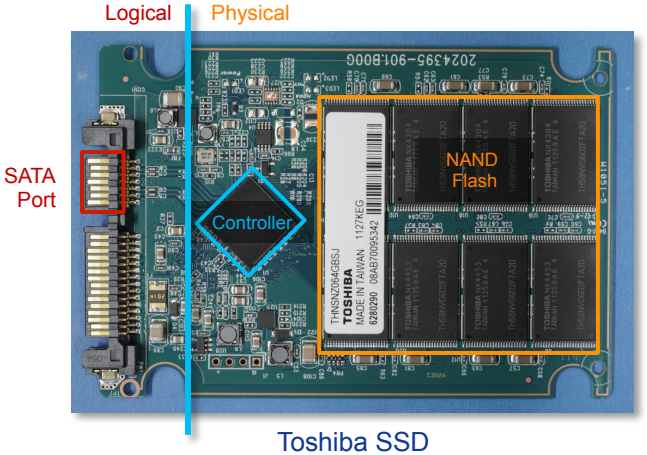
NAND Flash SSD Overview

- A port for host requests, such as SATA, USB, PCIe, eMMC, UFS, etc.
- Controller and many NAND flash memory devices
- Controller translates host requests to NAND flash memory requests
- The host cannot control the physical addressing (i.e., NAND flash).

Logical Address:
0
1
…
4000000
…



Toshiba SSD

Physical Address:
Channel 1, 2, …
Chip 1, 2, …
Block 1, 2, …
Page 1, 2, …
Column 1, 512, …

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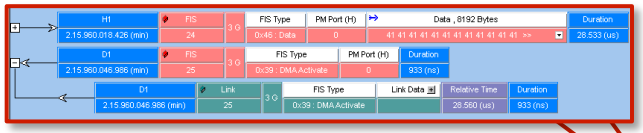
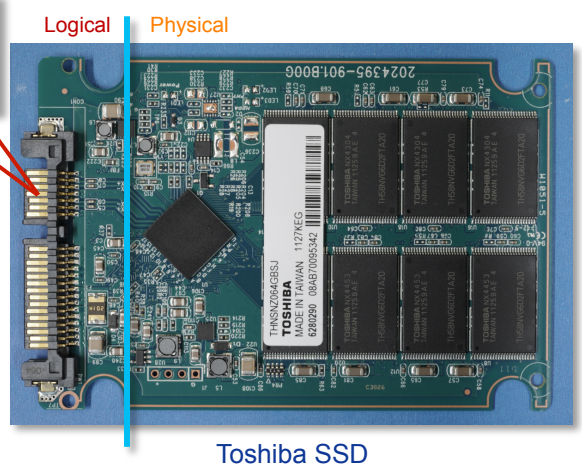
Important Test and Analysis Points

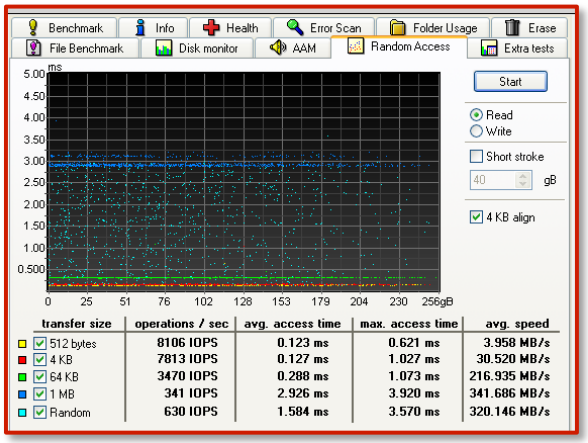
- Host side testing and analysis can be done
  - Simple host benchmarking and testing SW
  - Protocol analyzer (e.g., SATA analyzer)
  - Limited (access rates, speculation, etc.)



SATA Protocol Analysis



Toshiba SSD

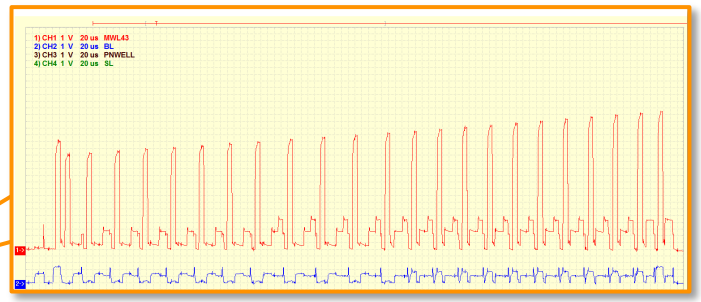


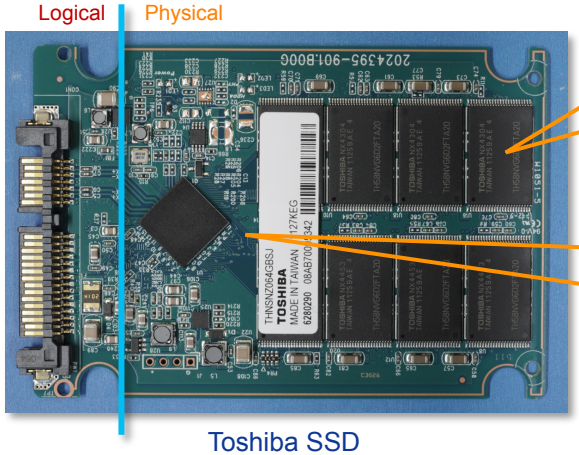
SATA I/F Benchmarking

Important Test and Analysis Points

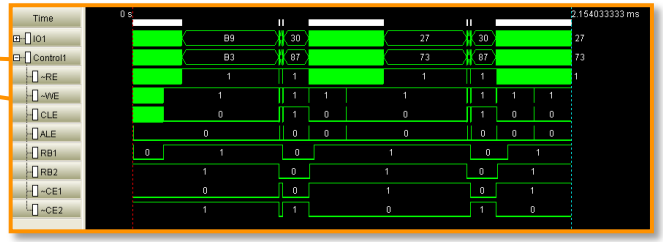
- Physical side has some interesting points for test and analysis
  - Internal flash operations (e.g., WL, BL, SL, etc.)
  - Controller to flash interface (ONFI, Toggle)

Internal NAND Flash Waveform Analysis





Toshiba SSD



NAND Flash Interface Signals

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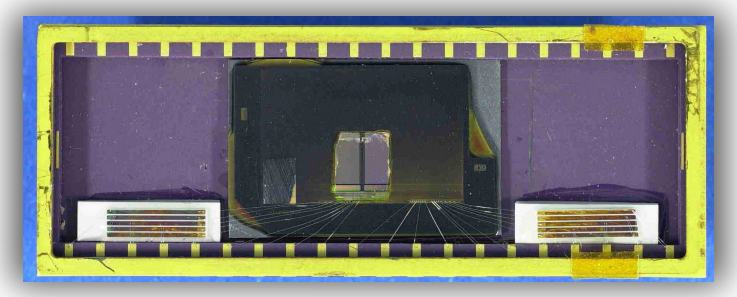
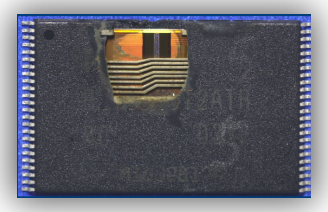
NAND Flash Waveform Analysis

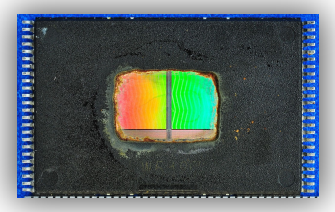
- Jet etch to expose die for FIB pad placement for IC probing
- Challenges can include:
  - packaging obstructions
  - BGA to programmer translation
  - device repackaging (e.g., SD card) for direct NAND flash connectivity to programmer.

Re-wiring NAND flash in SD card

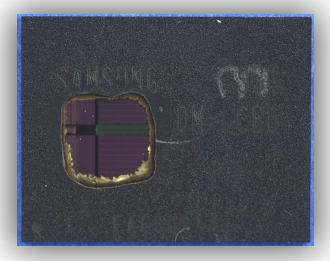




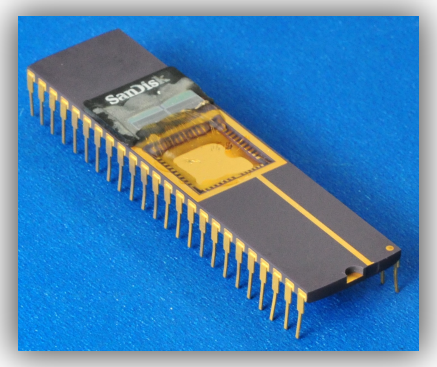
Cut lead frame



Bottom side



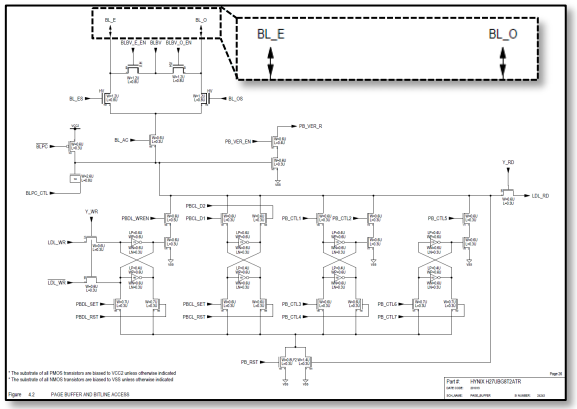
BGA



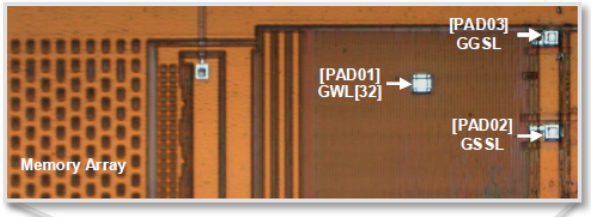
Re-wiring NAND flash in SD card

NAND Flash Waveform Analysis

- FIB pad placement challenges with shrinking NAND flash:
  - Requires initial circuit extraction from the NAND flash IC
  - Metallization thickness, M1 vs M2 for FIB connection
  - BL pitch to get BL signals!

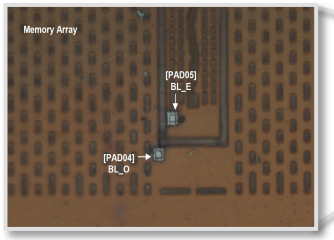


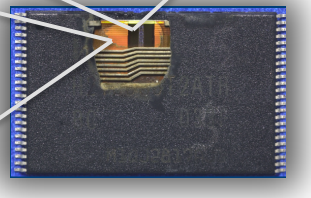
Circuit Extraction



Pad location A

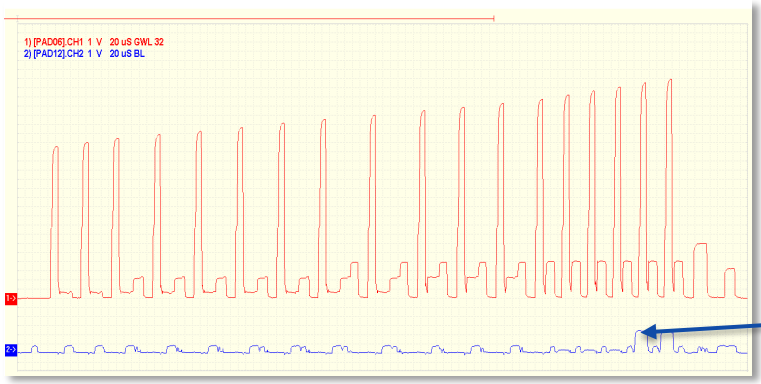
Pad location B





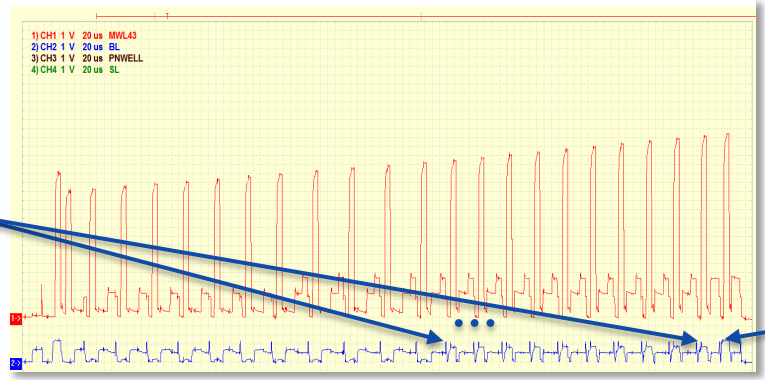
NAND Flash Waveform Analysis

- Fine tuning of programming during ISPP
- Raised BL voltage during programming pulses before inhibit
- Increased BL voltage during verify and small voltage difference (sensing scheme)



SanDisk/ Toshiba 43 nm MLC

Inhibit



SanDisk/ Toshiba 19 nm MLC

Raised BL voltage during pulse

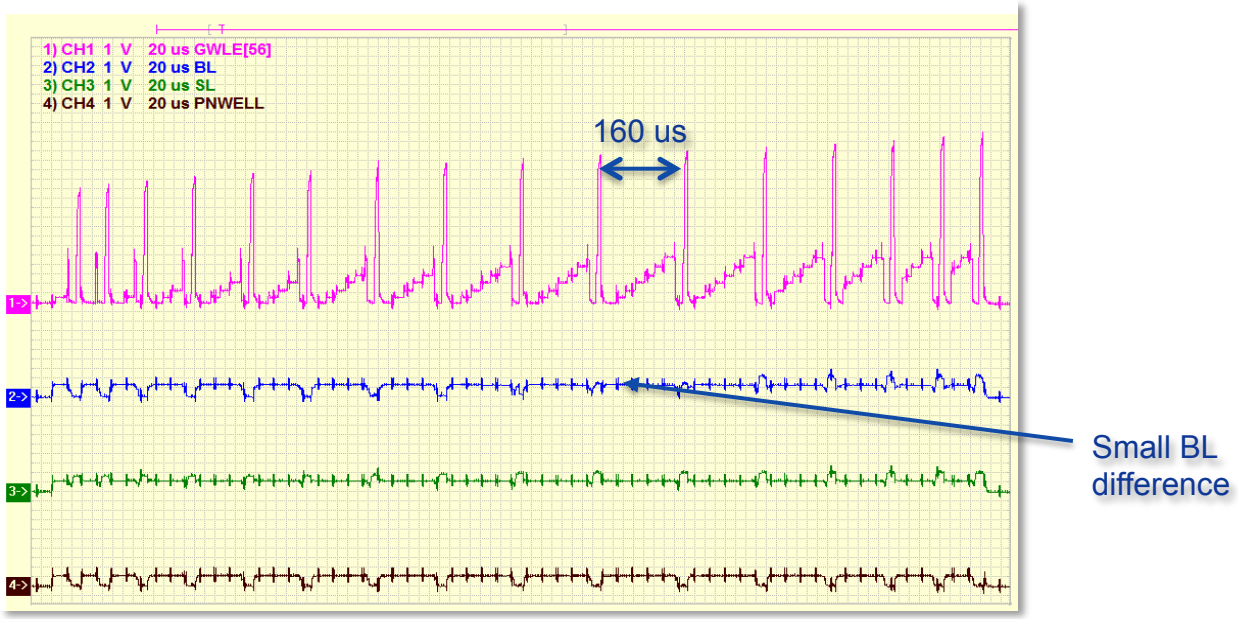
Inhibit

NAND Flash Waveform Analysis

- TLC verify extends programming time (~2x pulse-to-pulse)
- Sensing during verification produces small BL differences

SanDisk/
Toshiba
15 nm
TLC

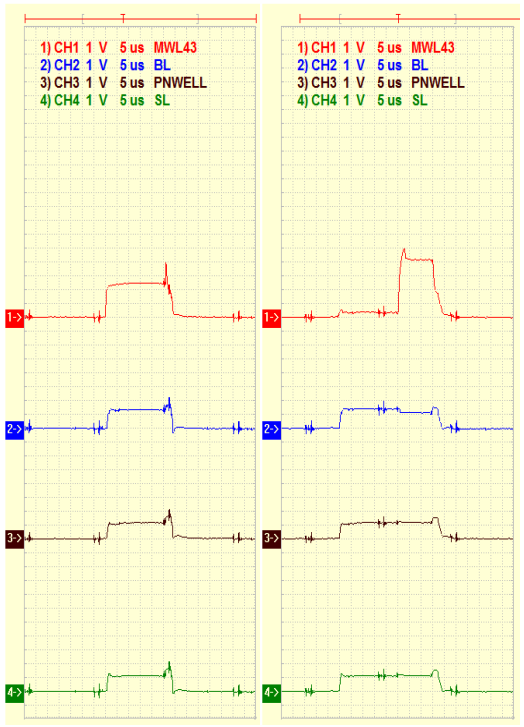
Middle page program



NAND Flash Waveform Analysis

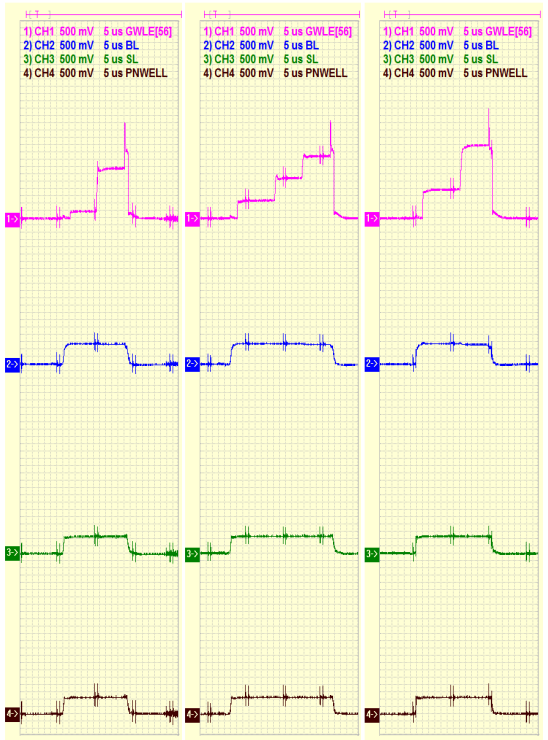
- Reading is simpler in MLC vs. TLC
- TLC requires many more read voltages

SanDisk/Toshiba 19 nm MLC



LSB *MSB*

SanDisk/Toshiba 15 nm TLC



Lower *Middle* *Upper*

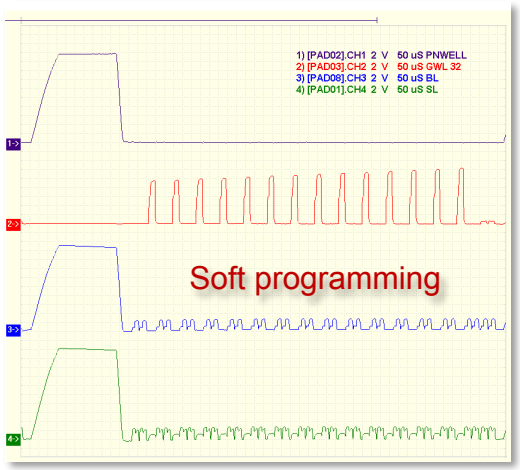
NAND Flash Waveform Analysis

- Variations in erase algorithms
- Single large pulse and programming

Micron 34 nm MLC

Samsung 42 nm MLC

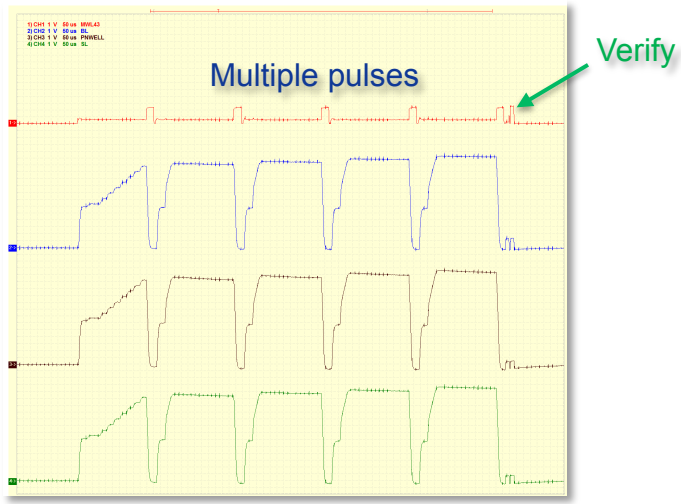
SanDisk/Toshiba 43 nm MLC

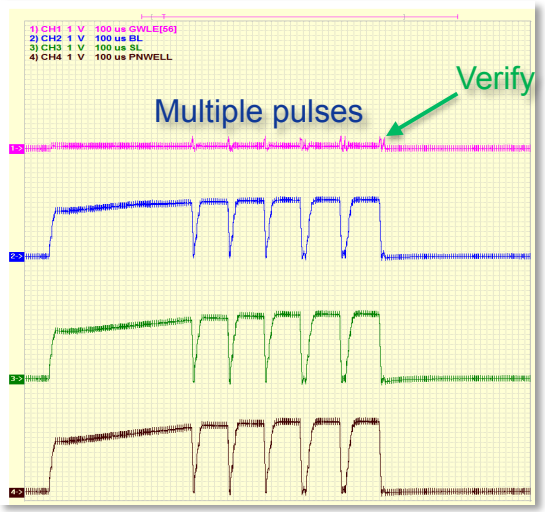


NAND Flash Waveform Analysis

- Variations in erase algorithms
- Multiple pulses and verification

SanDisk/
Toshiba
19 nm
MLC



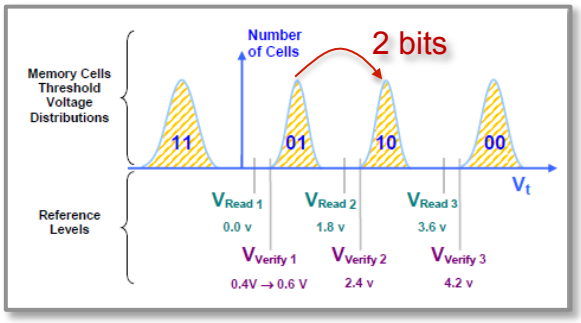


SanDisk/
Toshiba
15 nm
TLC

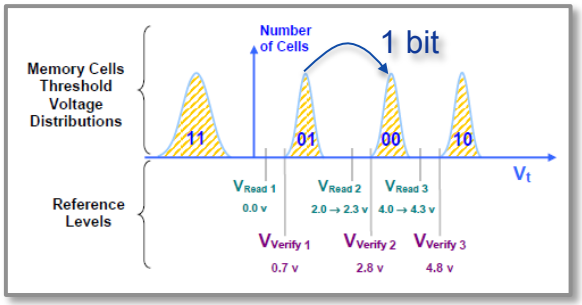
NAND Flash Waveform Analysis

- 2-bit change between states implemented across the industry around the 5x/4x nm node
- Changed to single bit change from state to state

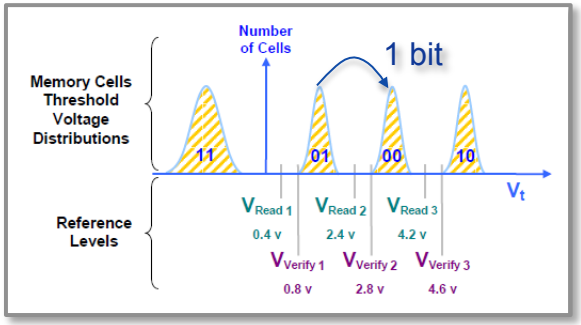
Samsung 42 nm MLC



Samsung 35 nm MLC



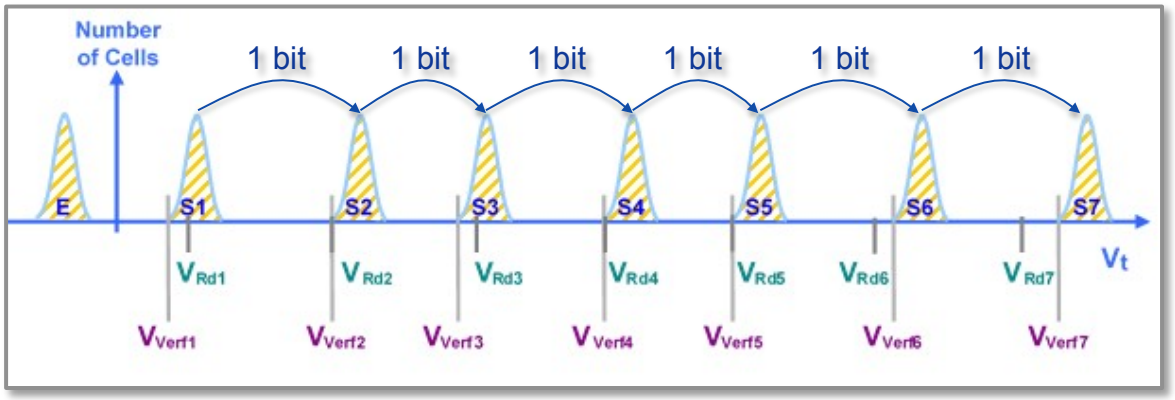
SanDisk/Toshiba 19 nm MLC



NAND Flash Waveform Analysis

- 2-bit change between states implemented across the industry around the 5x/4x nm node
- Changed to single bit change from state to state – including TLC

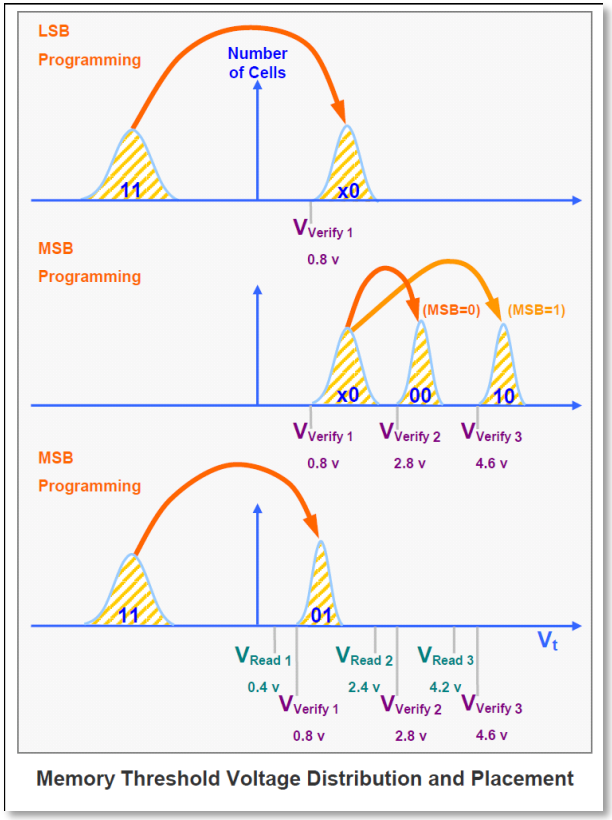
SanDisk/Toshiba 15 nm TLC



NAND Flash Waveform Analysis

- Simpler programming for 2 bits/cell
- LSB page and MSB page can be programmed at different times (page addressing)

SanDisk/Toshiba 19 nm MLC

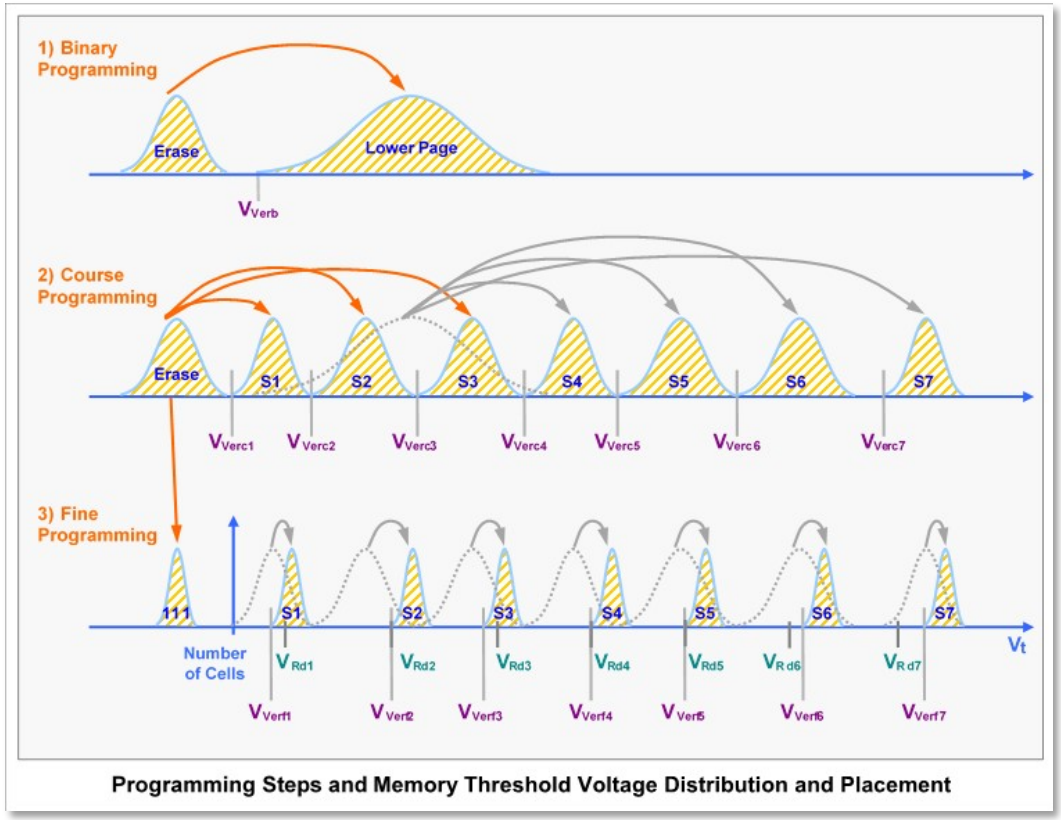


Memory Threshold Voltage Distribution and Placement

NAND Flash Waveform Analysis

SanDisk/Toshiba 15 nm TLC

- TLC devices can require all 3 pages of data together (WL addressing), multiple times



Programming Steps and Memory Threshold Voltage Distribution and Placement

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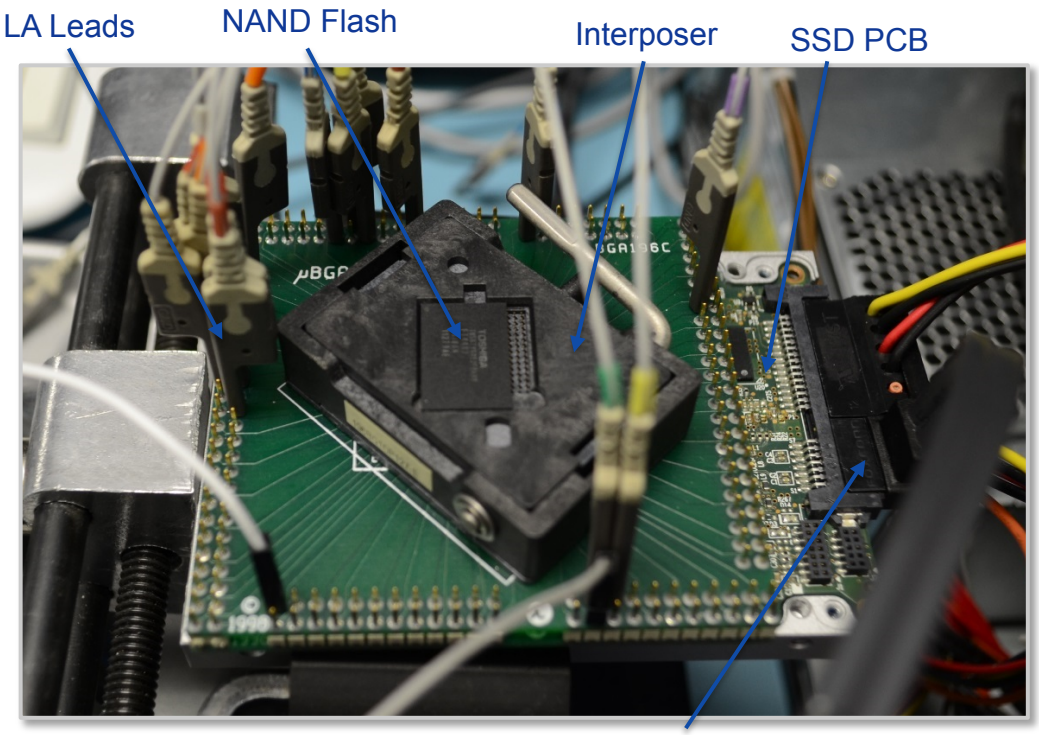
Controller to NAND Flash Analysis

- Simple clip-on interposers for TSOP-48 NAND flash
- BGA packages are more complex
- Case-by-case: many different standard pin-outs
- Can also be non-standard pin-out; would need to first reverse engineer pin-outs



*Testing and analysis of HGST SATA SSD

Controller to NAND Flash Analysis

- ONFI and JEDEC Toggle NAND Standards
- Customizations:
  - Raw NAND controllers
  - BGA layouts
  - Command sets
- Example of custom commands, SSD Boot-up:

  …

  0x70 – Read Status

  0xEF – Set Features

  0xC3 – Vendor Specific Command

  0x28 – Vendor Specific Command

  0xE7 – Vendor Specific Command

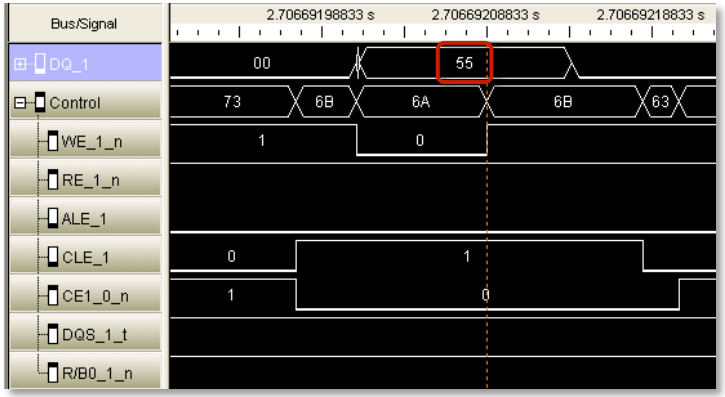
  0x55 – Vendor Specific Command

  …

Type	Opcode
Standard Command Set	00h, 05h – 06h, 10h – 11h, 15h, 30h – 32h, 35h, 3Fh, 60h, 70h, 78h, 80h – 81h, 85h, 90h, D0h – D1h, D4h – D5h, D9h, E0h – E2h, ECh – EFh, F1h – F2h, F9h, FAh, FCh, FFh
Vendor Specific	01h – 04h, 07h – 0Ah, 0Ch – 0Fh, 13h, 16h, 17h, 19h – 1Ah, 1Dh – 2Fh, 33h – 34h, 36h – 3Eh, 40h – 5Fh, 61h, 65h – 6Fh, 71h – 75h, 77h, 79h – 7Fh, 84h, 87h – 8Bh, 8Fh, 91h – CFh, D2h – D3h, D6h – D8h, DAh – DFh, E3h – EBh, F0h, F3h – F8h, FBh, FD – FEh
Reserved	0Bh, 12h, 14h, 18h, 1Bh – 1Ch, 62h – 64h, 76h, 82h – 83h, 86h, 8Eh

Table 91 Opcode Reservations

Source: Open NAND Flash Interface Specification, Rev 4.0



*Testing and analysis of HGST SATA SSD

Controller to NAND Flash Analysis

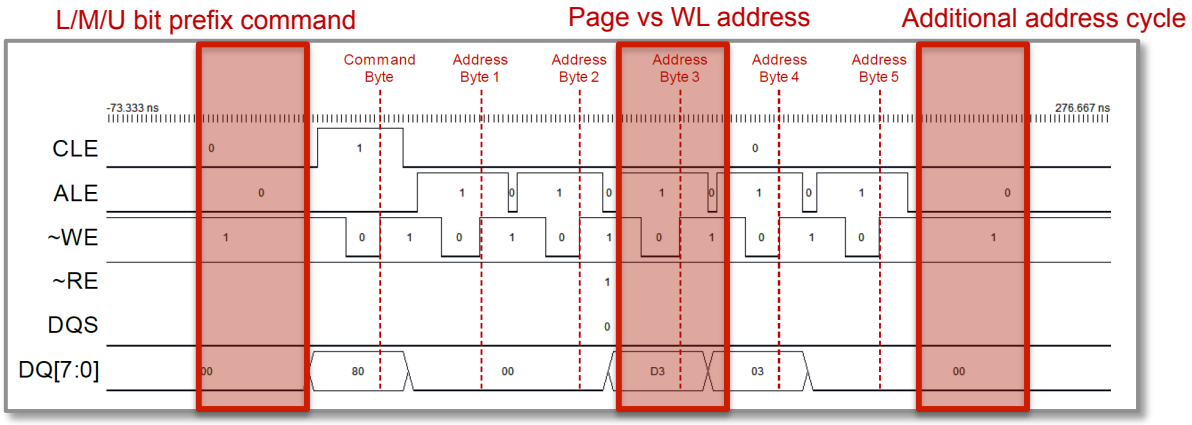
- Addressing dependent on NAND flash device
- Example typical 5 cycle addressing with column, page, block/ plane (SanDisk SSD):

Address Cycle	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]
1	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
2			CA13	CA12	CA11	CA10	CA9	CA8
3	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
4	BA6	BA5	BA4	BA3	BA2	BA1	BA0	PL
5					BA10	BA9	BA8	BA7

Page address

Controller to NAND Flash Analysis

- TLC and 3D NAND flash devices can greatly disrupt this
  - Page vs. WL + L/M/U bit command prefix
  - More address cycles will be needed
  - Locations of changes relative to standard addressing signals:



Controller to NAND Flash Analysis

- Logical blocking with multi-plane operations is the usual industry approach
- Reduced signalling with Status Check commands instead of Ready/Busy lines
- Example controller to NAND flash transactions excerpt (SanDisk SSD):

	Sample Time			Address Cycles										
Sample #	Start	End	Cmd	1	2	3	4	5	Command	Plane	Block	Page	Column	Data
28	20.000 ns	804.596706667 ms	70						Status check * 4					E0 E0
36	804.619170000 ms	804.689361667 ms	80	00	00	60	84	00	Program	0	66	96	0	1D AD 92 57 A8 64
17724	804.689420000 ms	804.689420000 ms	11						Data end					
17729	804.689601667 ms	804.689833333 ms	70						Status check					80 80
17736	804.690050000 ms	804.690281667 ms	70						Status check					E0 E0
17744	804.690520000 ms	804.757640000 ms	81	00	00	60	85	00	Program: multi-plane	1	66	96	0	60 9D 83 48 DC 4E
35433	804.757698333 ms	804.757698333 ms	10						Data end					
36733	804.758840000 ms	804.833320000 ms	70						Status check * 4993					80 80
77526	807.046306667 ms	9.680669426667 s	70						Status check * 270					E0 E0

- Industry preferences for certain commands, addressing, wear leveling, garbage collection, disturb management, etc. will be disrupted with TLC and 3D NAND
- New industry best practices going forward TBD

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VNAND

- 3D array and periphery configurations
  - Side-by-side
  - Stacked array over circuitry
  - Other future considerations (TSV)
- NAND flash standards
  - Pin-outs
  - Addressing
  - Control

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Thank you

For more information, go to
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