3D NAND Assessment for Next Generation Flash Applications

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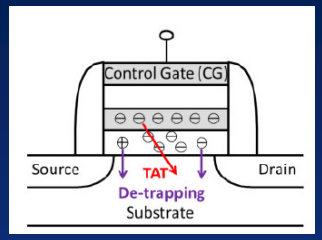
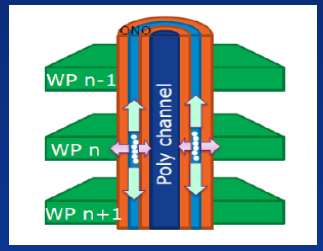
Agenda

- Industry Transition to 3D NAND
- 3D MLC NAND Assessment
- 3D TLC NAND Assessment
- Z-Dimension Cell-to-Cell Interference
- Arrhenius Activation Energy in 3D NAND
- Summary

Industry Transition to 3D NAND

- Challenges to continuing 2D NAND scaling are now significant
  - Cell-to-cell interference is dominant inhibitor
  - Significant pressure to maintain density growth and cost reduction trends
- 3D NAND architecture stacks cell layers vertically within single die
  - Wordline / bitline groundrules relaxed without sacrificing density
  - Reduced cell-to-cell interference improves threshold voltage distributions
  - Improved scalability achieved through increasing layer count
- Industry transition to 3D NAND is now definitive





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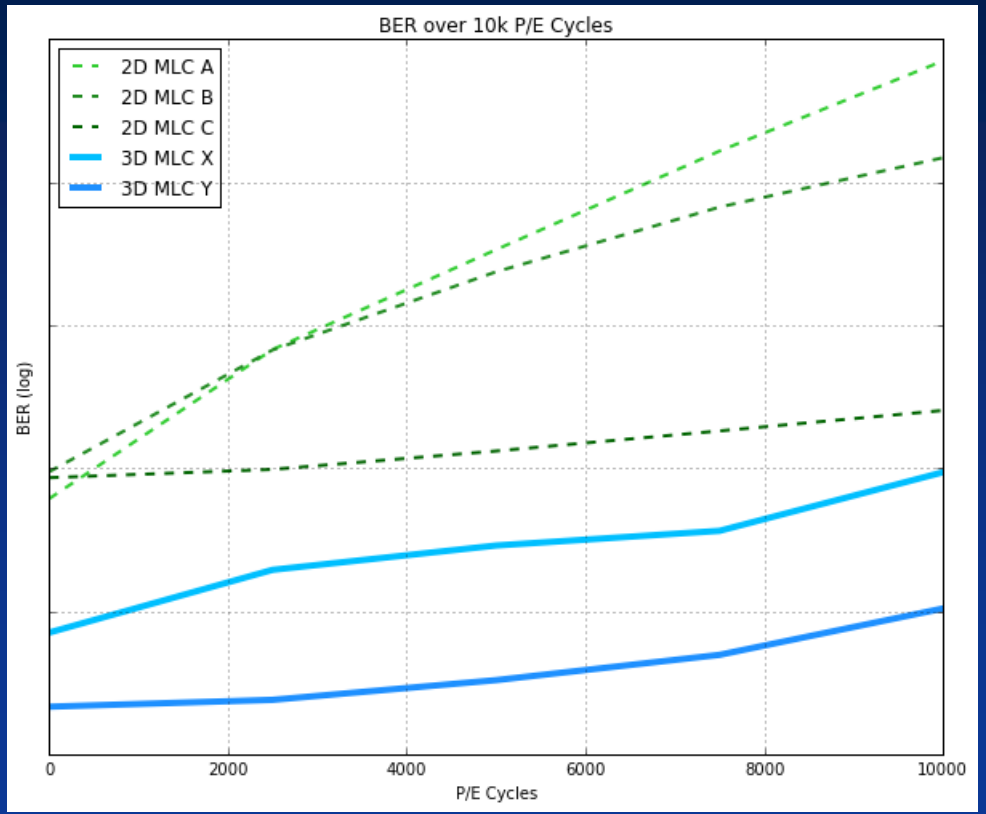
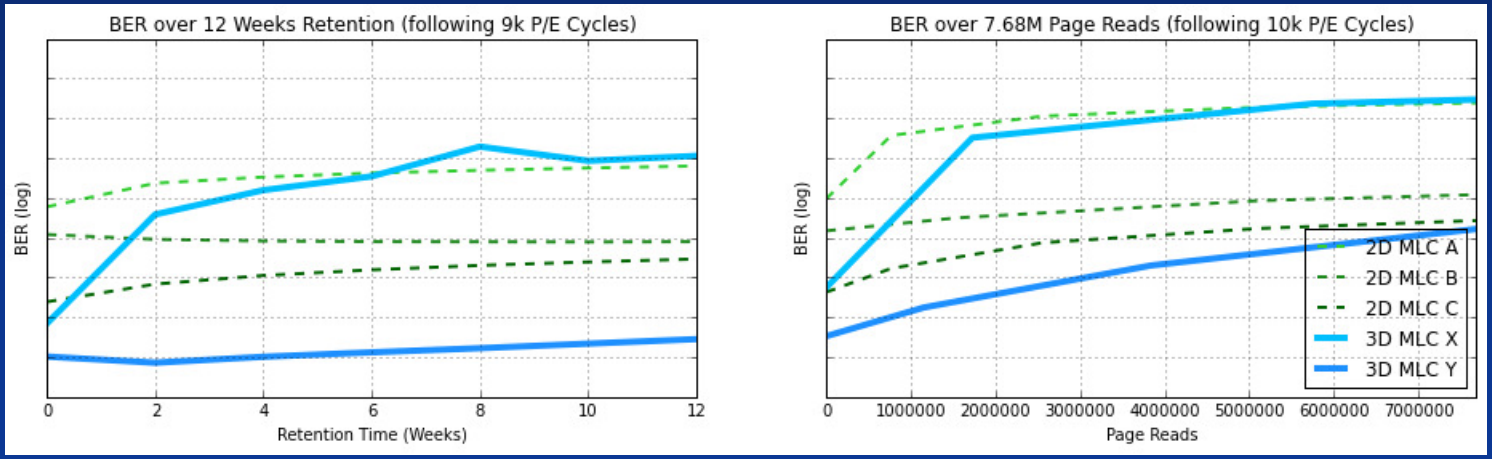
3D vs. 2D MLC - Program Erase Cycling

- Program erase cycling BER improved with 3D transition
- Significant variability observed across technologies



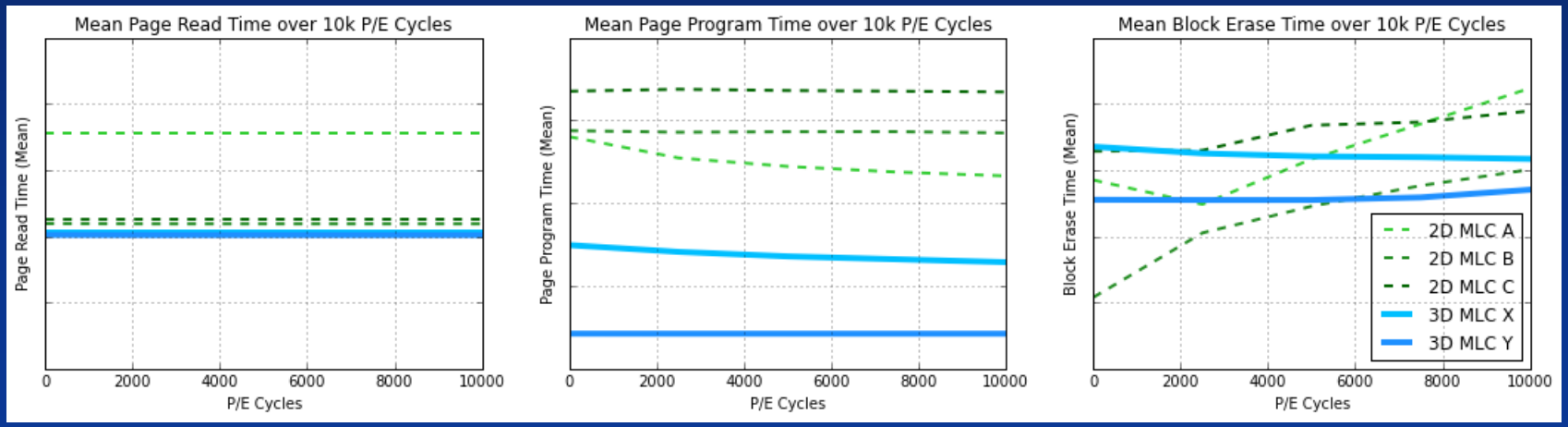
3D vs. 2D MLC - Data Retention and Read Disturb

- 3D MLC endurance advantage over 2D MLC degraded by follow-on data retention and follow-on read disturb characteristics
- Significant variability apparent across technologies



3D vs. 2D MLC - Timing Parameters

- Page Read times and Block Erase times similar between 3D and 2D
- Page Program times noticeably improved with 3D



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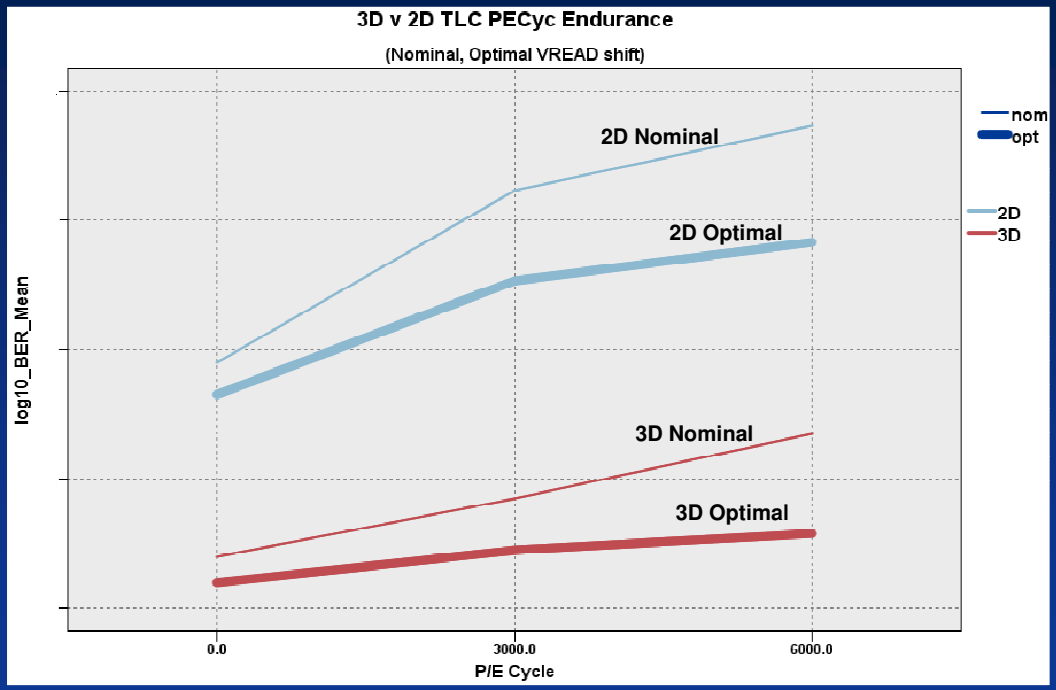
3D vs. 2D TLC - Program Erase Cycling

- 3D TLC Program Erase Cycling Endurance Bit Error Rate Improved over 2D TLC (6K Program Erase Cycles)

  Nominal = No VREAD Shift
  Optimal = VREAD Shift



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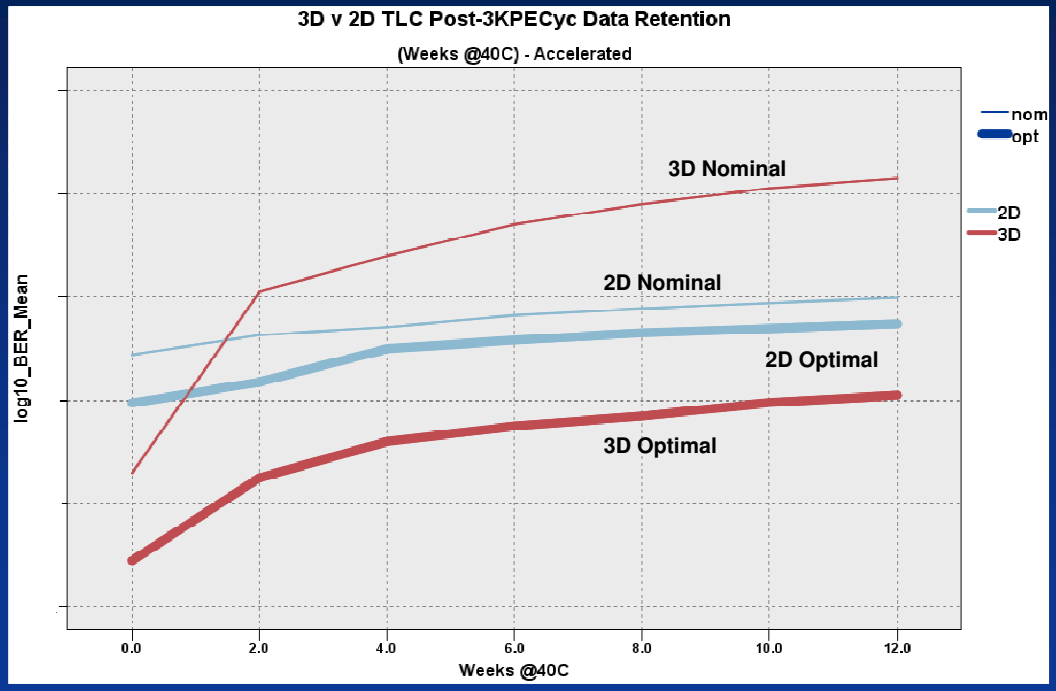
3D vs. 2D TLC - Data Retention



- 3D TLC shows higher nominal (no VREAD shift) post-3K PE Cycles Data Retention BER than 2D TLC
- However, better optimal gain (VREAD shift) for 3D TLC over 2D TLC
- 3D TLC shows higher initial Bit Error Rate trajectory

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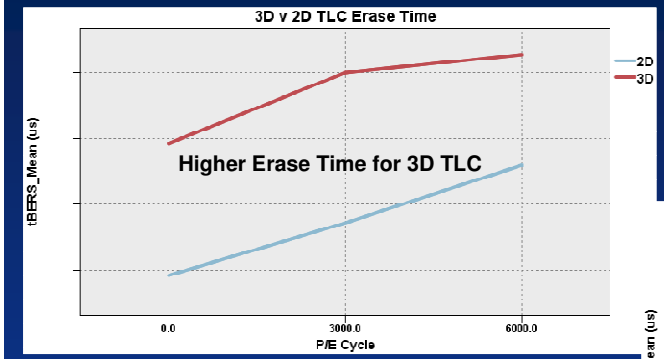
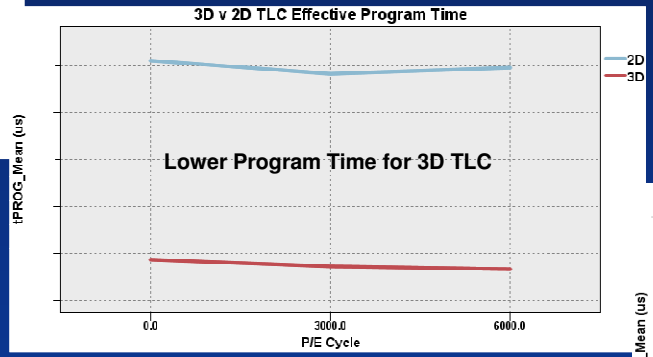
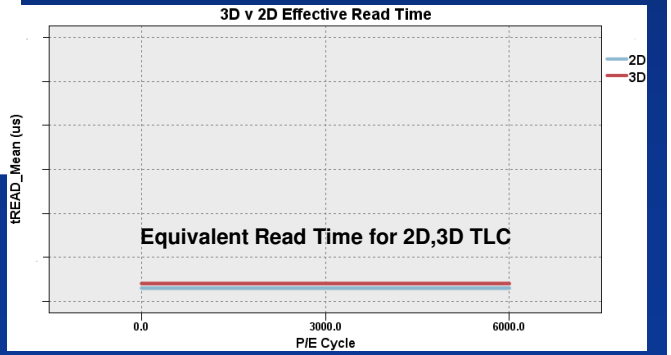
3D vs. 2D TLC - Timing Parameters

- Effective Program Time Improved for 3D TLC over 2D TLC (6K Program Erase Cycles)
- Block Erase Time Degraded for 3D TLC over 2D TLC (6K Program Erase Cycles)
- Effective Read Times for 3D TLC and 2D TLC are Equivalent



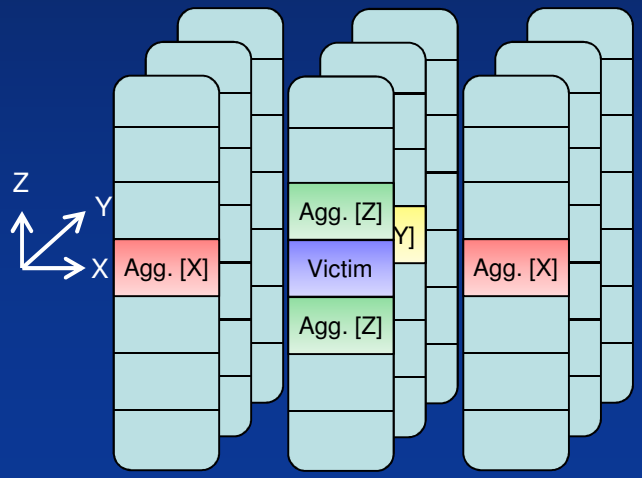




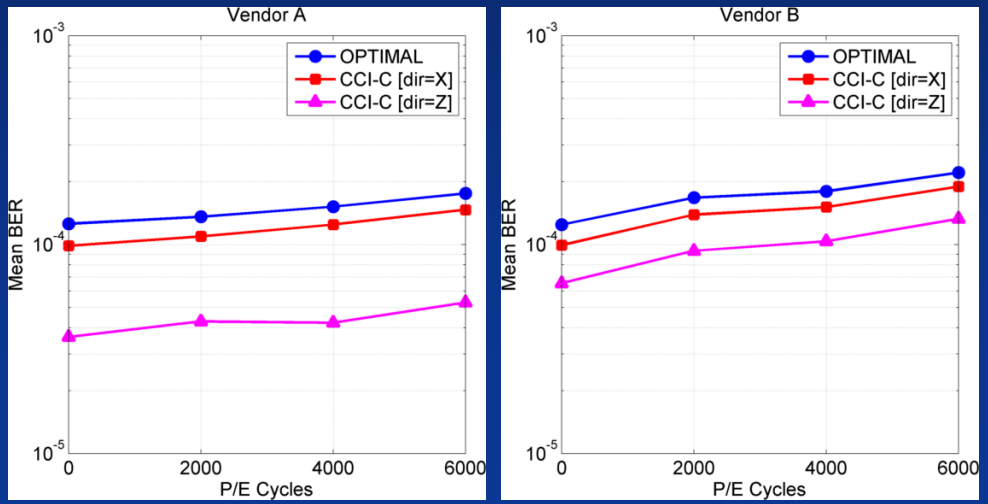
Z-Dimension Cell-to-Cell Interference (CCI)

- Programming of neighboring aggressor cells affects threshold voltage of victim cell
- Relaxed cell groundrules in 3D NAND result in reduced CCI in X/Y-direction
- However, vertical stacking of cells leads to new CCI effects in Z-direction

Aggressor Cells in 3D NAND Architecture



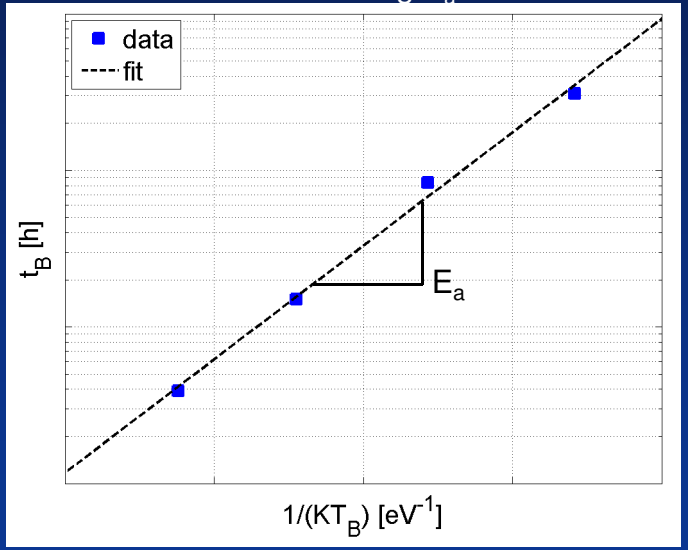
Cancelling of CCI in Z-direction - Significant Reduction in BER



Arrhenius Activation Energy in 3D NAND

- High-temperature acceleration of Flash aging is required for timely characterization of Flash devices
  - Acceleration factor depends on activation energy (E_a) of device under test
- Industry-standard activation energy for 2D NAND is 1.1eV
  - However, 3D NAND E_a no longer matches this value
  - Additionally, devices from different 3D NAND vendors exhibit different E_a values
    - Different technologies
    - Different materials / processes
- Careful design of characterization procedure is necessary to enable accurate acceleration of device testing during program erase cycling and data retention

Arrhenius determination for 3D MLC NAND Flash device showing E_a < 1.0eV



Summary

- Challenges to continuing 2D NAND scaling have become significant
- Industry transition to 3D NAND is now definitive
  - Reduced CCI and improved scalability
- 3D TLC is well positioned for enterprise design points based on observed capabilities
- Data retention and read disturb characteristics must be closely monitored with 3D NAND

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