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False Decoding Probability (Detection) of BCH and LDPC Codes

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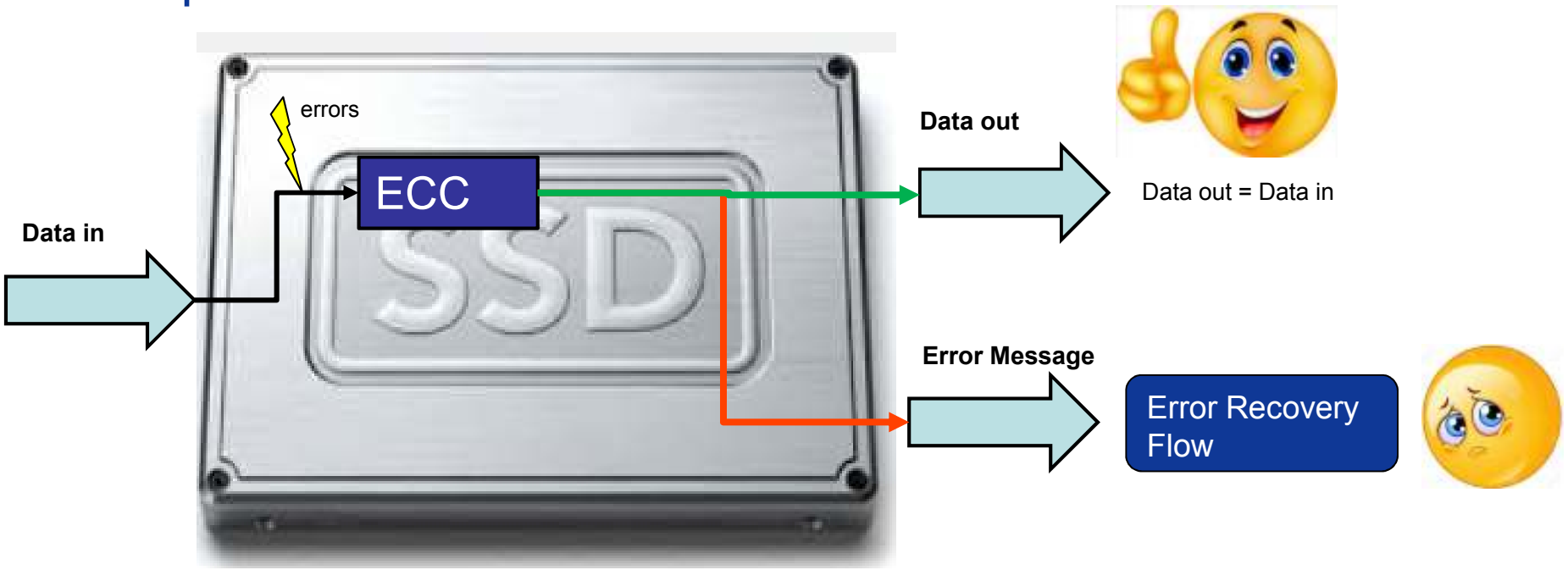
Agenda

- False decoding probability in SSDs
- BCH code
- LDPC code
- HW/SW co-simulation
- CRC concatenation
- Conclusions

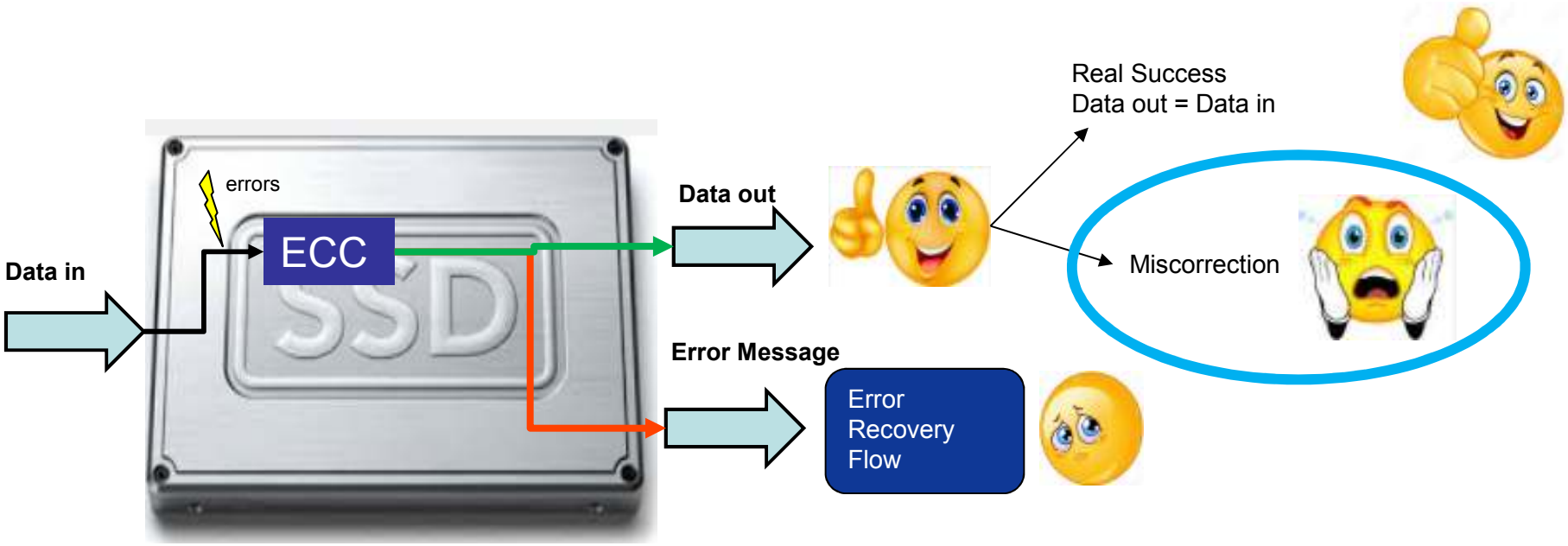
SSD's Built-in ECC

- When working with SSDs, we always rely on the error correction code (ECC) inside the code to correct all errors, or at least warn if the error capability of the code is surpassed



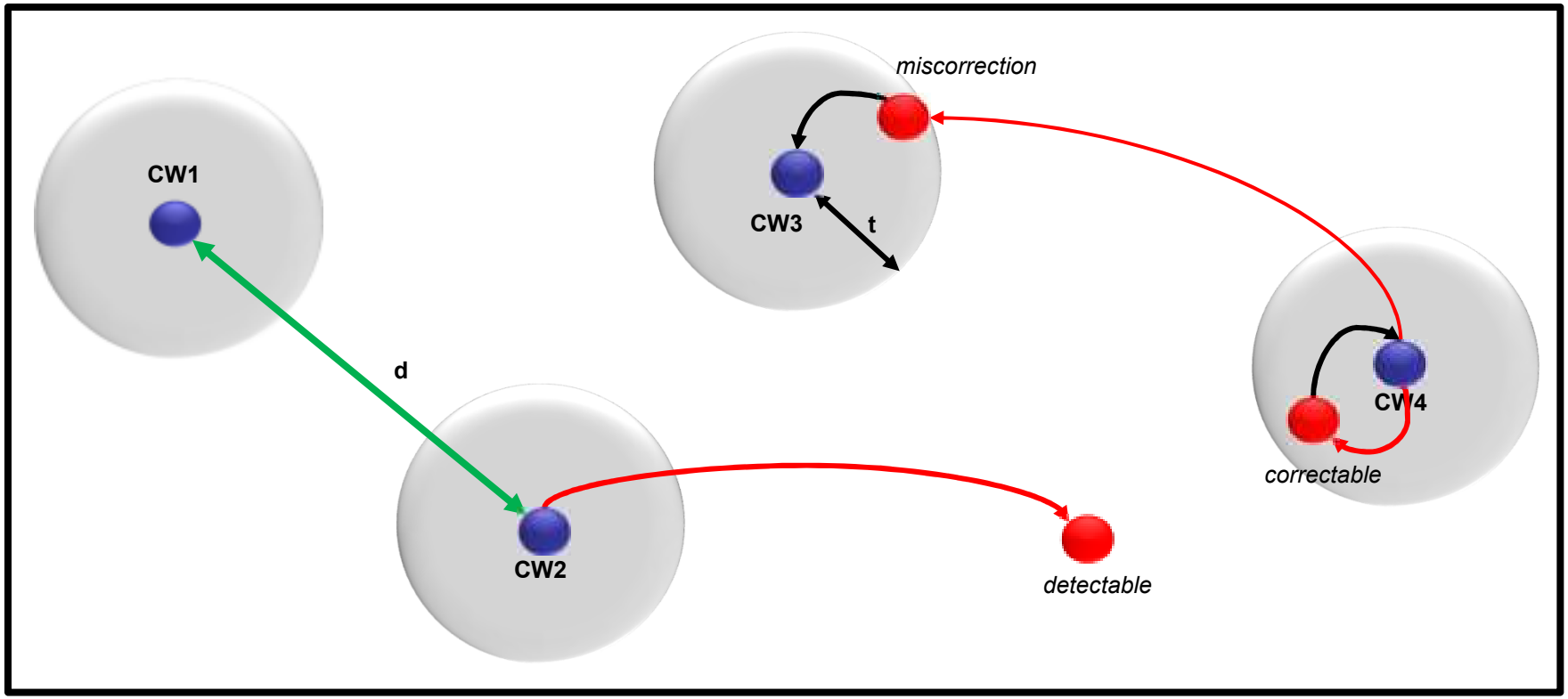
False Decoding Probability

- Unfortunately, there is a not-null probability of false decoding. This is when the ECC performs erroneous correction while declaring successful decoding (in practice, a silent, catastrophic event).

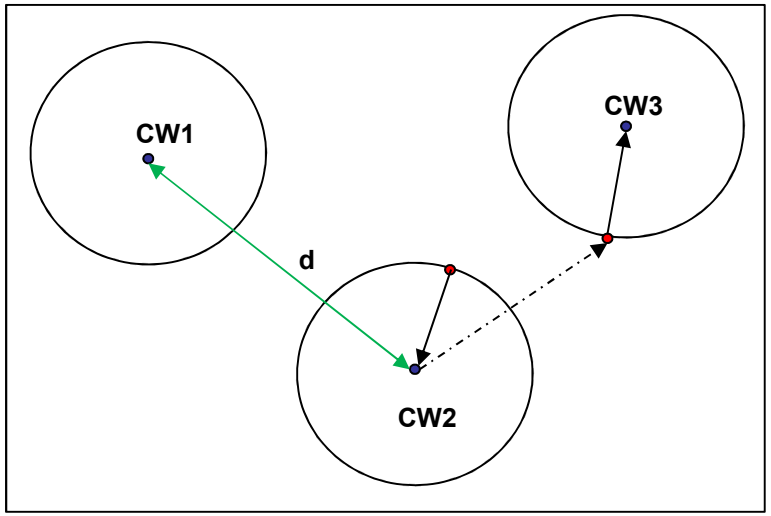


False Decoding: Why?

- False decoding is an intrinsic issue of any code
- No way to prevent it



Algebraic Space



- Hamming code is perfect and it corrects single-error. Whenever there is a double-error, miscorrections happen.
- BCH code is not perfect. In order to estimate the probability, we need to study the algebraic structure of the code.

$$P_E(w) = \frac{\sum_{l=0}^{n} a_l \sum_{s=0}^{t} N(l,w;s)}{\binom{n}{w}} \qquad t+1 \le w \le n$$

$$P_{ME} = \sum_{w=t+1}^{n} P_E(w)\phi(w)$$

$$\phi(w) = \binom{n}{w} p^w (1-p)^{n-w}$$

- w = Number of errors
- t = Number of correctable errors
- n = Codeword length
- a_i (weight) is the number of codewords having a 1-count equal to i
- $N(l,w;s)$ is the number of words with weight w at a distance s from a codeword with weight l

BCH Weights

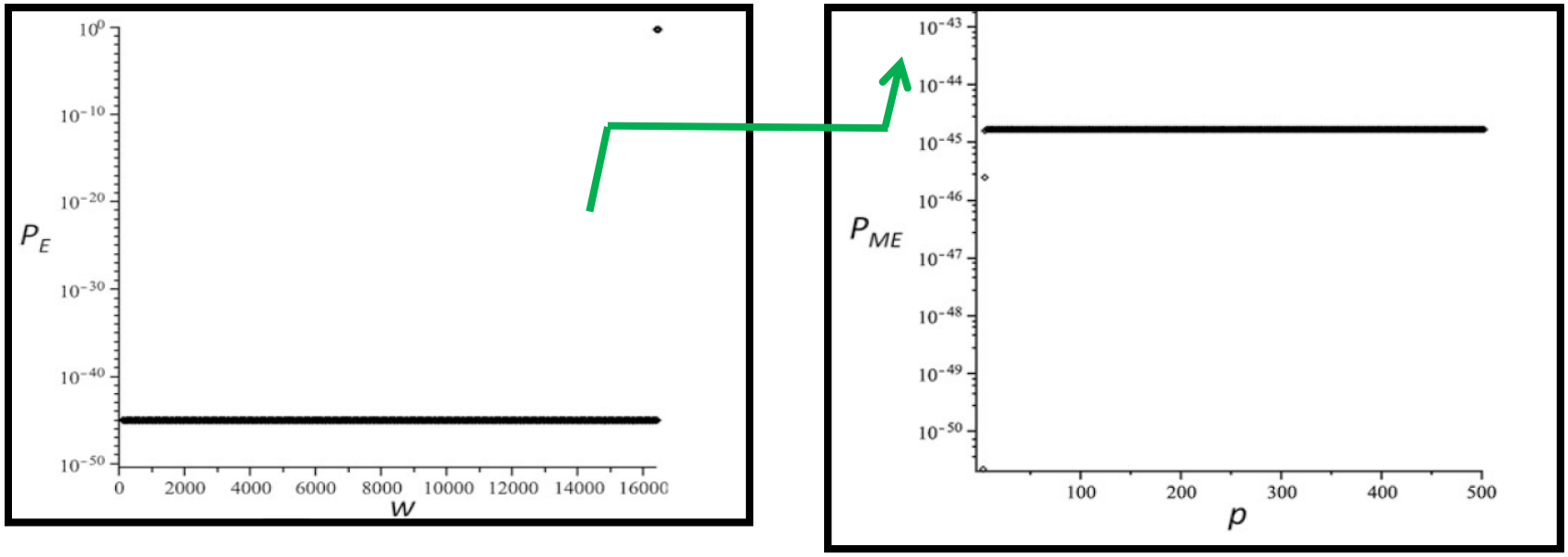
- BCH weights are unknown in most cases
- Therefore, estimates must be done

- Peterson estimate:
  - For a primitive BCH code with length *n* and correcting capability *t*, weights can be estimated as

$$a_i \cong \frac{\binom{n}{i}}{(n+1)^t}$$

- Successive estimates introduce a corrective term E_i to the formula

BCH[16893, 15851, 77]

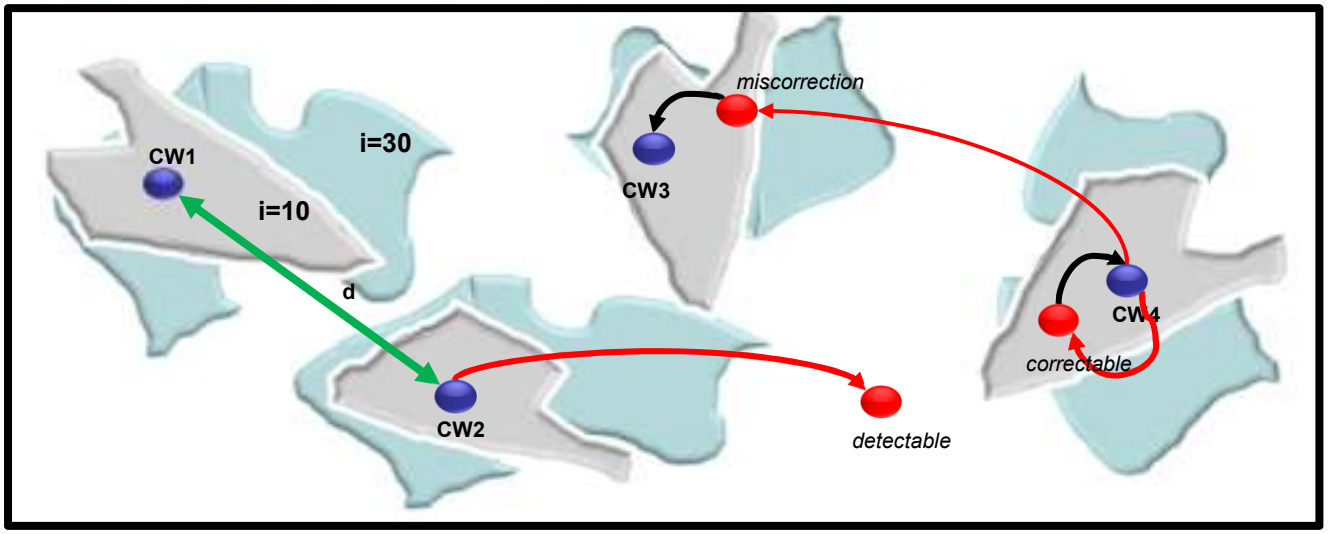


R. Micheloni, 3D Flash Memories, Springer 2016

- Probabilities have monotonic behavior with a long floor in the middle, approximated with $Q = 2^{-(n-k)} \sum_{s=0}^{t} \binom{n}{s}$
- BCH has very good detection capability for long codeword and high code rate

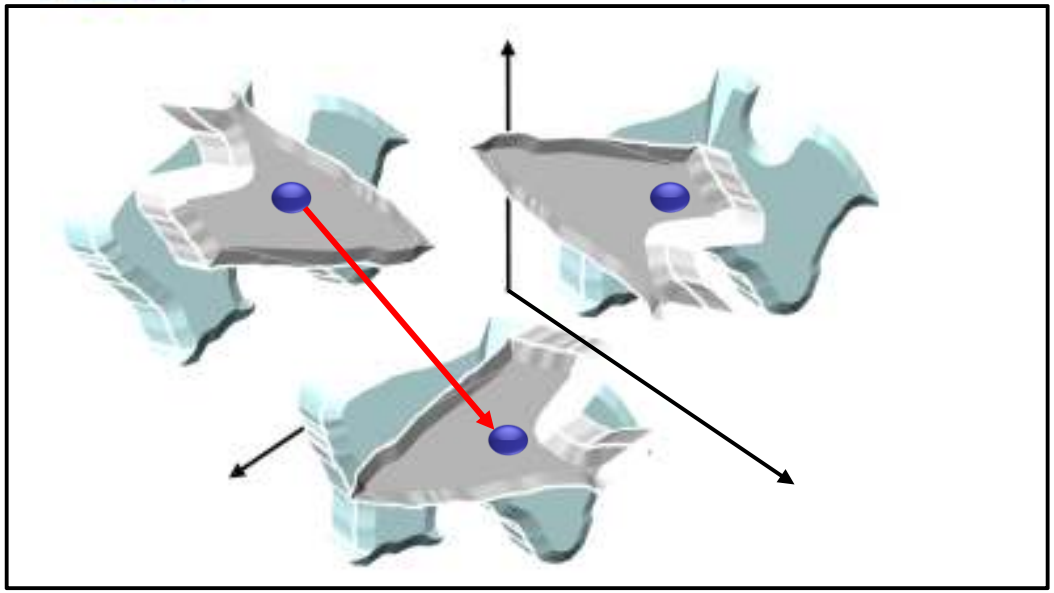
False Hard Decoding in LDPC

- Decoder is not Bounded Distance but Belief Propagation (BP)
- Weight estimation does not apply to BP. Therefore, the BCH approach is not applicable here.
- As the LDPC decoder is iterative, the “correctable region” changes with the number of iterations
- LDPC relies on its sparseness

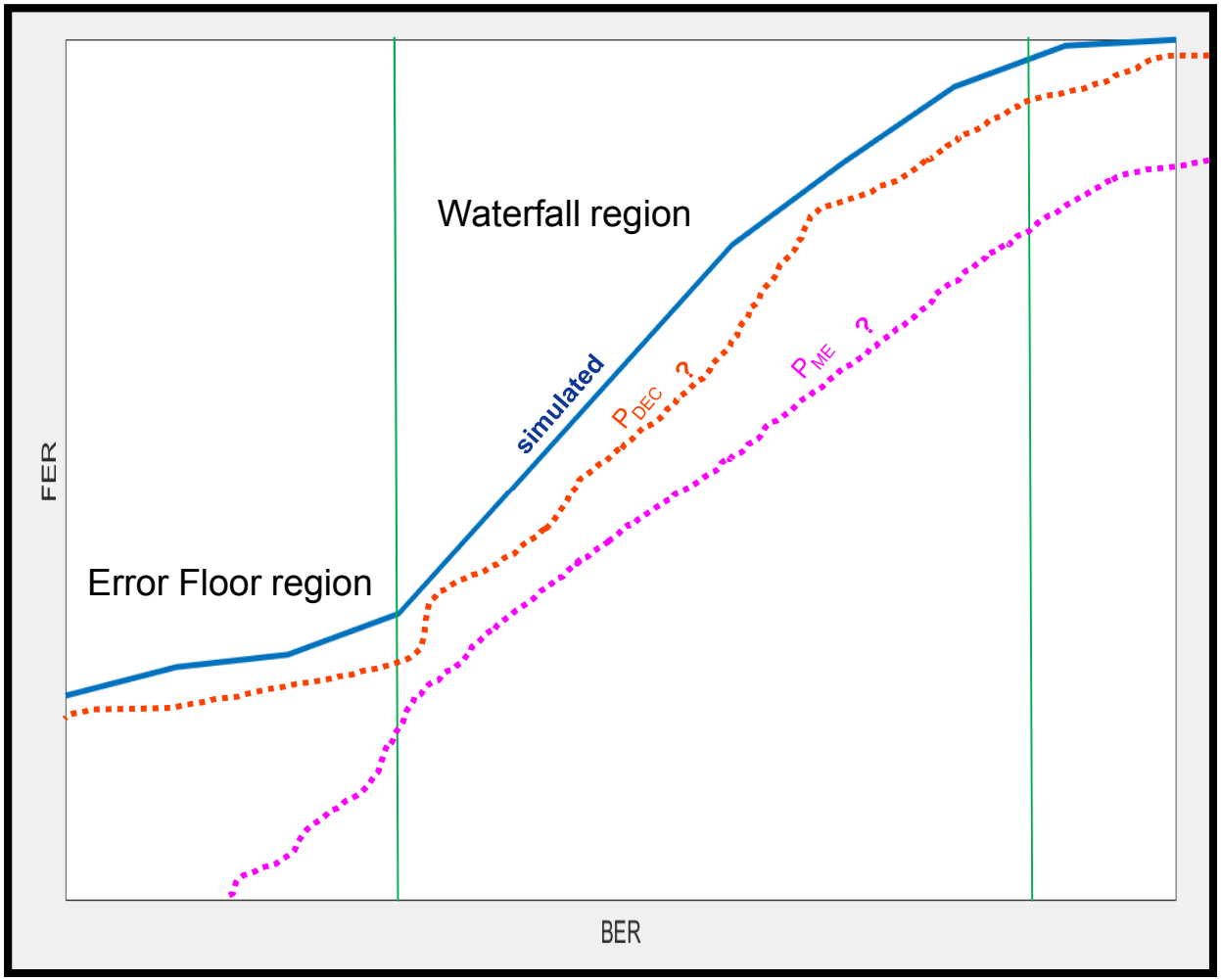


Soft False Decoding in LDPC

- With soft decoding, Hamming distance is replaced by Euclidean distance
- Even if the algebraic space changes, the false decoding probability does not, since we are still using BP
- Soft False Decoding probability can possibly be even higher in the soft case

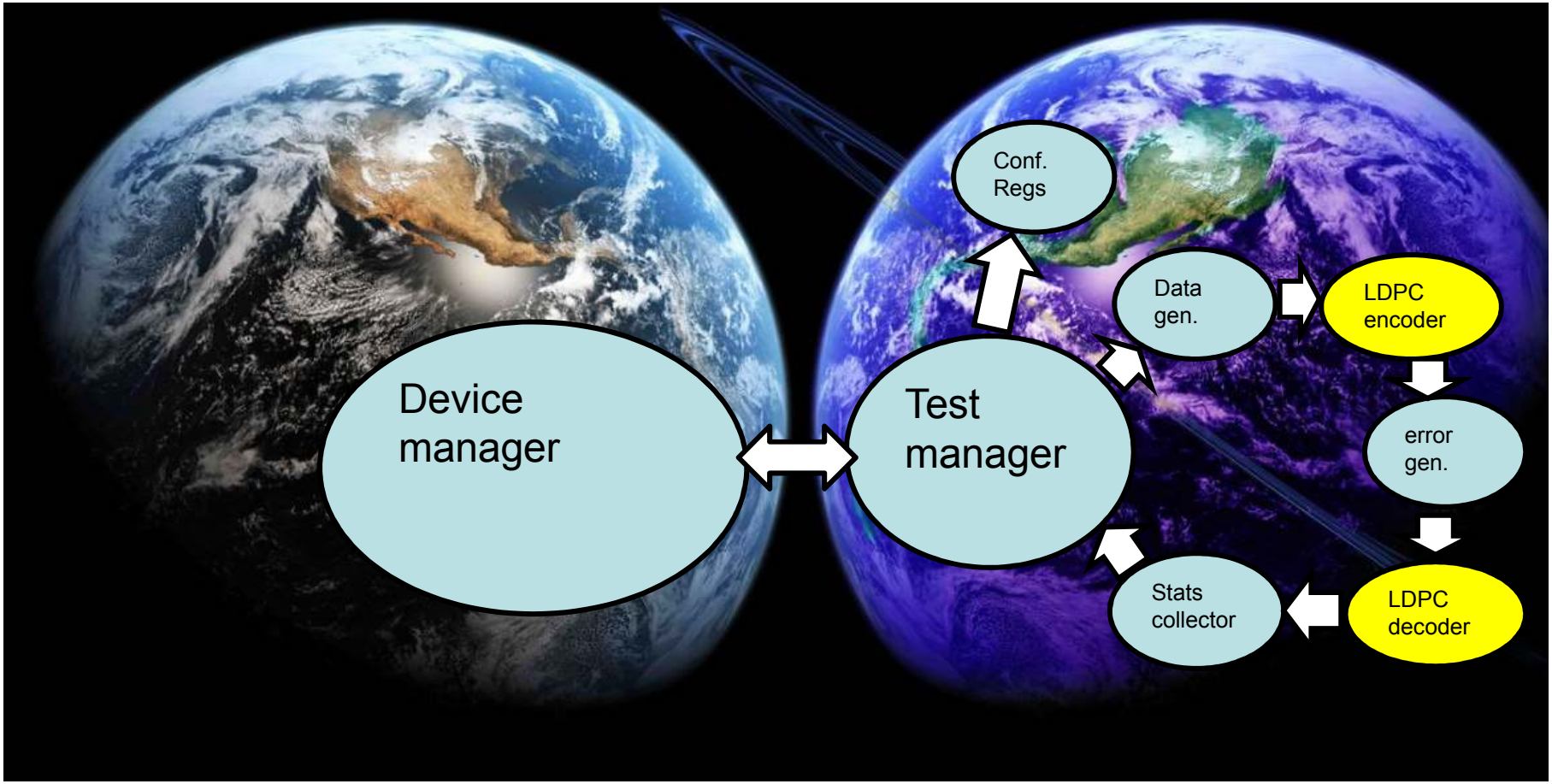


LDPC Simulations



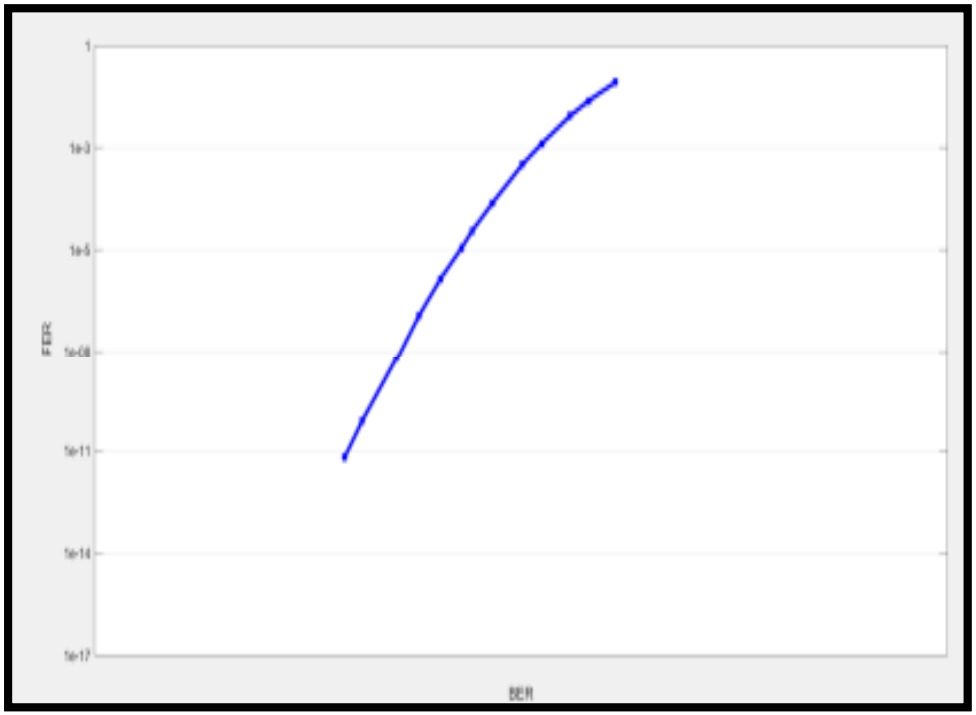
- The only way to estimate false decoding probability is through simulations
- FER = P_{ME} + P_{DEC}

HW/SW Co-simulation Flow



Simulation Speed

- An FPGA rack is used to accomplish the desired speed



- Able to reach FER 1e-11 on a weekly basis

CRC Concatenation

- A CRC can help lower the false decoding probability

CRC	P_{ME}(CRC)	P_{ME}(LDPC)	P_{ME}(concat)
CRC-16	$< 2*10^{-5}$	$< 10^{-11}$	$< 2*10^{-16}$
CRC-32	$< 2*10^{-10}$	$< 10^{-11}$	$< 2*10^{-21}$
CRC-48	$< 4*10^{-15}$	$< 10^{-11}$	$< 4*10^{-26}$
CRC-64	$< 6*10^{-20}$	$< 10^{-11}$	$< 6*10^{-31}$

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Conclusions

- False decoding can cause trouble in SSDs
- False decoding is an intrinsic issue of any code and cannot be avoided
- BCH code has a very low false decoding probability
- BCH weight estimation does not apply to LDPC
- False decoding + error floor can be estimated by HW/SW co-simulations
- Concatenation with CRC can be used to lower the probability of false decoding

Resources

- R. Micheloni, "3D Flash Memories", *Springer*, 2016.
- S. Lin, D. Costello, "Error Control Coding", *Prentice Hall*.
- R. Micheloni, A. Marelli, and K. Eshghi, "Inside Solid State Disks (SSDs)," *Springer*, 2012.
- R. Micheloni, L. Crippa, and A. Marelli, "Inside NAND Memories“, *Springer*, 2010.
- R. Micheloni, A. Marelli, and R. Ravasio, "Error Correction Codes for Non-Volatile Memories", *Springer*, 2008.

Thank you!

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