Low Error-Floor Soft-decision Finite Alphabet Iterative Decoders

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LDPC Design Issues and Goals

- Known issues in LDPC
  - Error floor problem (require FER of 1e-11 or lower)
  - Higher chip area and power
  - Requiring multiple reads for soft-decoding adding to read latency (to achieve higher RBER targets such as 1e-2)
- **Goal for this talk**: Achieve low error floor performance beyond RBER of 1e-2 using at most 3 reads for soft-decision decoding.
- Will focus on 1KB and 2KB codes (1KB are more prone to error floor).

FAID: New Decoding Approach

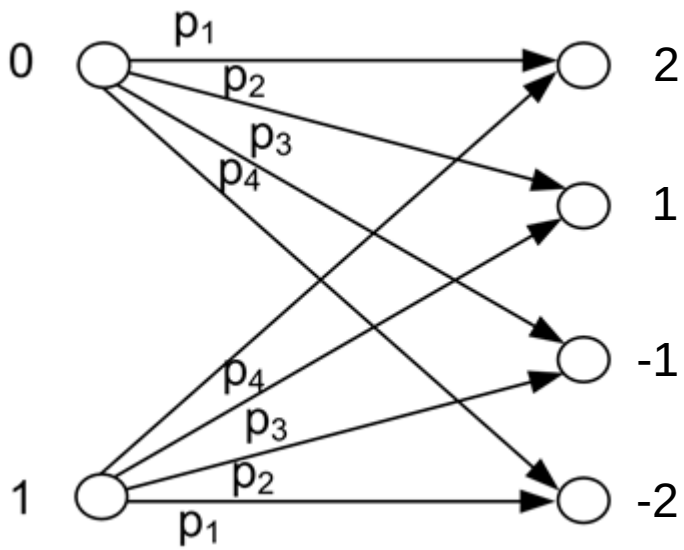
- Finite alphabet iterative decoding (FAID): messages belong to a finite alphabet represented as 0, ±1, ±2, etc.
- Check node update: same as a typical min-sum decoder (sign operation of messages along with minimum of magnitudes).
- The main differentiator is in the variable node update (VNU).
- VNU is a simple map designed to operate with 3-bit messages.

FAID: Hard-decision Decoding

- Y={-1,+1}, is the set of possible channel values.
- The VNU is a (d_v-1)-dimensional map or look-up table (LUT), where d_v is the column-weight.
- For d_v = 3, it is a 2D LUT (below). For d_v = 4, it is a 3D LUT.

m_1/m_2	-3	-2	-1	0	1	2	3
-3	-3	-3	-3	-3	-3	-3	-1
-2	-3	-3	-3	-3	-2	-1	1
-1	-3	-3	-2	-2	-1	-1	1
0	-3	-3	-2	-1	0	0	1
1	-3	-2	-1	0	0	1	2
2	-3	-1	-1	0	1	1	3
3	-1	1	1	1	2	3	3

FAID:Soft-decision Decoding(2-bit)



- 2-bit quantized AWGN – thresholds chosen to maximize mutual information
- The set Y is now Y={-2,-1, 1, 2}.
- Messages are still 3-bit messages.
- For d_v = 4, we now need to design two 3D LUTs, one for ±1 and for ±2
- They are chosen to optimize for both waterfall and error floor performance.

Hardware Implementations

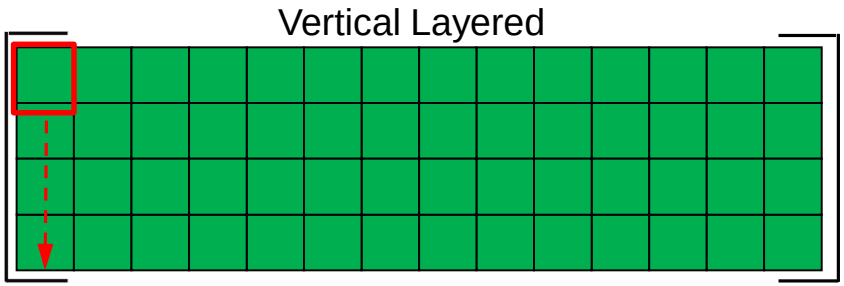
- Code Properties: Quasi-cyclic column-weight four codes.

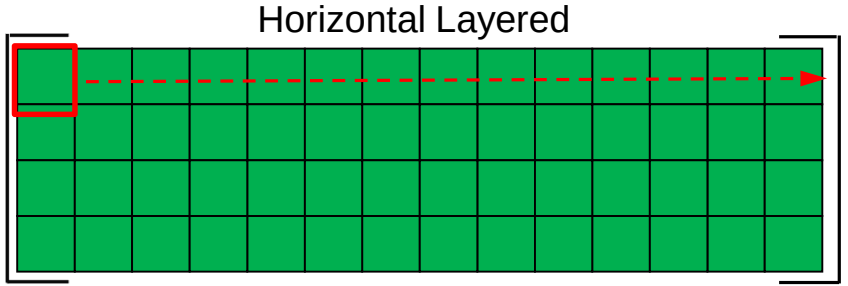
- Decoding Architecture: Vertical Layered
  - Current architecture processes 1 circulant/clock cycle
  - Can support flexible code rate and length
  - Single Architecture operating in hard or soft-decision mode.

- Hard-decision and 2-bit Soft-decision decoding (but can support additional reads).

Vertical vs Horizontal Layered

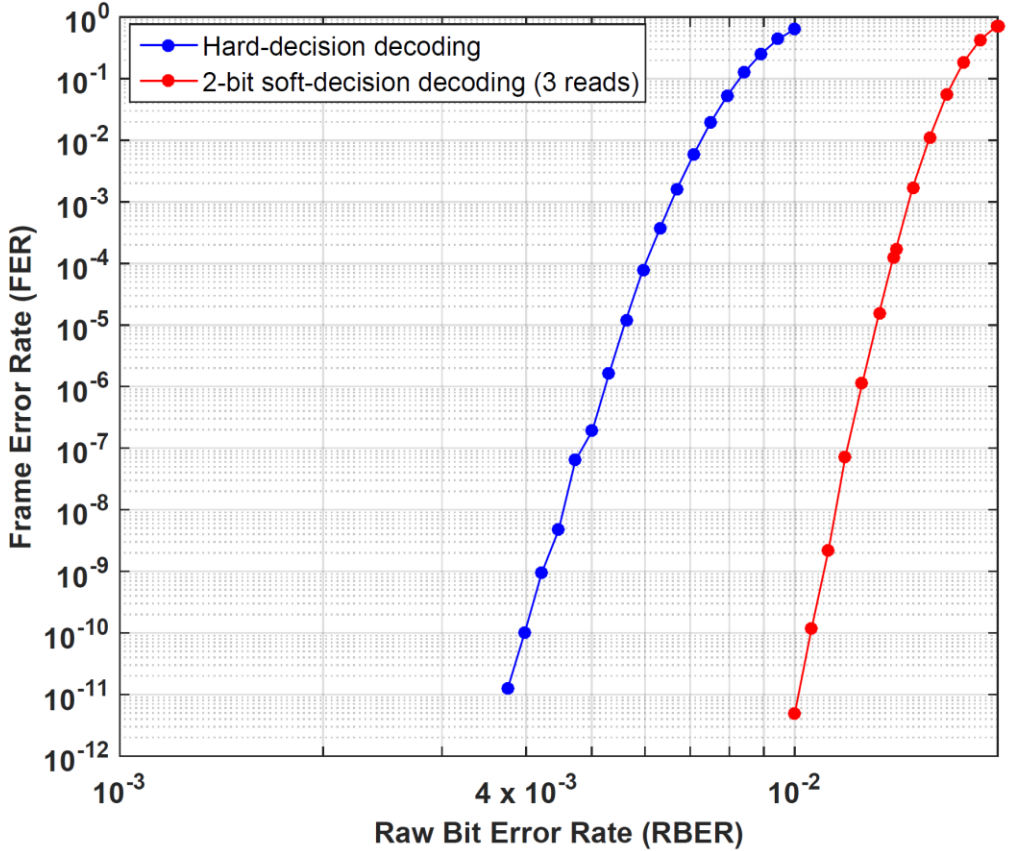
- Sequentially updating messages across columns (vertical layered) or rows (horizontal layered) of the parity-check matrix.





- Comparisons of both schemes using a 3-bit Min-sum with UMC 40nm at 250MHz
  - Chip area and power slightly lower for vertical layered (processing 1 circulant per clock cycle)

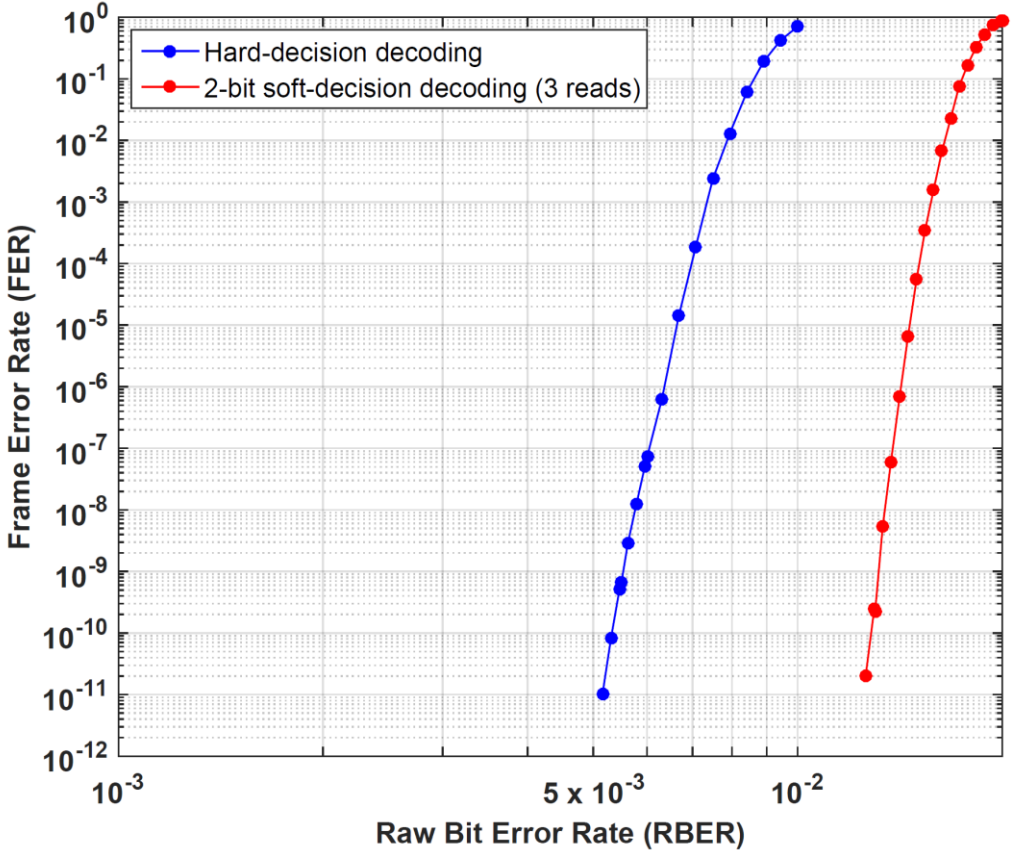
FER vs RBER Results: N=1KB, R=0.883



- No occurrence of error floor at FER of 1e-11.
- Achieves FER of 5e-12 at RBER of 1e-2 with 2-bit soft-decision (only 3 reads).

Results generated using multiple Xilinx Virtex-7 FPGA boards

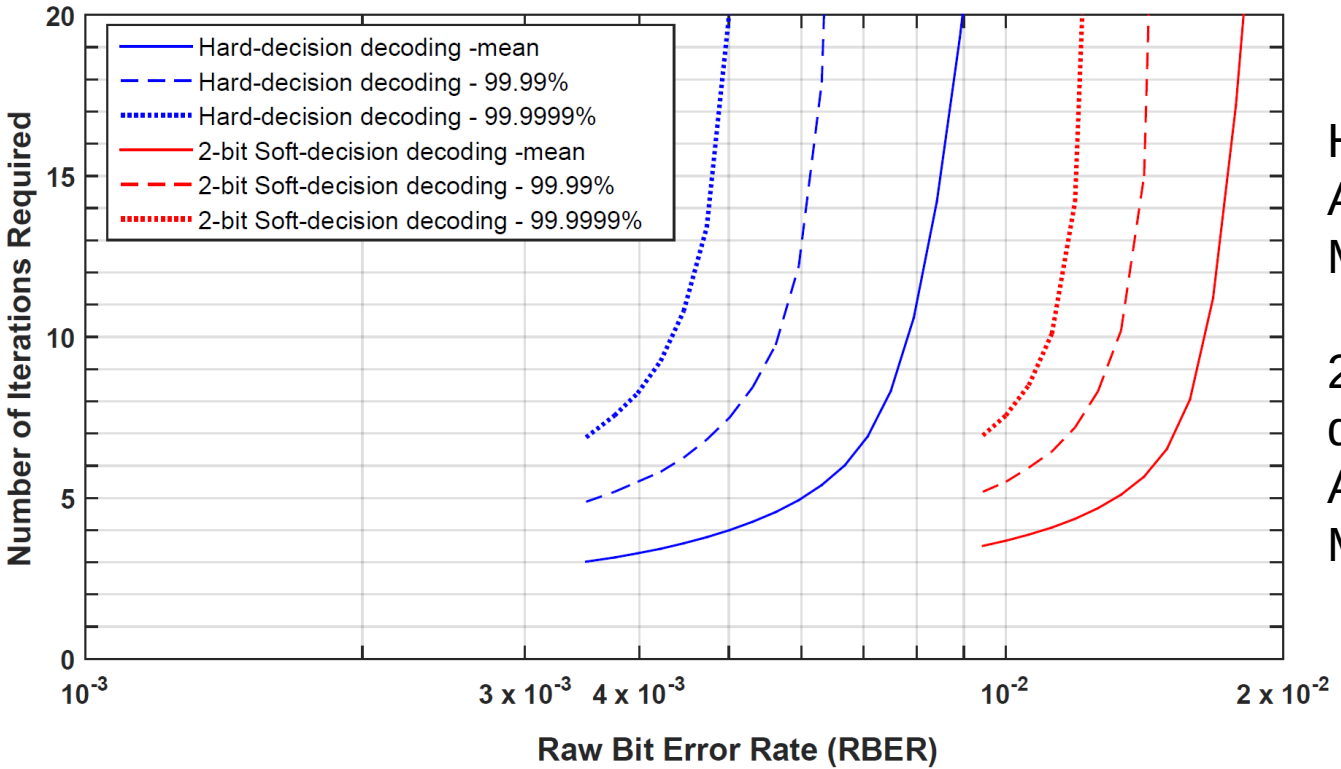
FER vs RBER Results: N=2KB, R=0.883



- No occurrence of error floor at FER of 1e-11.
- Achieves FER of 1e-11 at RBER of 1.26e-2 with 2-bit soft-decision (only 3 reads).

Results generated using multiple Xilinx Virtex-7 FPGA boards

Number of Iterations vs RBER: N=1KB, R=0.883



Hard-decision decoding:
At RBER of 3.5e-3
Mean no. iterations = 3.1

2-bit Soft-decision decoding:
At RBER of 1e-2
Mean no. iterations = 3.6

ASIC Synthesis Results – 1KB code, R=0.883

- UMC 40nm HLP (using only HVT cell)
- Clock frequency 400MHz

Latency per iteration	0.68 us
Throughput per iteration	1.45 GB/s
Total cell area (including memory)	0.54 mm^2
End-of-life Power (soft-decision decoding)	180 mw

Conclusions and Future Development

Conclusions

- Achieves low error floor performance for 1KB and 2KB
- Achieves FER of 1e-11 at RBER >1e-2 with only 2-bit soft information.
- Provides savings in power and chip area.

Future Development

- Additional hardware optimizations.
- Validation with data from NAND Flash samples.