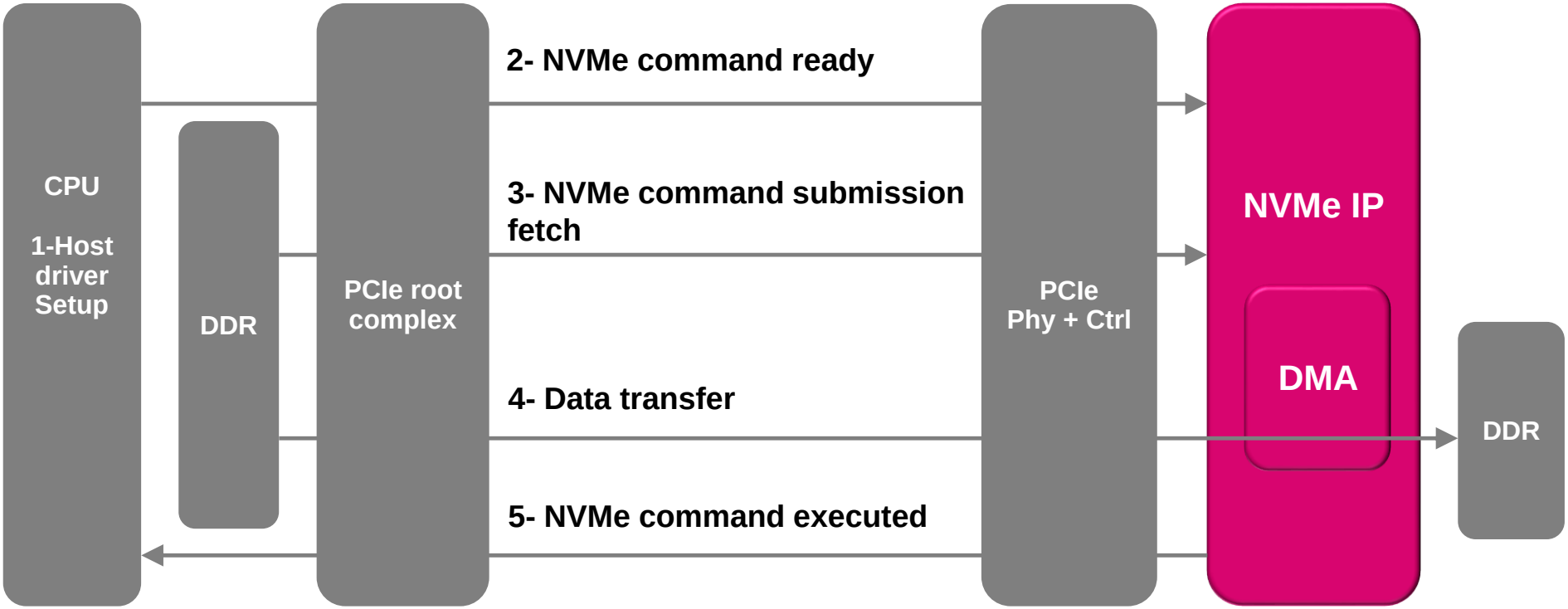
NVMe : Redefining the Hardware/Software Architecture

Jérôme Gaysse, IP-Maker

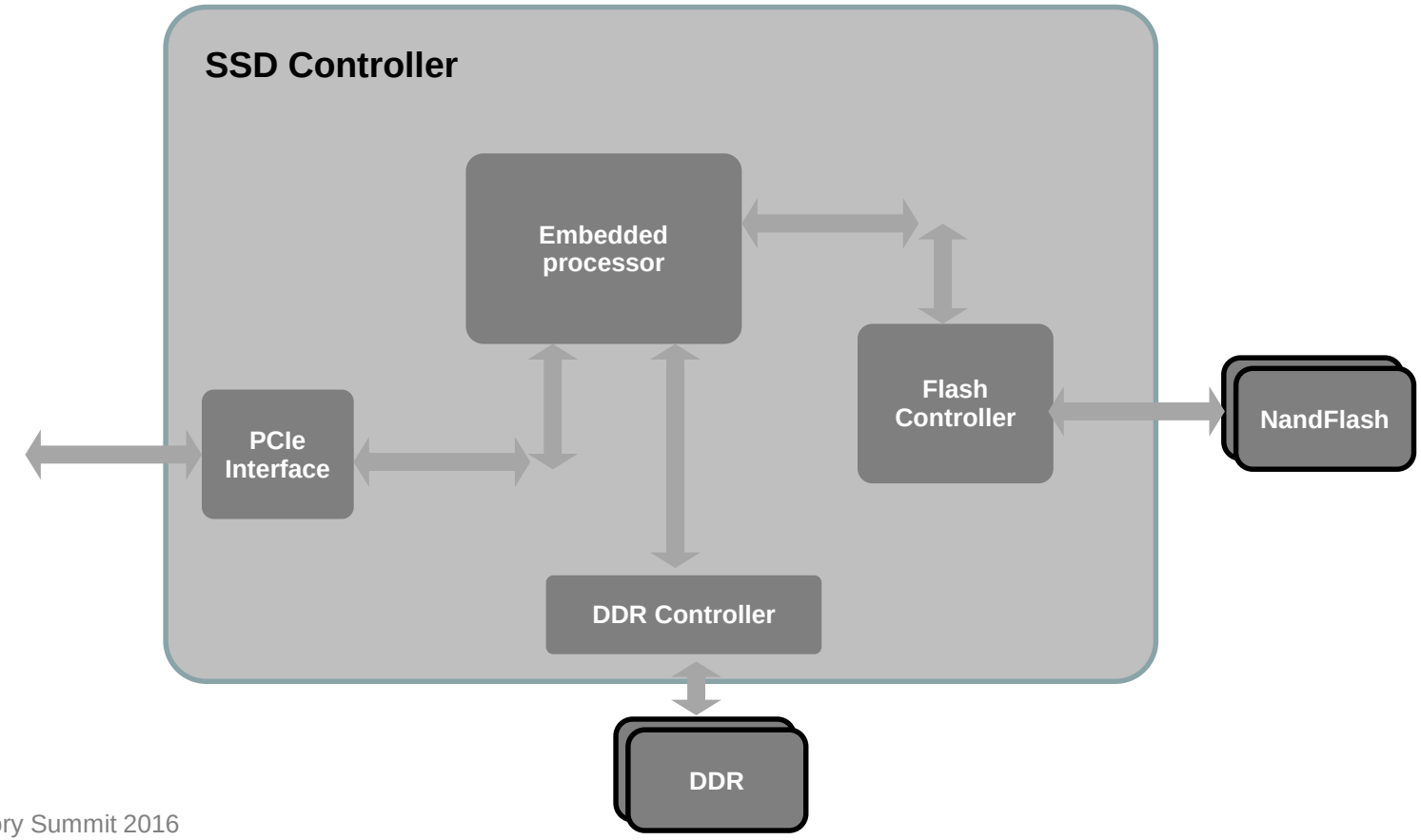
NVMe Protocol

- How to implement the NVMe protocol?
  - SW, HW/SW or HW?



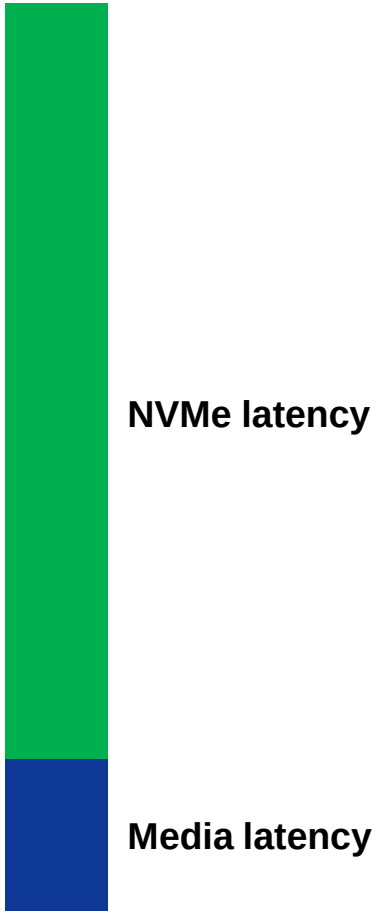
Software implementation

- Architecture



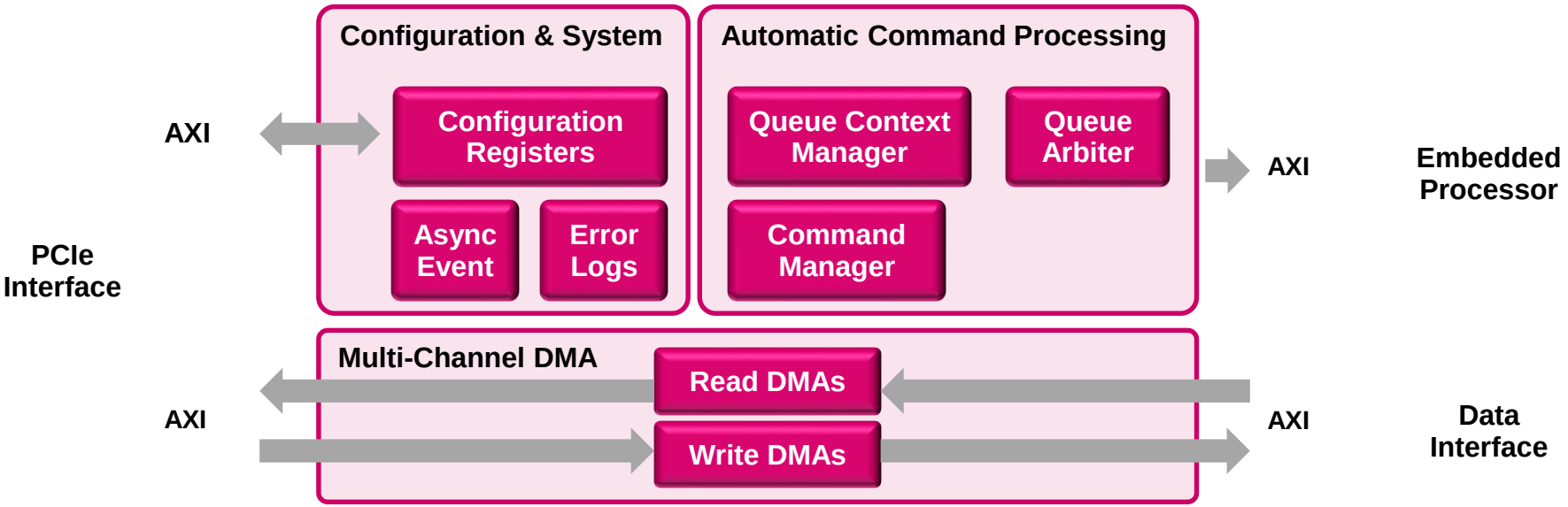
Software implementation

- Latency
  - CPU at 2GHz
  - 10,000 clock cycles per IO
  - **=> 5µs**
- Power
  - **=>60pJ/bit**



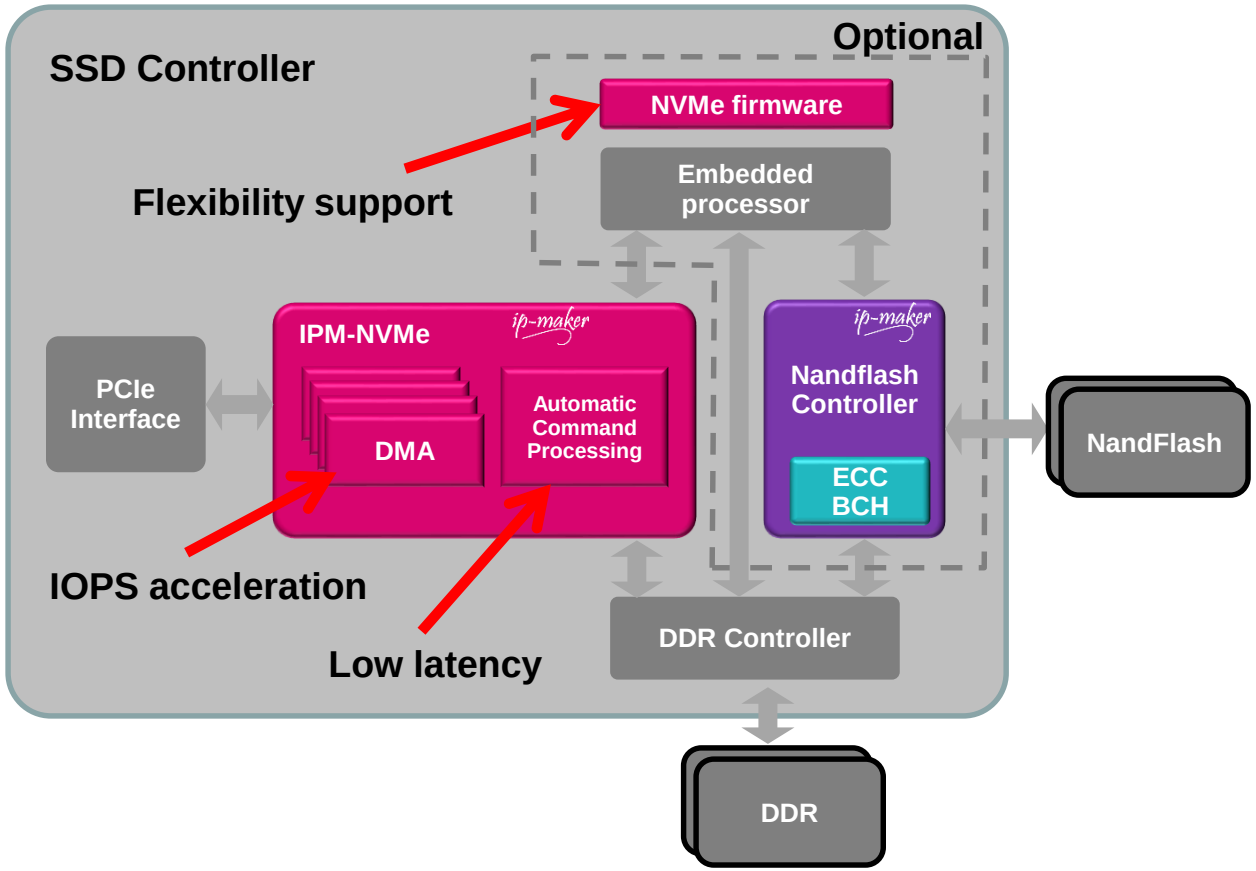
HW/SW NVMe IP architecture

- Automatic command processing => Low latency
- Multi-channel DMA => IOPS acceleration



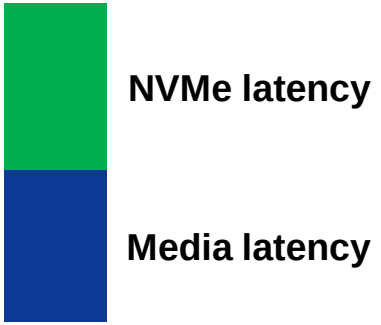
Hardware/Software implementation

- Architecture



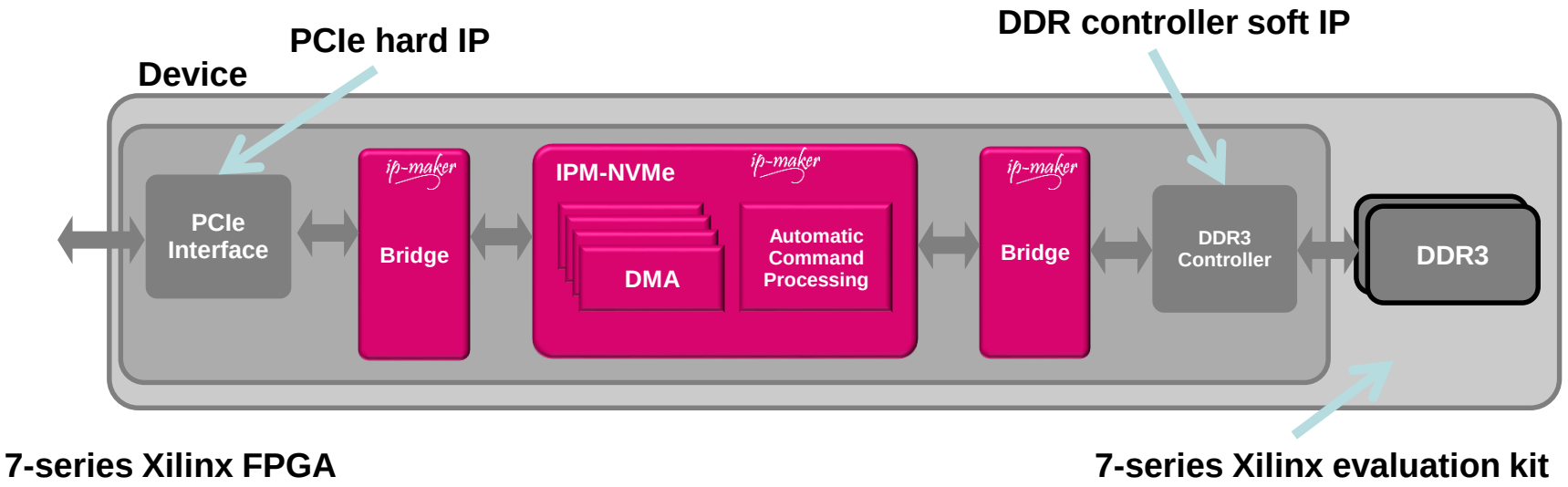
Hardware/Software implementation

- Latency
  - Digital Clock = 250MHz
  - 40 cycles
  - CPU at 2GHz
  - 2000 clock cycles per IO
  - **=> 1.1µs**
- Power
  - **=>15pJ/bit**



Hardware implementation

- Architecture



Hardware implementation

- Latency
  - FPGA Clock = 250MHz
  - 80 cycles
  - **=> 320ns**
- Power
  - **6pJ/bit**

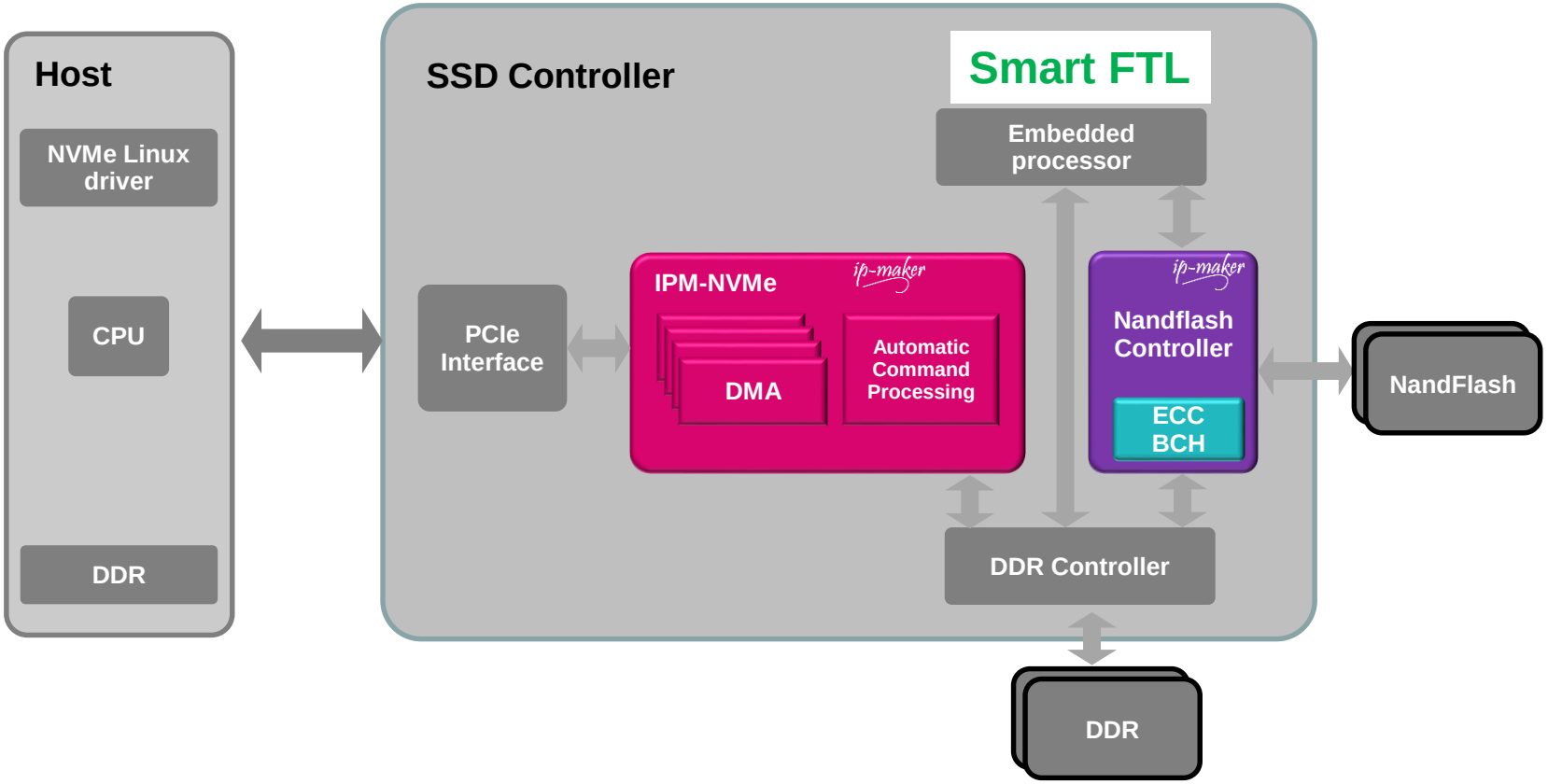
Implementation Summary

	SW	HW/SW	HW
Latency	**5µs**	**1.3µs**	**320ns**
Energy	**60pJ/bit**	**15pJ/bit**	**6pJ/bit**

- How to benefit from this improved latency and power consumption?
  - Adding features for the same power budget
    - Smart FTL
    - Protocole management for HBA…
  - Improve the overall system power efficiency

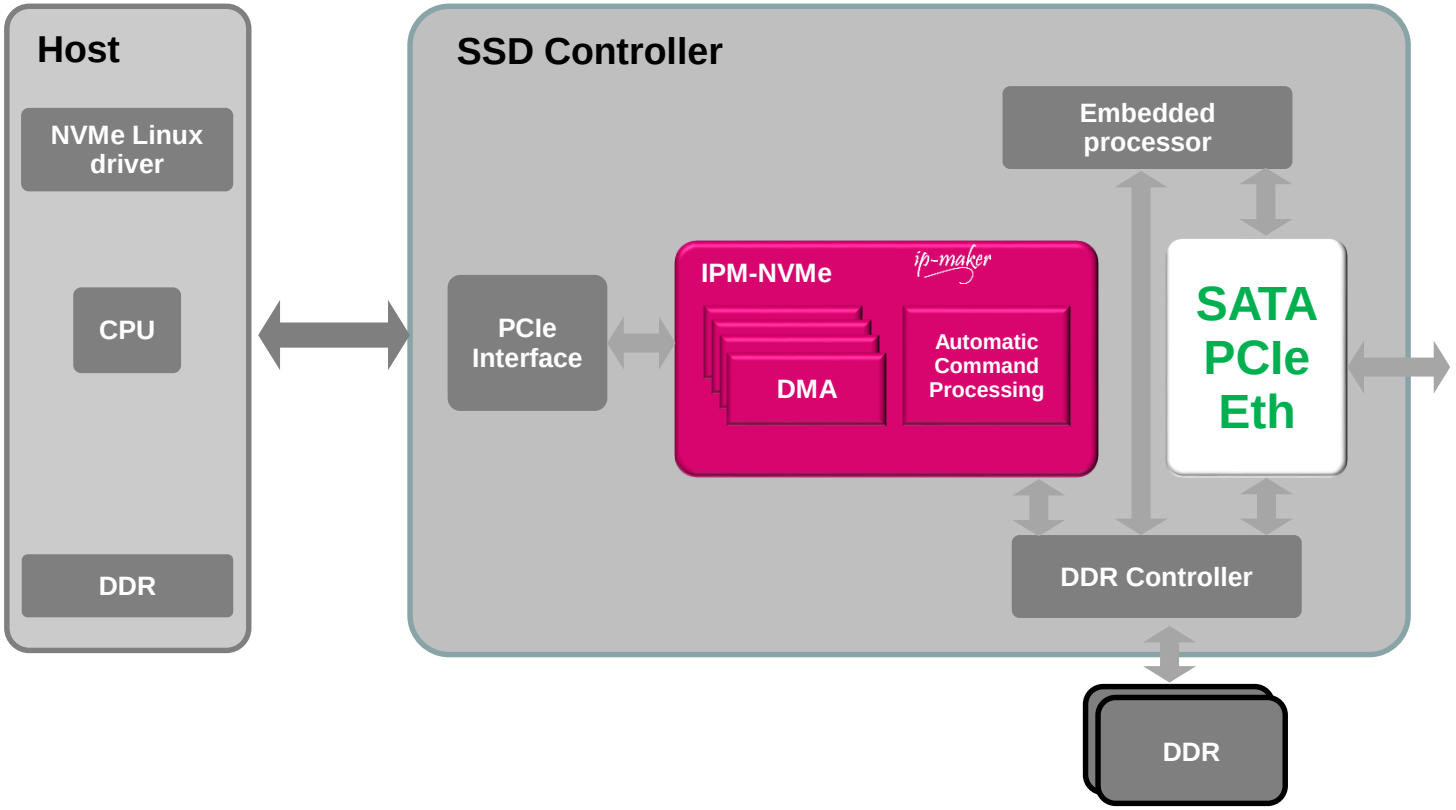
Hardware/Software implementation

- Application example : PCIe SSD



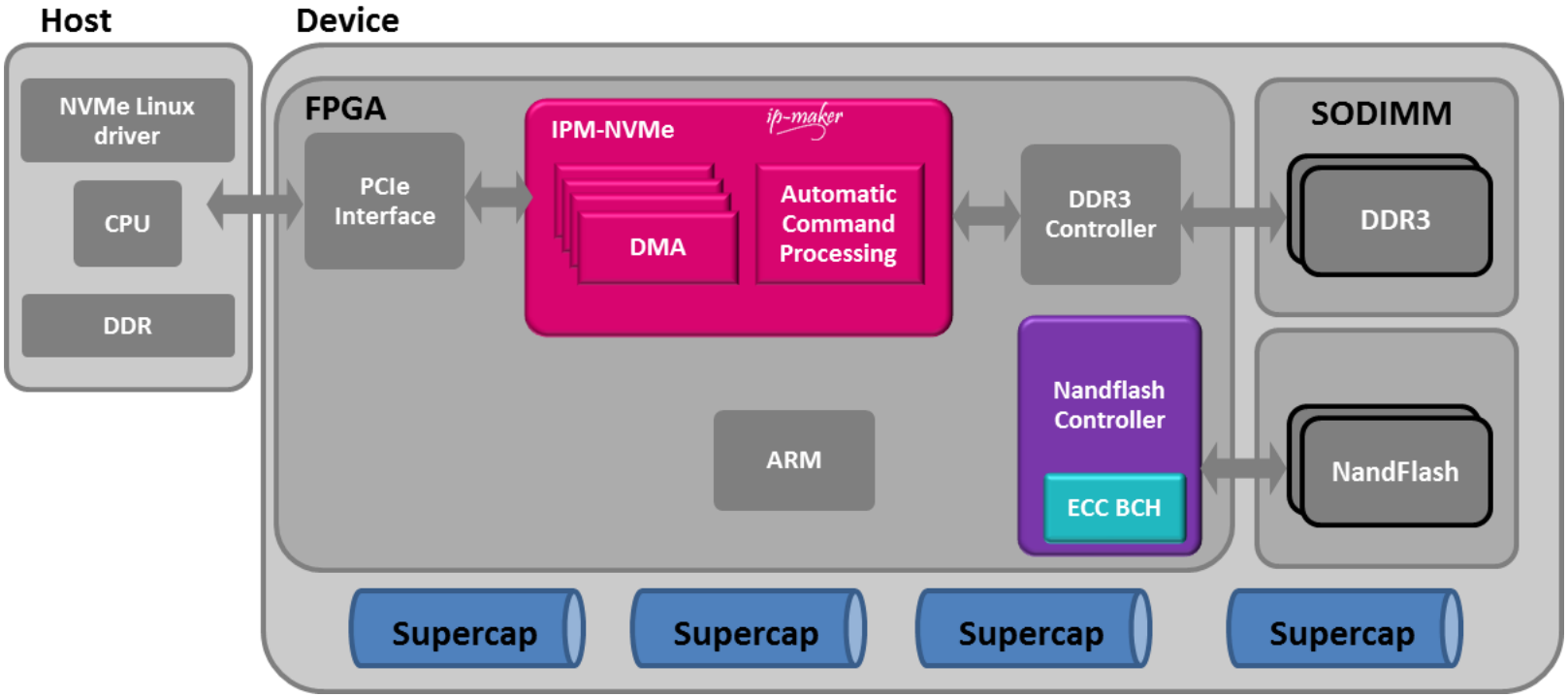
Hardware/Software implementation

- Application example : HBA



Hardware implementation

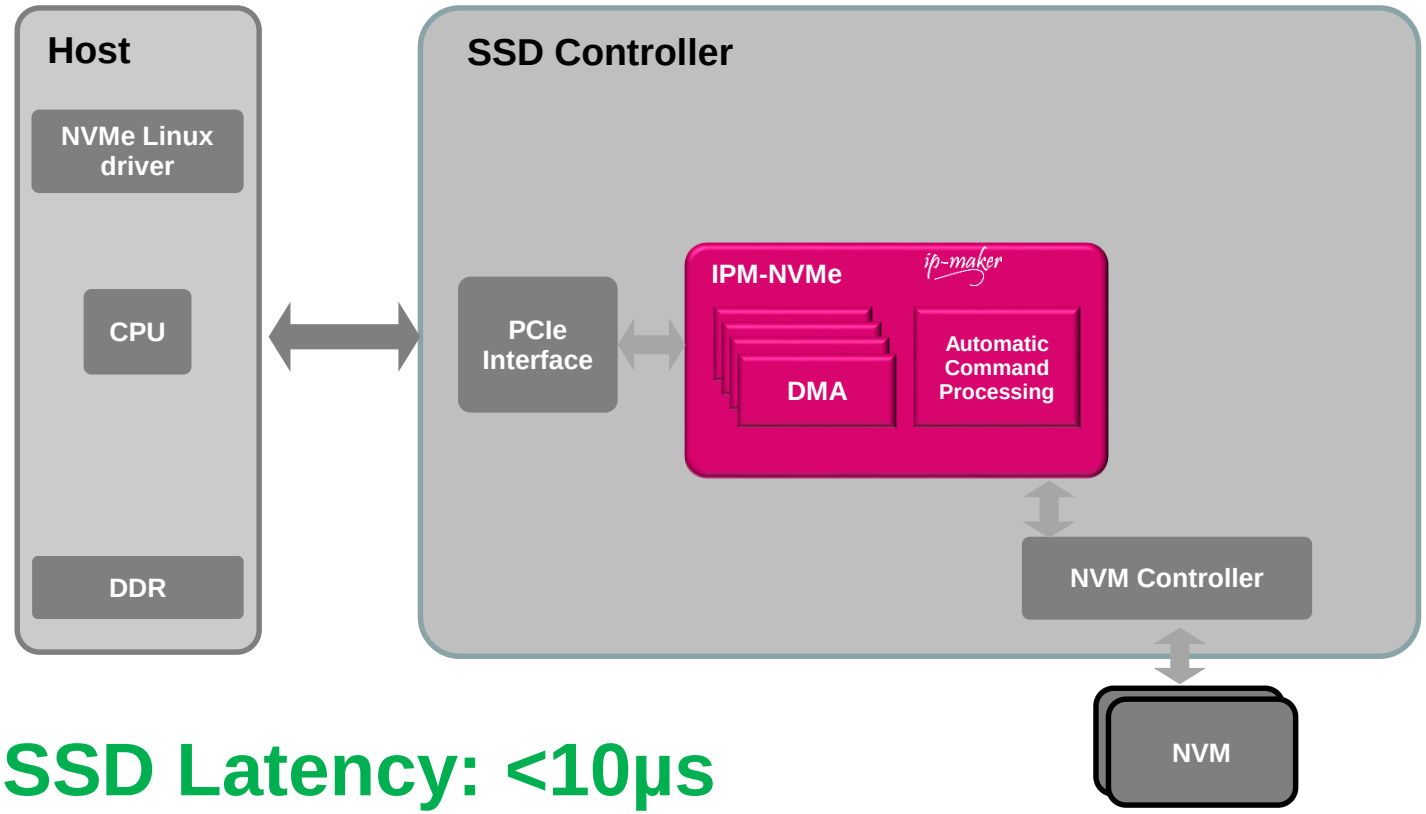
- Application example : NV-RAM Drive



- **Drive Latency: 5-7µs**

Hardware implementation

- Application example : SSD with NG-NVM



- **SSD Latency: <10µs**

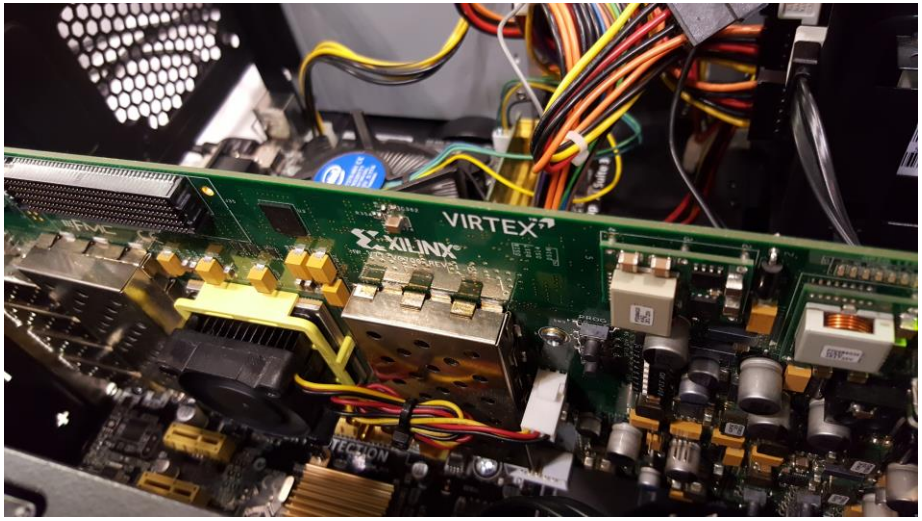
Conclusion

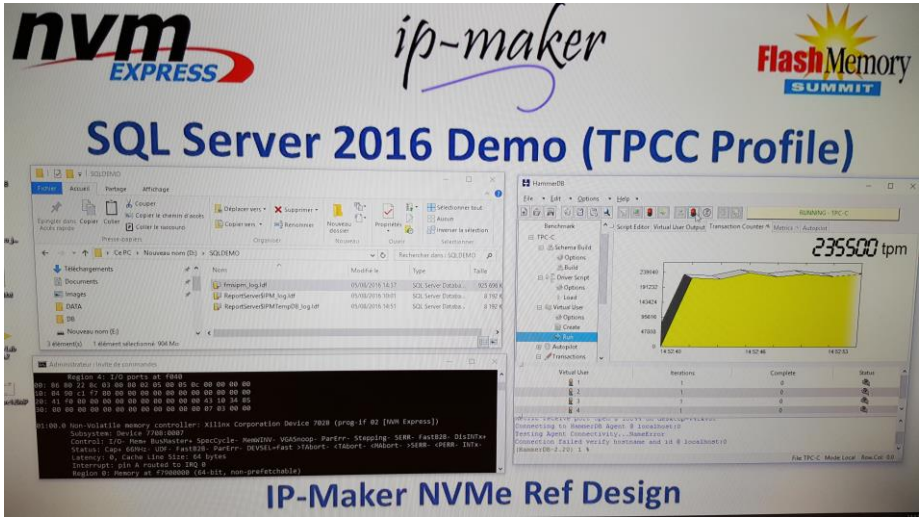
- Benefits of a software/hardware NVMe architecture
  - Excellent power/feature tradeoff
  - Allow new NVMe applications

- Benefits of a hardware NVMe architecture:
  - Less power and lower latency
  - Ready for NG-NVM

Thanks!

Visit IP-Maker booth #717
NVMe live demo!





jerome.gaysse@ip-maker.com
www.ip-maker.com