PCIe® NVMe® Extensions Part 1

Uma M. Parepalli

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Agenda

- Session Description
- Session Organization
- Individual Presentations
- Q&A at the end of each presentation

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Session Description

- PCIe SSDs offer higher performance than ones based on disk interfaces, since they utilize the high-speed (and widely supported) PCIe bus.
- They have quickly become popular in many enterprise applications, particularly in implementations utilizing the new NVMe standard.
- Of course, all the usual design problems occur ranging from connectors through power management, power consumption, configurability, and hardware/software tradeoffs.
- But with over 100 million enterprise PCIe ports already shipped, this is an approach enterprises find to be both reasonably priced and easily implemented. It can work in both client and data center applications.

Session Organization

- Uma Parepalli, SK hynix memory solutions
  - Session Chair & Organizer
- NVMe: Redefining the Hardware / Software Architecture
  - Jerome Gaysse, Business Development Manager, IP Maker
- High Performance FTL Architecture for PCIe NVMe SSDs
  - Ying Tai, Sr. Director, VIA Technologies
- Prioritization in the NVMe Block Layer
  - Jon Saunders, Applications Engineer, Microsemi
- Q&A

Uma Parepalli, SKHMS

- Session Chair / Organizer
- Uma M. Parepalli is a Firmware Architect at SK Hynix Memory Solutions. He is also SK Hynix's organizational representative for industry standards. Uma has over 25 years of experience and previously worked for EMC, LSI, Dell, Intel, and others in various capacities from Principal Engineer / Architect to Director and VP of Engineering. He is a Computer Engineering graduate of the University of Mysore, India.

Jerome Gaysse, IP Maker

- **NVMe: Redefining the Hardware/Software Architecture**
- Jerome Gaysse is an expert in emerging technologies for data center and works for IP-Maker on product and technology innovation. He successfully worked with startups to major companies including research institutes. He has strong knowledge in Memories, IP, FPGA and ASIC for the storage industry. Jerome has a masters degree from National Institute of Applied Sciences in Lyon, France with specialization in Semiconductors.
- **Presentation Abstract**: This session describes a way to implement the NVM Express management in a full hardware IP, therefore, offloading the embedded CPU: allowing to use more CPU bandwidth for higher FTL computing capabilities, or using smaller and slower CPU. This architecture provides low latency and low power features thanks to the hardware implementation, and still provides flexibility by using the embedded CPU for the FTL management and NVMe vendor specific commands. It also addresses use cases where NVMe can be used in other applications than PCIe SSDs with low latency and power consumption benefits, such as NVRAM drives, HBA and network interface cards.

Dr. Ying Tai, VIA Technologies

- Dr. Ying Tai joined VIA Technologies in 2015 as a Senior Director/Chief Architect, where he is leading the innovation effort in latest hardware and firmware architectures for NVM based storage systems. Prior to VIA Technologies, he was a Director in SanDisk Corporation, where he was in charge of the NAND Flash endurance related architecture development for enterprise SSDs. In his career, Dr. Tai has held several senior management and technical positions in the areas of data storage and communications at Cadence Design Systems, Boeing Satellite Systems, and Ikanos Communications.
- Dr. Tai received his Ph.D. degree in Electrical and Computer Engineering from University of California, Davis. He also earned his M.S and B.S. degrees from Stanford University and National Sun Yat-Sen University, respectively. He has published more than 30 peer-reviewed conference and journal papers, and has more than 30 granted or pending patents. In addition, Dr. Tai is a senior member of IEEE and a recipient of IEEE Communications Society Stephen O. Rice Prize.

Jon Saunders, Microsemi

- Prioritization in the NVMe Block Layer
- Jon Saunders is an Applications Engineer, Technical Lead at Microsemi in the Performance Storage Business Unit.
- His current responsibilities include Microsemi Flashtec™ NVRAM drive products. Jon previously supported the Microsemi Flashtec™ NVMe Controllers.
- Prior to his work at Microsemi, Jon spent the majority of his career at Hewlett Packard in various roles within the laser printer business.