Client PCIe/NVMe SSD with 3D NAND

Rick Huang

SSD Product Marketing

SiliconMotion Inc.

Client PCIe SSD

Client PCIe SSD Challenges

Power Consumption

Host Compatibility

3D NAND Support

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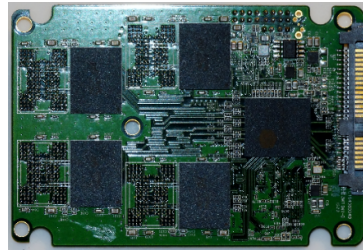# **Why Power Consumption Critical**
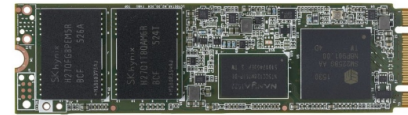
Lower power to extend battery life

Smaller form factor limits thermal dissipation

Add-In Card   **U.2**   **M.2**   **BGA**

NVMe/PCIe Power States

NVMe Power State	PCIe Link State	Active / Idle	Power	Exit Latency
PS0	L0 / L0s / L1	Active	100%	No
PS1	L0 / L0s / L1	Active	75%	Very Short
PS2	L0 / L0s / L1	Active	40%	Very Short
PS3	L1 / L1.1 / L1.2	Idle	Low	Moderate
PS4	L1.2	Idle	Extreme Low	Long

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Thermal Throttling

Slow down Clock to run slower

Cool down ASAP, then recovery to high speed

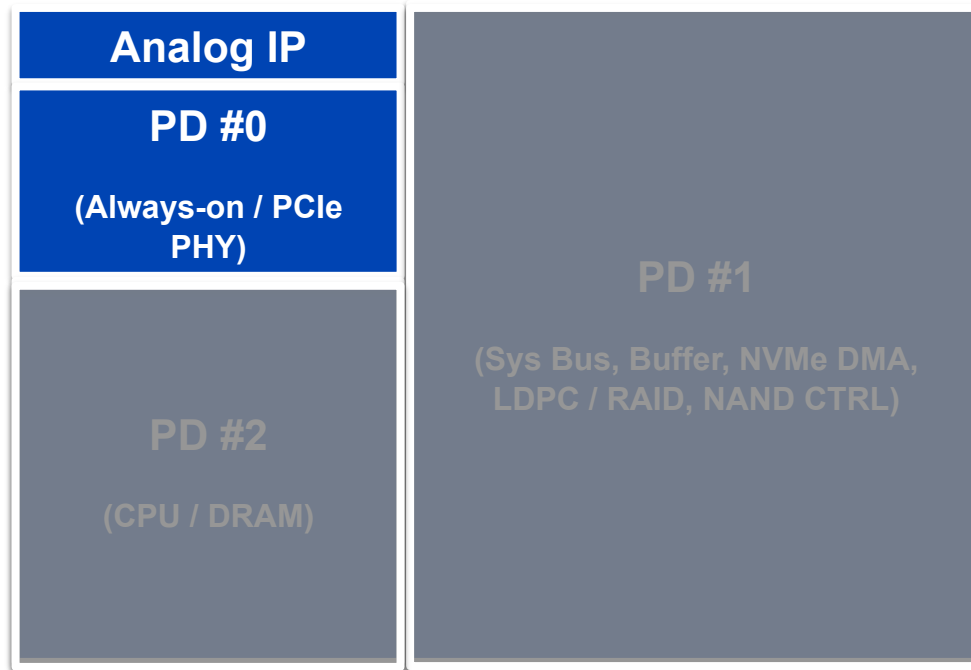

Drive temperature

Write speed

Thermal state

Power Domain Design

Analog IP	PD #1
PD #0 (Always-on / PCIe PHY)	(Sys Bus, Buffer, NVMe DMA, LDPC / RAID, NAND CTRL)
PD #2 (CPU / DRAM)	

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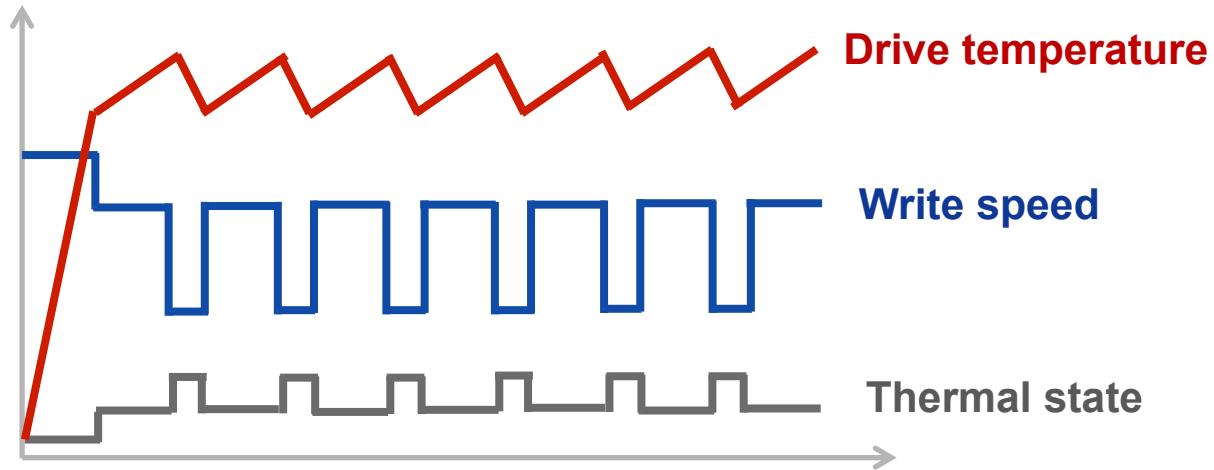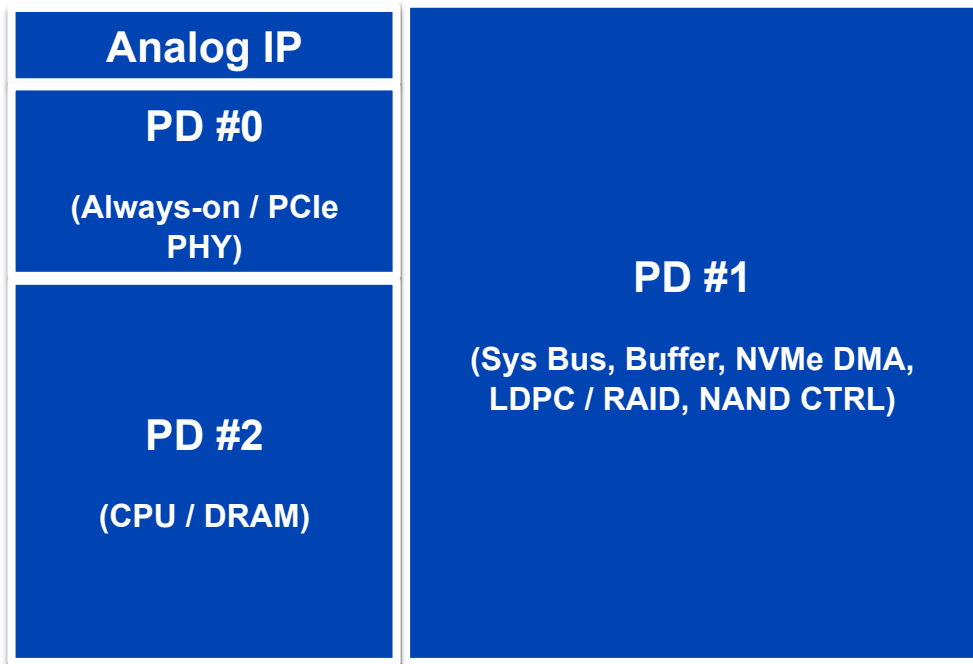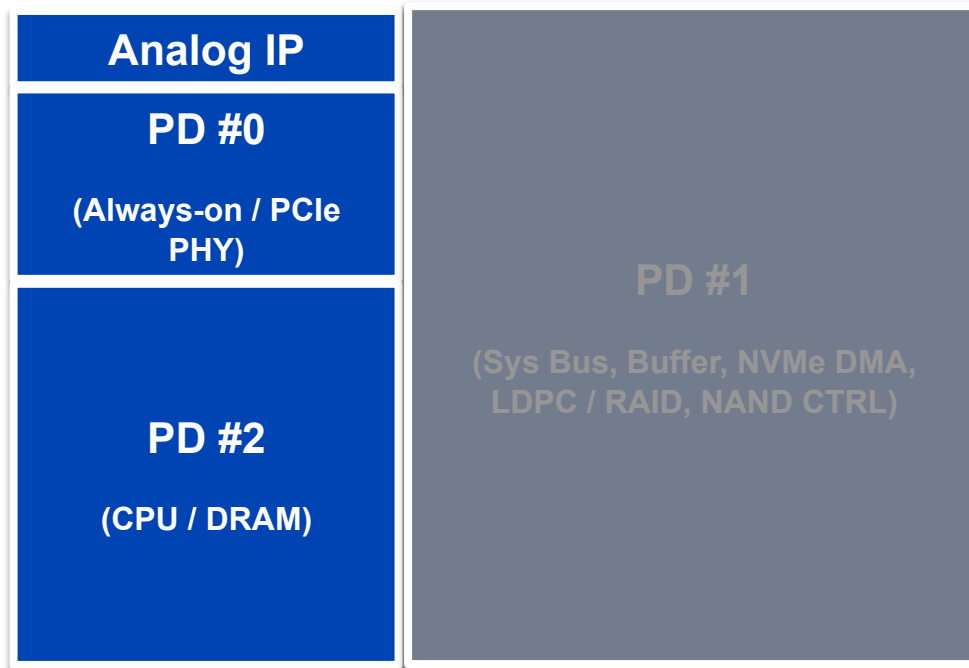
Power down modules only used in active mode

Power Domain Design

Analog IP

PD #0

(Always-on / PCIe PHY)

PD #2

(CPU / DRAM)

PD #1

(Sys Bus, Buffer, NVMe DMA, LDPC / RAID, NAND CTRL)

Power down modules only used in active mode

Put CPU to sleep and DRAM in refresh

Power Domain Design

AIP and always-on to ensure fast resume
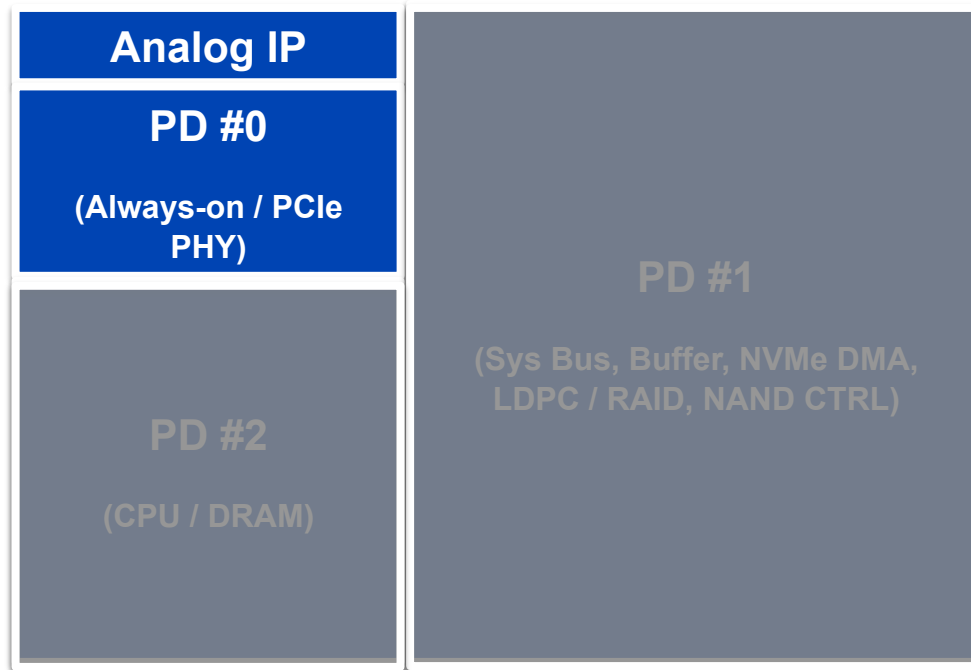
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3D NAND Support

Compatibility Issue…

Same language, but can't communicate

Compliance and Interoperability

Compliance test to verify the design capability

- Electrical Testing
- Configuration Space Testing (CV Test)
- Link and Transaction Protocol Testing (PTC Test)

Interoperability test to ensure compatibility

- PCI-SIG IOT and NVMe Plugfest

Why Compatibility Especially Important in PCIe/NVMe

- Built-in SSD in desktops/laptops

  - Qualified by PC makers on selected platforms

- Retail SSD for replacement/upgrade

  - Qualified by SSD makers on many platforms

L0 Standby (L0s)

Entry: Detection of defined number of EIOS

Exit: Detection of negotiated number of FTS

Not only robust design, but "adapt to the other"

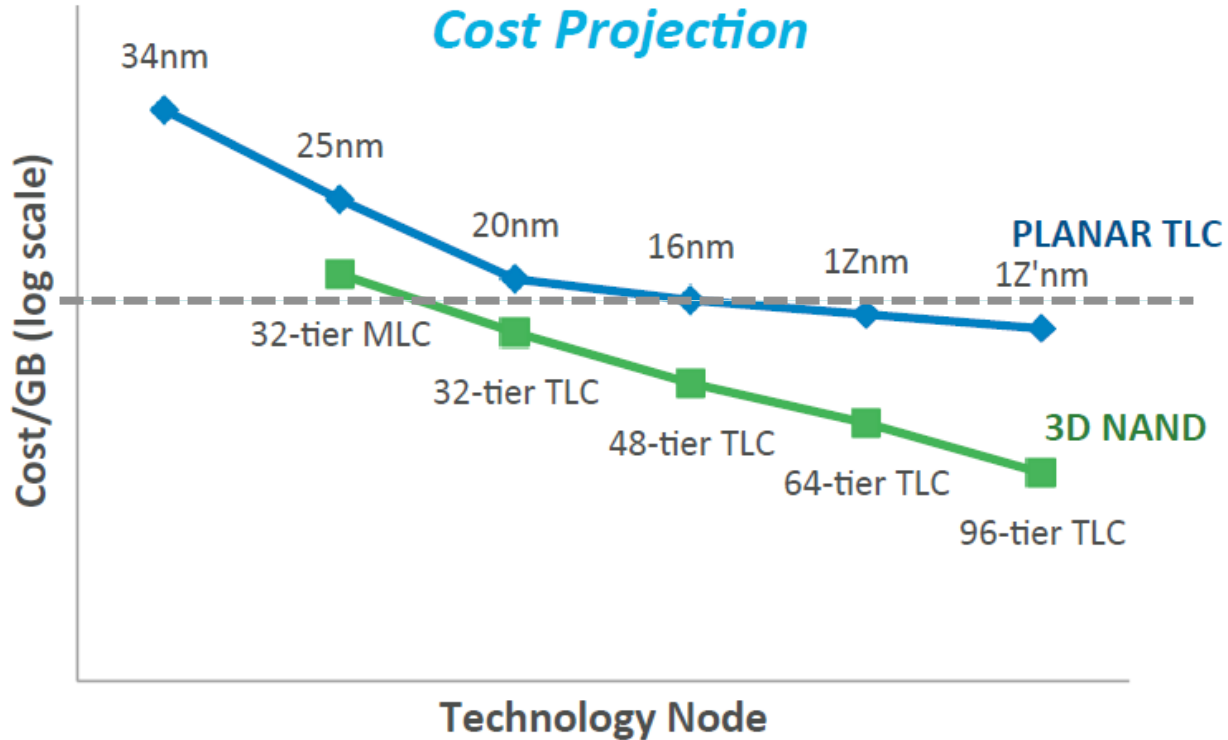No shortcut, just time and resource

The more experienced, the more capable

Client PCIe SSD Challenges
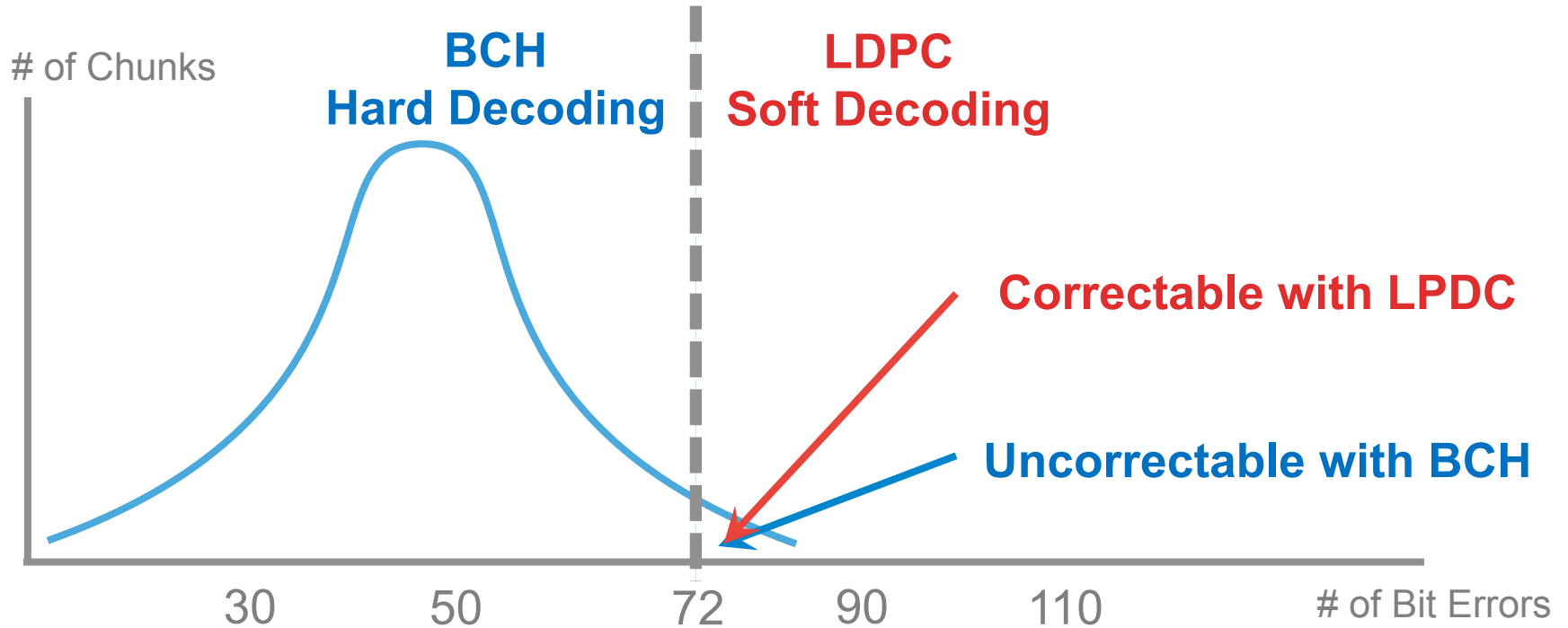
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Lower Cost 3D NAND

* Micron 2015 Winter Analyst Conference

LDPC – Higher Correction Capability

BCH
Hard Decoding

LDPC
Soft Decoding

# of Chunks

Correctable with LPDC

Uncorrectable with BCH

30   50   72   90   110   # of Bit Errors

Flexible RAID Design in ASIC/FW

RAID parity for 2nd dimension protection

Parity overhead of concern

Flexibility in ASIC and FW

Different schemes as needed for different NAND

To keep low parity overhead to retain user capacity
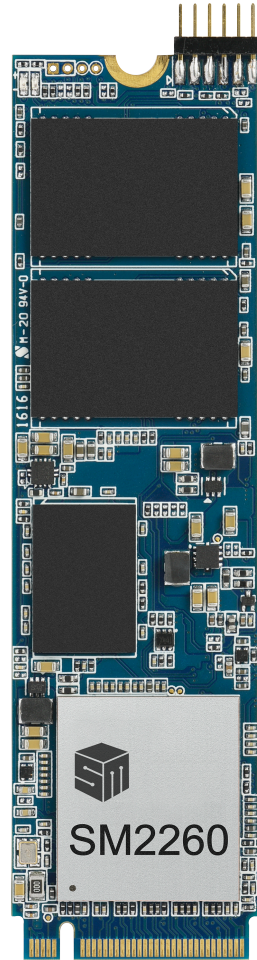
A Client PCIe SSD

Low Power

Compatibility

3D NAND

SMI

Booth

#413

PCIe Gen3 x4

NVMe 1.2

Support 3D NAND

Seq. Read 2.4GB/s

Seq. Write 1.1GB/s

PS4 <5mW

Thank You!