SEAGATE

Pre-Conference Seminar H: Designing SSD Controllers

Organizer/Chairperson:

Erich F. Haratsch

Seagate

Agenda

Title	Speaker	Duration (mins)
Introduction	Erich Haratsch	5
NAND Flash Basics & Error Characteristics	Roman Pletka	40
NAND Flash Media Management Algorithms	Erich Haratsch	40
LDPC Error Correction for NAND Flash	Osso Vahabzadeh	45
Break		10
ASIC/Merchant Chip-Based Flash Controllers	Jeff Yang	45
FPGAs in Flash Controller Applications	David McIntyre	45
Panel Discussion	All	10

Thank You! Questions?

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