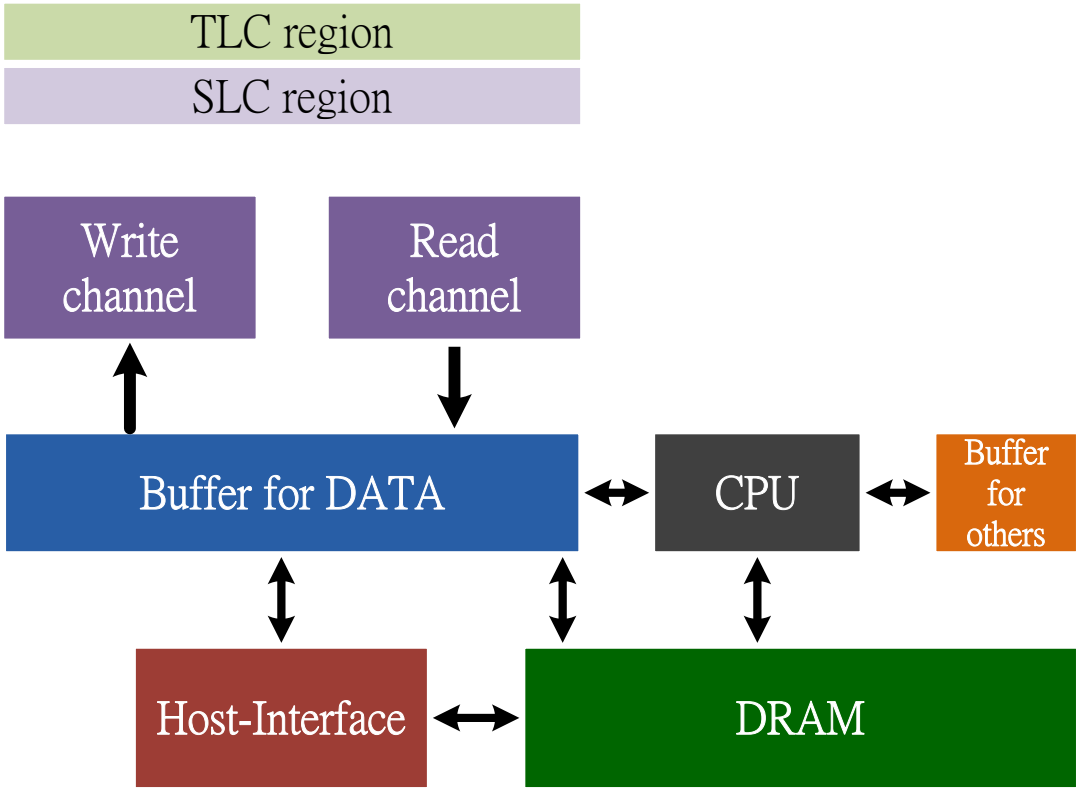
ASIC/Merchant Silicon Chip-Based Flash Controllers

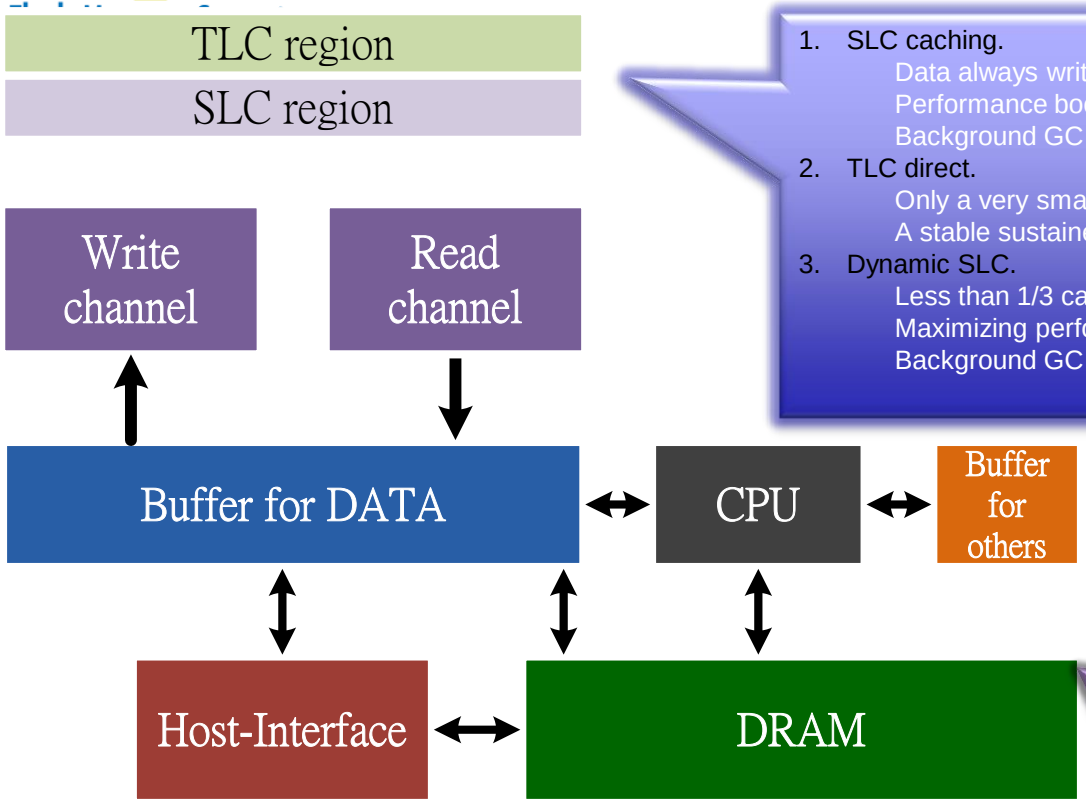
Jeff Yang

Silicon Motion

Basic architecture



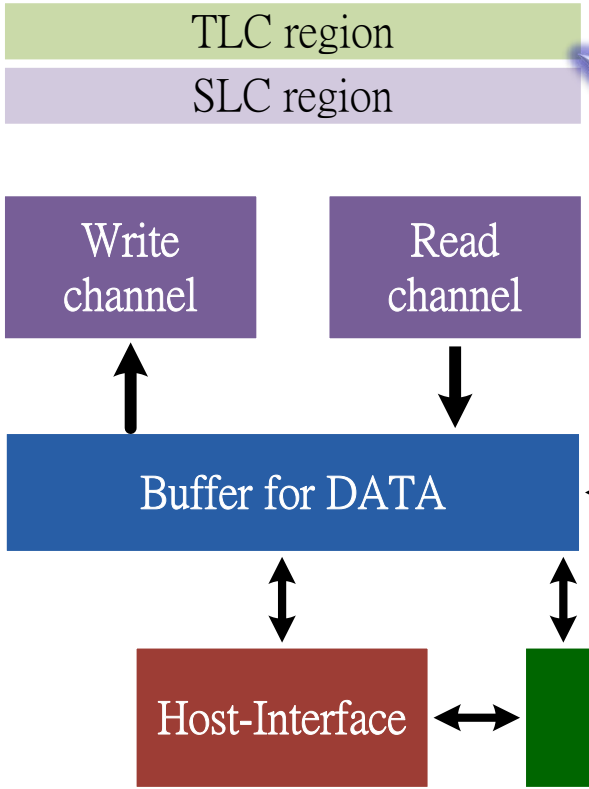
Application combinations on TLC/QLC



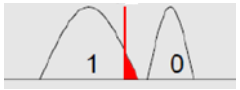
1. SLC caching.
   - Data always write into SLC. A Fixed portion of SLC regard as a cache buffer.
   - Performance boost on SLC caching.
   - Background GC to TLC block.
2. TLC direct.
   - Only a very small portion for system usage and small random write data.
   - A stable sustained write performance.
3. Dynamic SLC.
   - Less than 1/3 capacity threshold, using SLC.
   - Maximizing performance boosting period.
   - Background GC to TLC block.

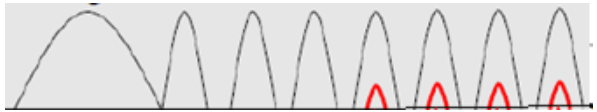
1. Full size DRAM
   - For host data write caching. Full lookup table.
2. Non-DRAM
   - Extremely low cost.
   - Optimize for user experience.
   - More system info access from SLC blocks.
3. Small DRAM.
   - Full lookup table on external buffer
   - No host data buffer.

Different TLC reliability issue



1. 3D.
   - One-pass program, two-pass program, multi-pass program.
2. Program failure protection flow.
   - Program failure range.
   - Read back data from flash cache buffer.
   - DRAM back up. SLC back up, SRAM backup.
3. One WL open and Multi-WL short.
   - Need raid or read back check after program.
4. TLC/SLC dynamic changing usage.
   - TLC endurance calculation issue.
5. Internal copy back for SLC to TLC
   - Internal read without ECC correction





Challenge: Support all combinations and cost efficiency

3D

- One-pass
- Two-pass
- Multi-pass

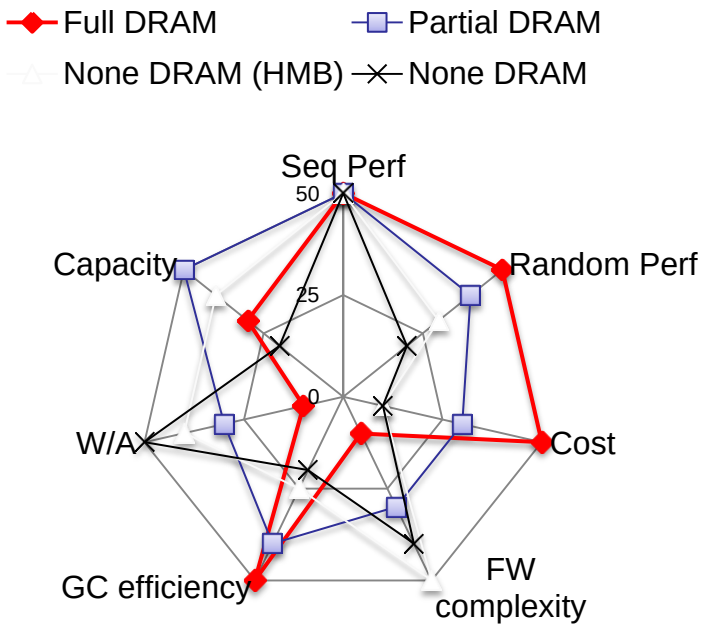
SLC usage

- SLC caching
- TLC direct
- SLC/TLC dynamic

External buffer

- Full DRAM
- Non-DRAM
- Partial DRAM

SMI Product comparison



Full DRAM

Pros
- High Perf
- GC efficiency
- Low W/A
- Low complexity

Cons
- Capacity limitation (2TB)
- DRAM bandwidth limitation
- Power consumption
- Cost

Partial DRAM

Pros
- GC efficiency
- Capacity limited by L2P address bit (8TB)

Cons
- Med Random Perf (DRAM L2P buffer)
- Med W/A

None DRAM

Pros
- Cost
- Perf still good for CDM

Cons
- High W/A
- Low Random Perf (SRAM L2P buffer)
- Program Failure
- High capacity support

None DRAM (HMB)

Pros
- Cost
- Random perf

Cons
- Same as “None DRAM”
- More complex than “None DRAM”

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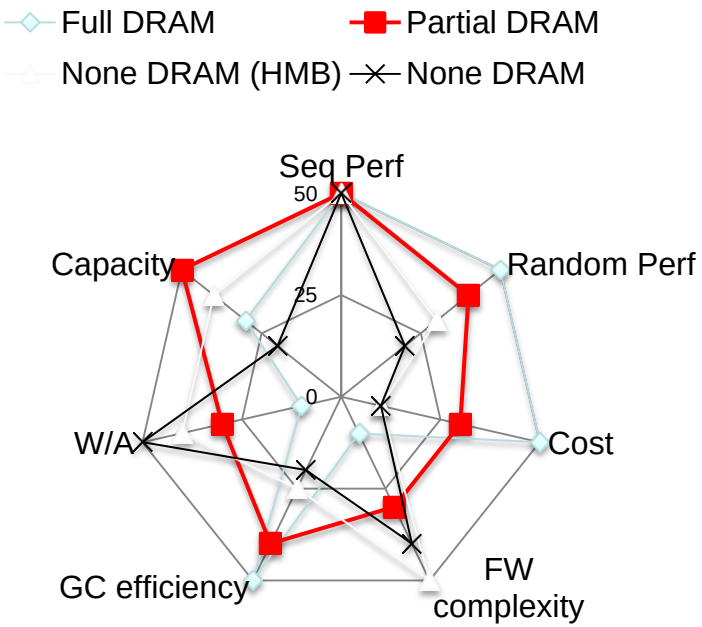

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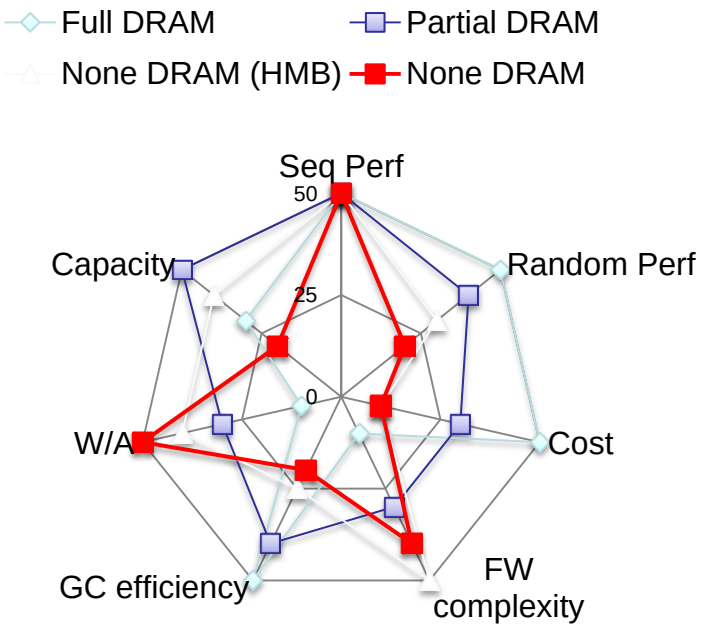

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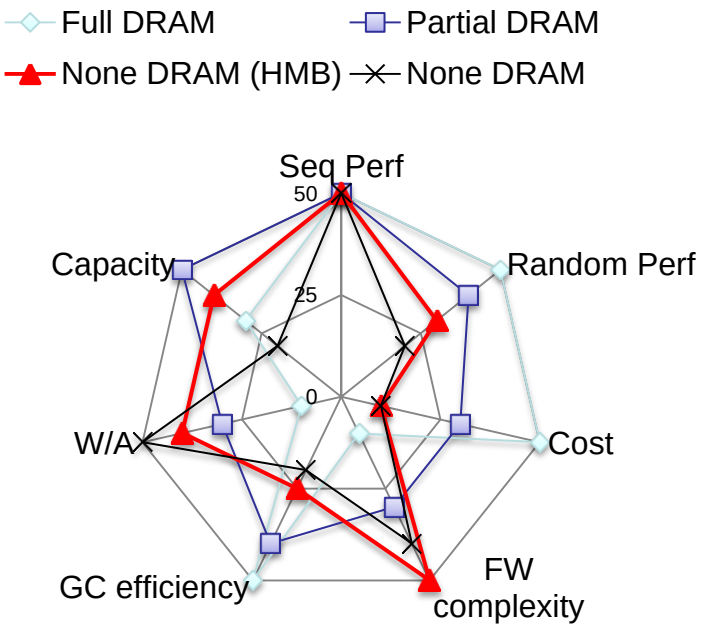

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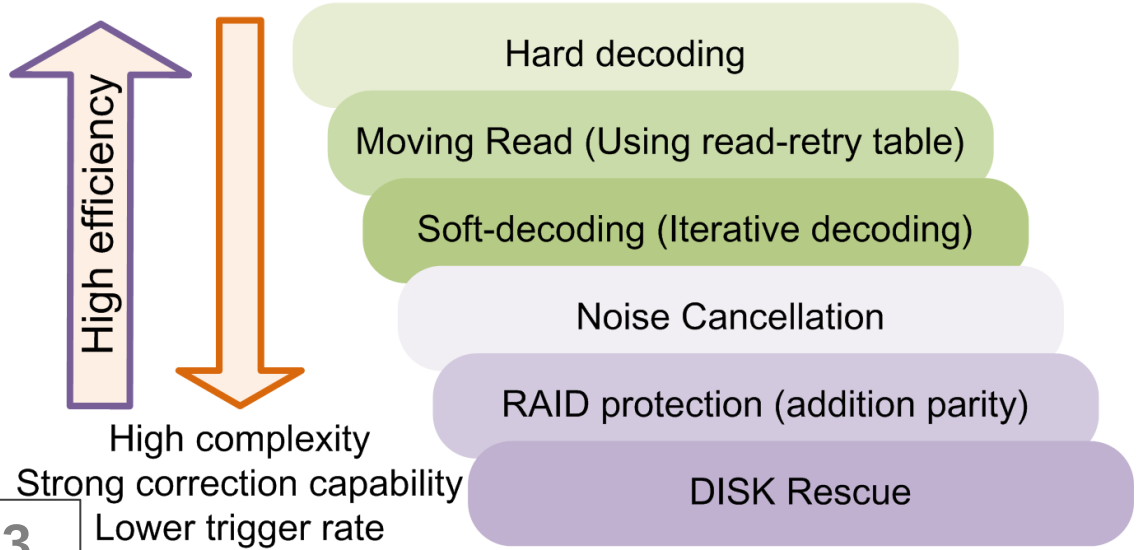
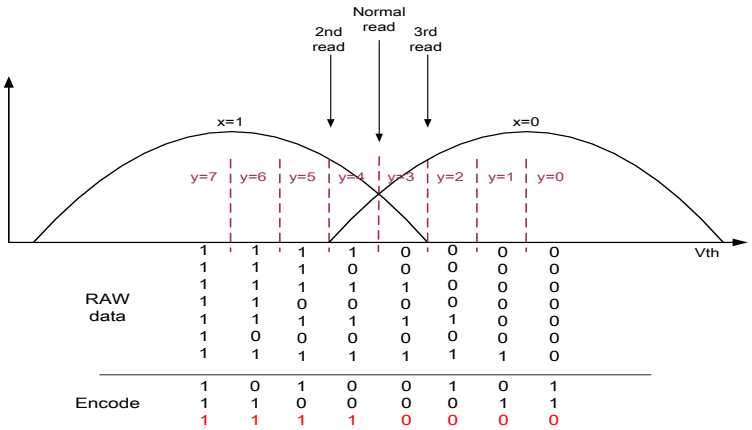
Traditional Error recovery flow

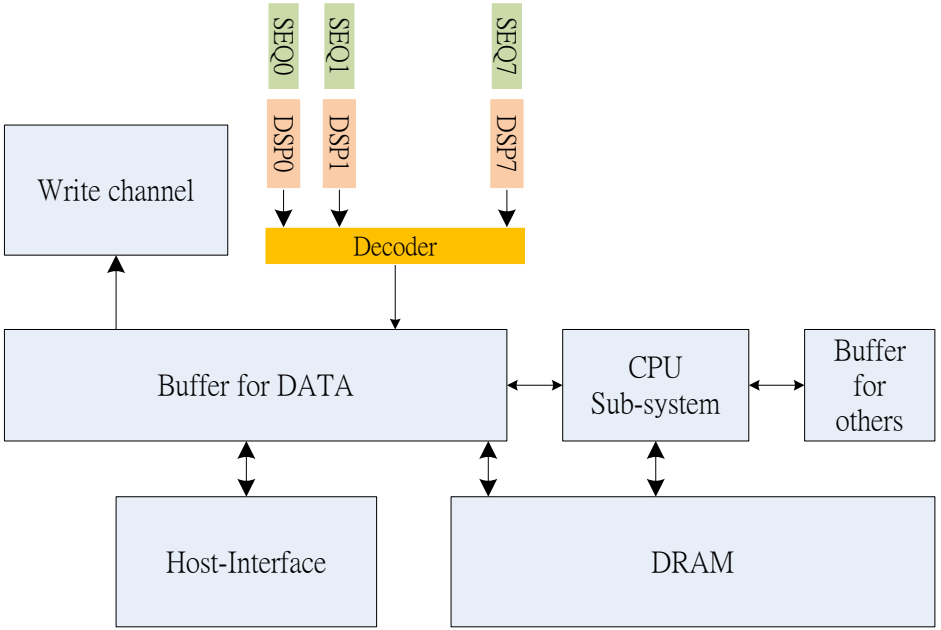
Error recovery flow



Flash Memory Summit 2013
Santa Clara, CA

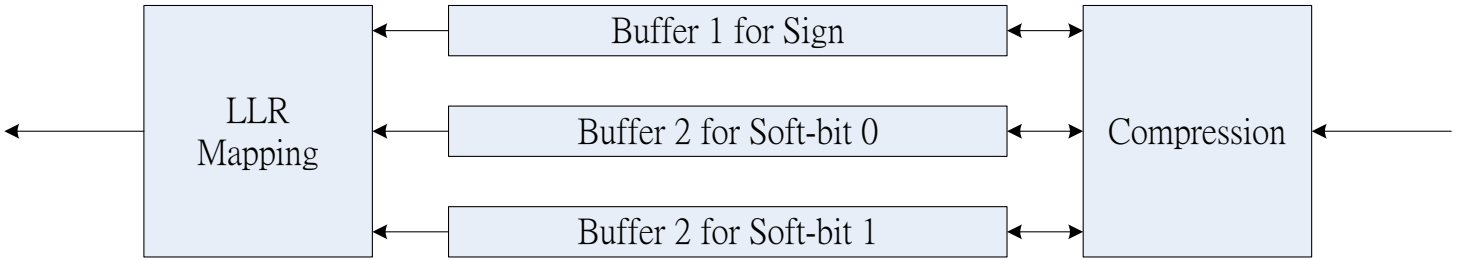
Soft-information interface





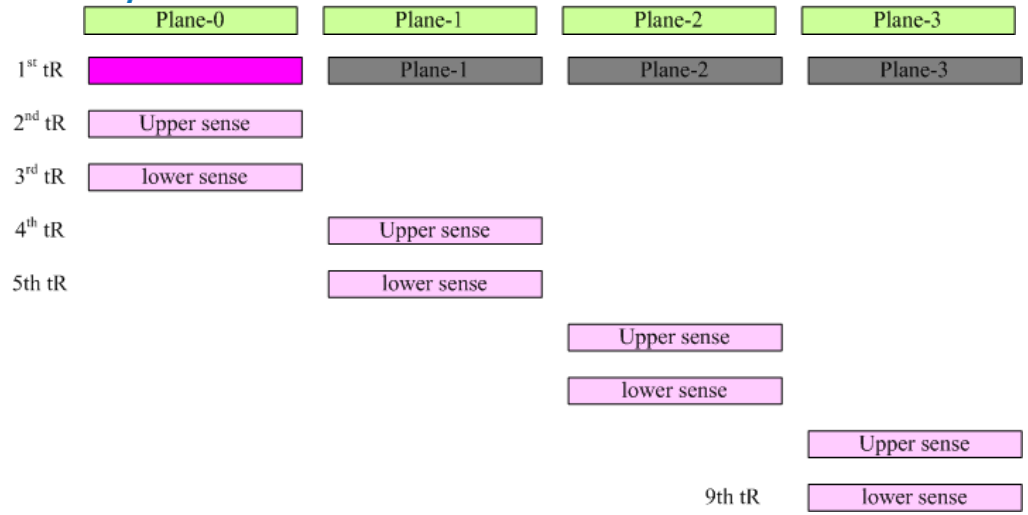
- In order to provide better decoder's correction capability, using the soft-info to get more reliability bits.
- NAND interface support .
  - Traditional read/retry interface.
  - Direct soft-info interface.

DSP engine's buffer size



- The buffer size is the capability to contain the number of chunks soft-bit.
- Access addition soft-info from NAND may need additional read busy time.
- Read the soft-bit under the same busy time will have higher efficiency, but buffer size requirement is huge.

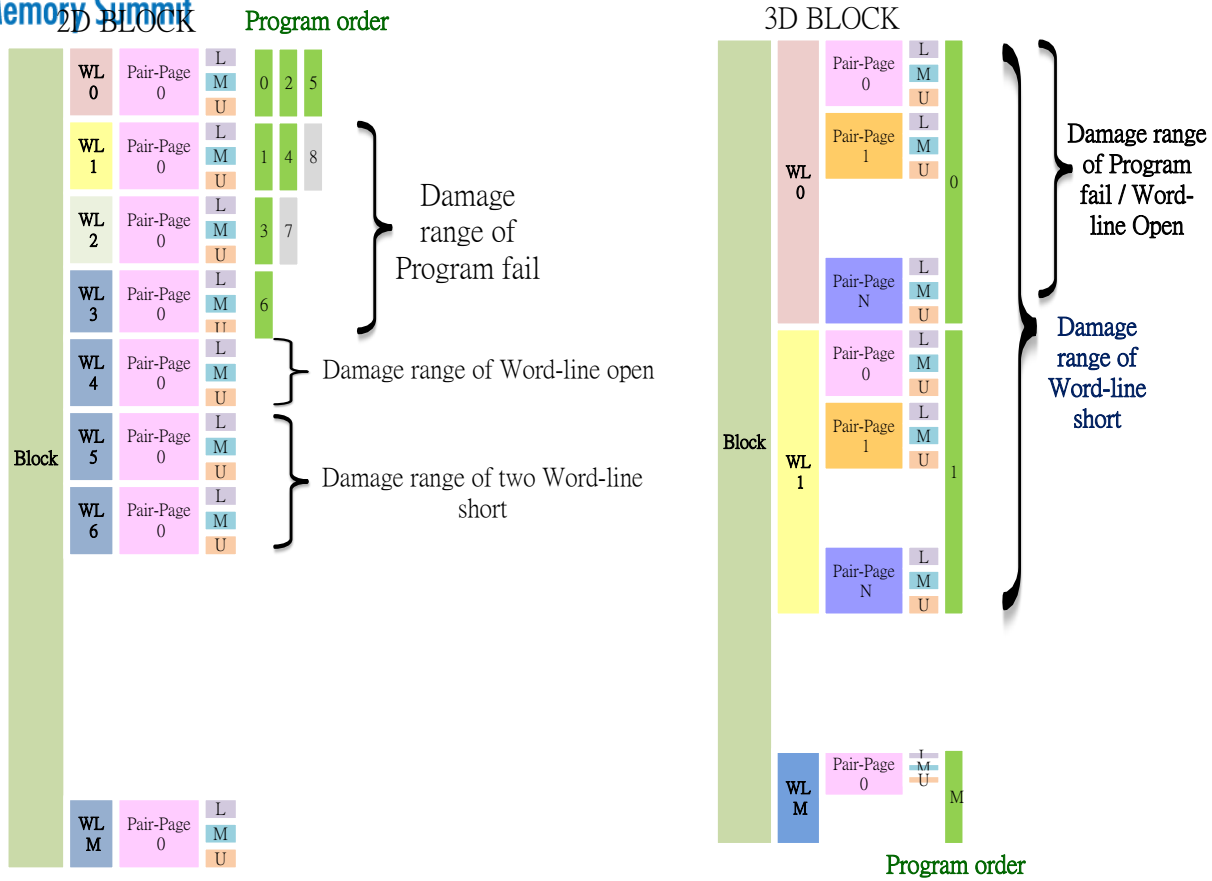
Soft-decoding throughput limitation



- One Transfer time = 2.5ns/1B x 18432B = 46us (400MTs)
- Assume DSP-buffer size 16KB.
  - 9 tR time + 12 transfer-time = 9x(100us) + 12 x (46us) = 1452us
  - Throughput = 64KB/1452us = 44MB/sec
- Assume DSP-buffer size 64KB.
  - 3tR time + 12 transfer-time = 3x(100us) + 8 x(46us) = 668us.
  - Throughput = 64KB/668us = 95MB/sec

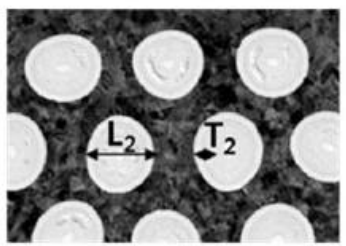
In Client SSD applications,
Soft-decoding will regard as the ERROR-Recovery flow.
We will not ask the throughput under recovery mode.
But we will take care the recovery mode trigger rate.

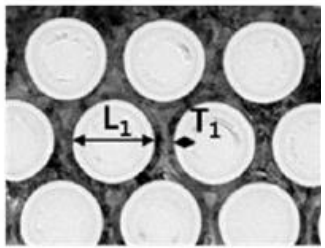
Failure range from 2D to 3D.



3D NAND Challenges

- Each 3D generation will increase the layer number by 30~50%.
- High-aspect ratio channel hole etch.
- Cell current reduction is seriously concerned.
- Reduce the read-voltage to improve the read-count (degradation the read-disturbance) make cell current worse.
- Different cell characteristics for each WL. (program-speed, cell-to-cell interference, retention)
- Poor retention characteristics.



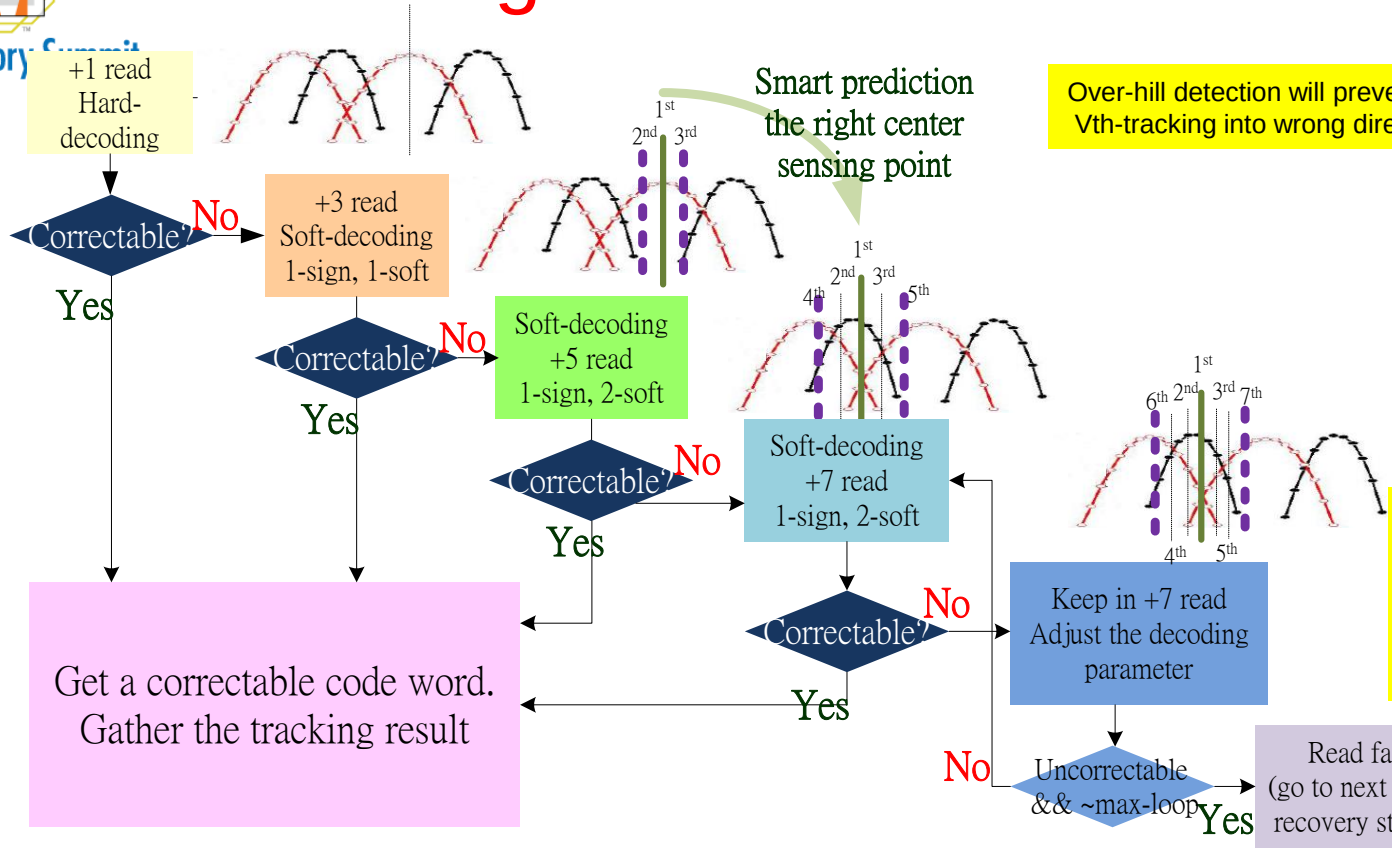


Not easy to screen out some defects.

Especially on bit-column related defect.

Ref: Evolution of NAND flash memory: from 2D to 3D… 2017 IMW

DSP algorithm for the Vth-tracking



Over-hill detection will prevent the Vth-tracking into wrong direction.

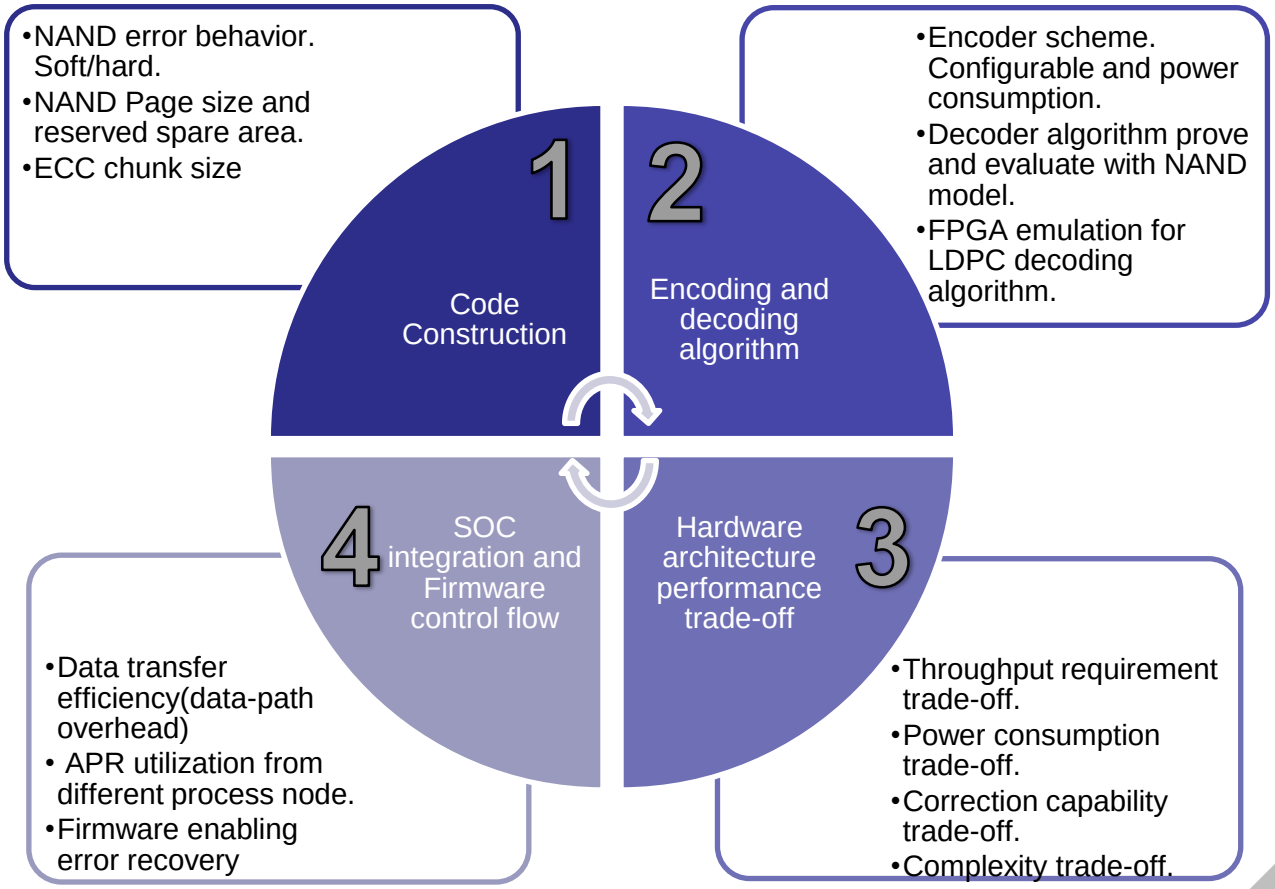
The parameter include:

1. Sensing step size.
2. Decoder internal coef.
3. Dynamic tuning the LLR
4. ……

ECC design loop related to NAND characteristics.

Flash Memory Summit

- We already have 7th generation LDPC decoder.
- Keep improving the LDPC performance.
- For higher throughput ~8GB/sec, we may go back to step1.
- After 28nm process, the design iteration depth will from code-construction to trial APR.
- EX: Find the Routing congestion issue in step 4, it may need to solve from step1.



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Before the RAID protect flow…..

Flash Memory Summit

DRAM/
DRAM-less/
Small DRAM

SLC-first/
TLC-direct write/
Dynamic SLC

One-pass /
Multi-pass/
Pair-page
mapping

WL to WL short
Failure range

All the issues combine together!

Capacity
(RAID overhead)
Binary/arbitrary

Program failure
DRAM-backup/
Flash-cache/
RAID recover/

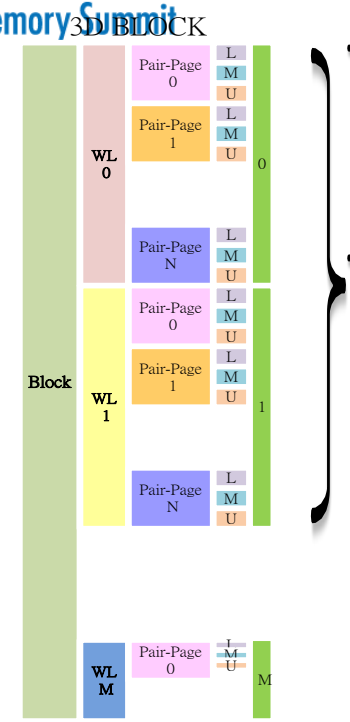
WL open
Failure range

Recovery latency

BUT THE SAME CONCEPT IS…….

Sili on

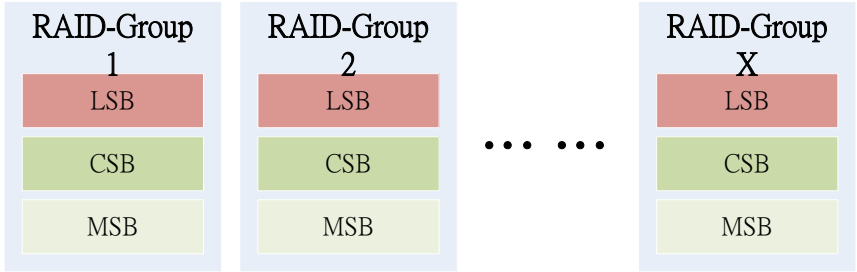
Don’t put eggs in the same basket.



Damage range of Program fail / Word-line Open

Damage range of Word-line short

Put the pages in the same failure range into different RAID-Group



- Different flash will have different failure range.
- Different application will have different RAID encoding flow.
- Reserve the maximum flexibility for all controller to support all kinds of 2D/3D NAND.
- If you don’t want to use RAID, What alternative you still have?
  - Read-back check after program.

Matlat demo platform.

Matlab interface

- Matlab base program.
- Gather the data and process by matlab.
- More easily to show the figure.
- Provide high level controller interface.
- NAND access CMD packet

CMD translation

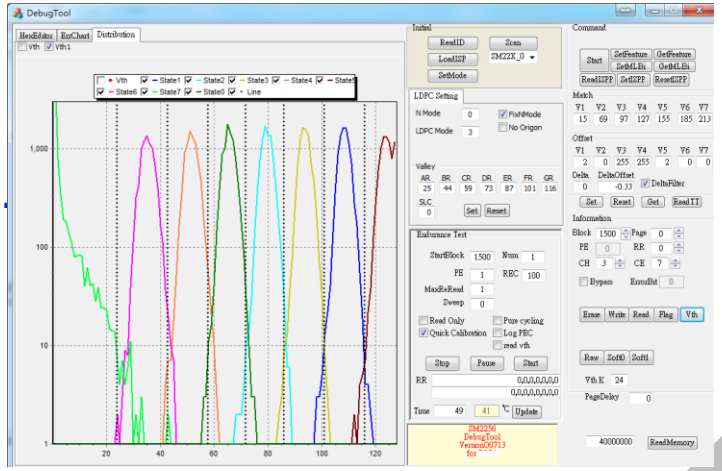
- Hookup the Matlab API to USB/PCIE driver.
- Provide several different NAND access functions to provide Matlab high level control interface.
- SMI controller specification function demo. (Adaptive chargine/Vth-trakcing/LDPC soft-decoding). Provide a function call.

SATA/PCIE controller

- Firmware implement the Vendor CMD to serve all kinds of NAND access.
- Complex function implement by ARC/ARM firmware to provide specific function demo.

ECC tool update with all NAND.

- SATA 2258/2259
- PCIE 2260/2262/2263/2270/2264
- Color Vth-distribution. All WL Vth-distribution.
- Error recovery golden flow.
- Soft-info fetch correctness analysis.
- Automation RTBB analysis.
  - (OEM special request support)
  - ECC decoding/encoding, randomizer model.
- ISPP tuning for verification.



Thanks.

- Q&A

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