Page and Block Alignments to Maximize SSD Performance

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Outline

- What is Block Alignment?
- Design Space
- Fixed ECC per Page
- Fixed ECC data size
- Integer ECC per block
- Summary

Block Alignment

- How to select IO Block boundaries and FEC block boundaries for maximum performance?
  - Minimize Flash Read BW
  - Minimize ECC BW and complexity
  - Minimize Firmware Complexity
  - Minimize Latency
  - Maximize Drive size

Definitions

- Flash Page (ie. 16k Bytes)
- Flash Spare (ie. 448 Bytes/8k)
- FEC Block Data
- FEC Block Parity
- User IO Block or “IOB” (ie. 4k,2k,1k Byte)
  - FEC Data + FEC Parity = “FEC”
  - Code Rate = “CR”
  - Frame (FEC Block) Error Rate = “FER”

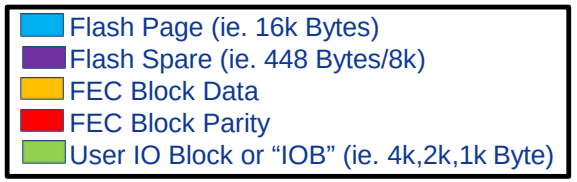
Complexities

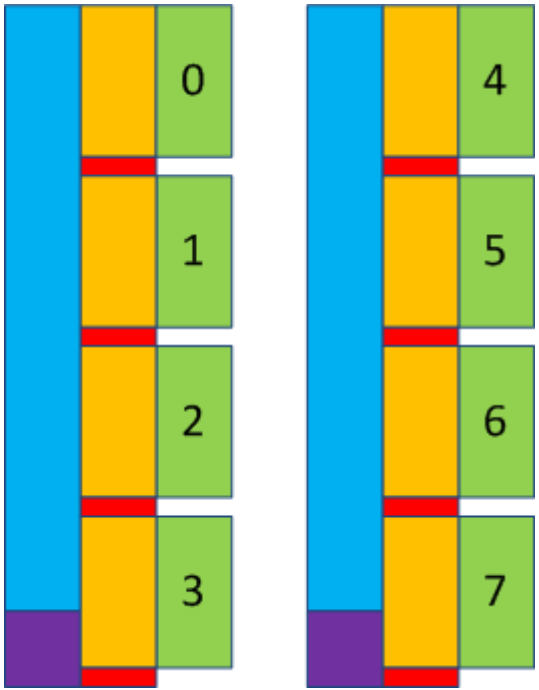
- Flash Technology?
  - MLC, TLC or QLC
  - Performance differences per sub-page
  - Spare Size
  - How many PE Cycles
  - Support for multiple devices
  - Future Device Support

Complexities (cont)

- ECC Code Rate Support
  - Variable or fixed per page?
  - Fixed or changing over time?
  - Multiple Quality Of Service targets
  - FER performance targets
  - Future-Proof design
- Outer structure (RAID), Sector Size (512/520), Meta Data structure and size,etc…

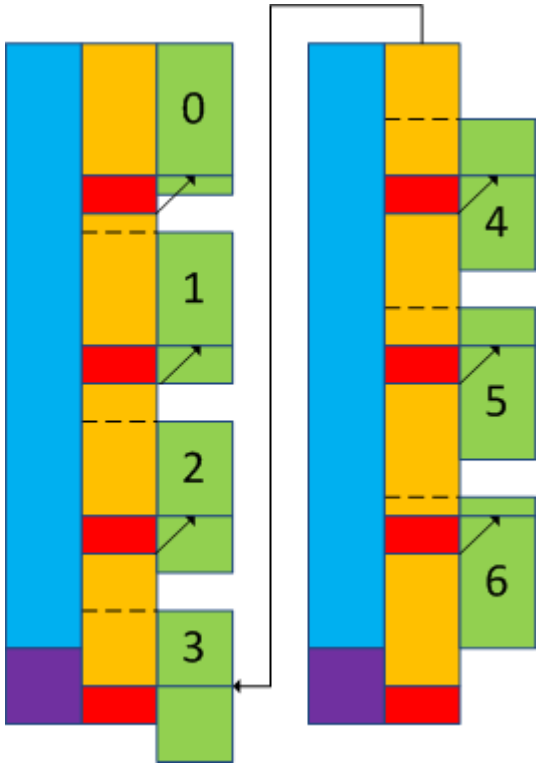
Fixed ECC/Page Standard Alignment





- 4 FEC / 16k Page
- 4 4k IOB / Page
- Always 4 FEC / Page

Fixed ECC/Page Reduced Code Rate



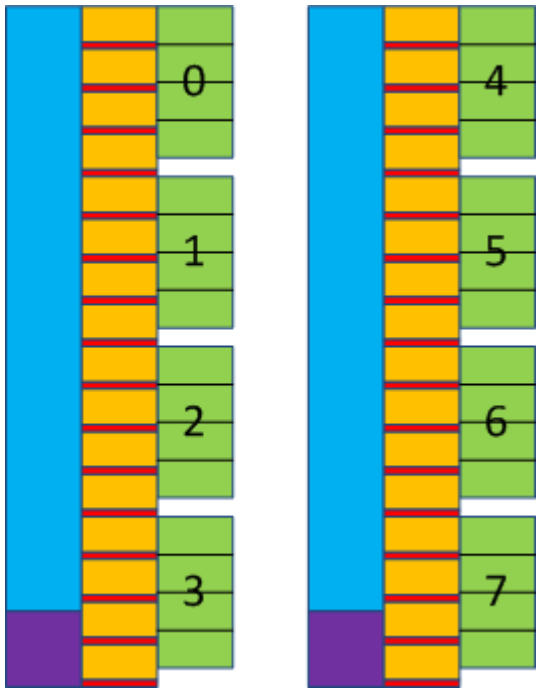
Flash Page (ie. 16k Bytes)
Flash Spare (ie. 448 Bytes/8k)
FEC Block Data
FEC Block Parity
User IO Block or “IOB” (ie. 4k,2k,1k Byte)

- Same overall FEC size
- Reduce data size to reduce CR
- FEC and IOB no longer aligned

Fixed ECC/Page

- Good Code Rate Control
- All FEC blocks the same size
- Loss of FEC/Block alignment
  - 50+% higher Flash Read Bandwidth
  - 50+% higher ECC power consumption

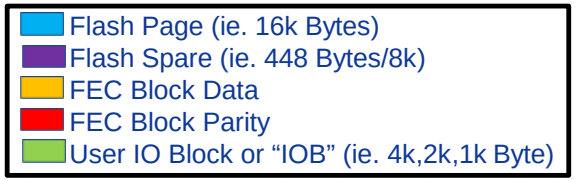
Fixed ECC Data Size Standard Alignment

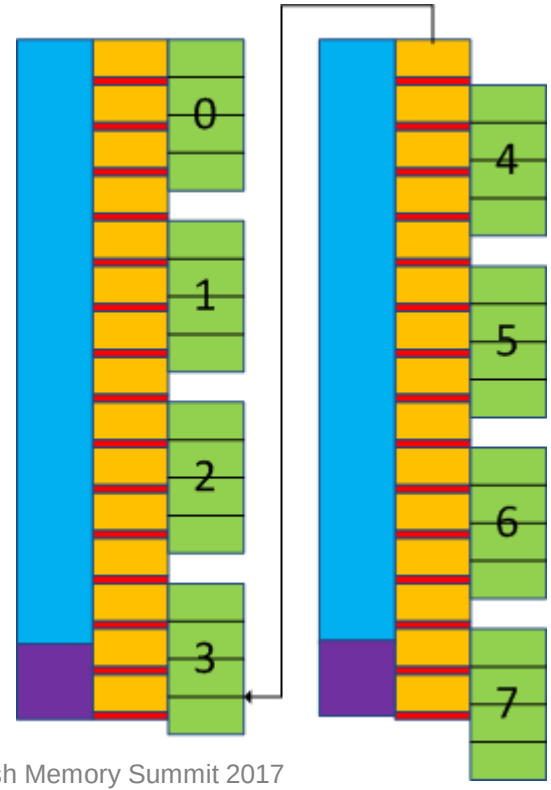


- IOB is 4kByte
- FEC is 1kByte Data
- 16 FEC / 16k Page
- IOB is 4 FEC blocks
- Alter FEC / Page to change CR

Flash Page (ie. 16k Bytes)
Flash Spare (ie. 448 Bytes/8k)
FEC Block Data
FEC Block Parity
User IO Block or “IOB” (ie. 4k,2k,1k Byte)

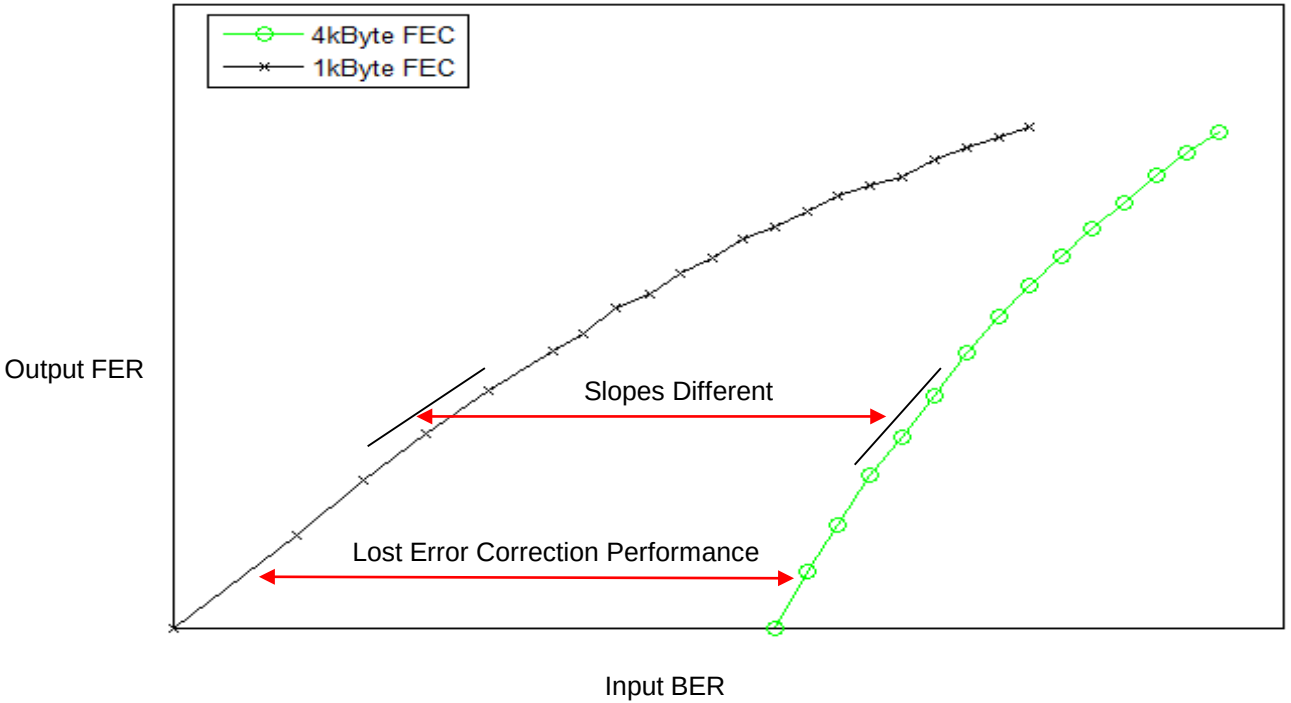
Fixed ECC Data Size Reduced Code Rate





- 15 FEC / Page
- New CR is 15/16 * original CR
- Integer FEC / Page
- Integer FEC / IOB

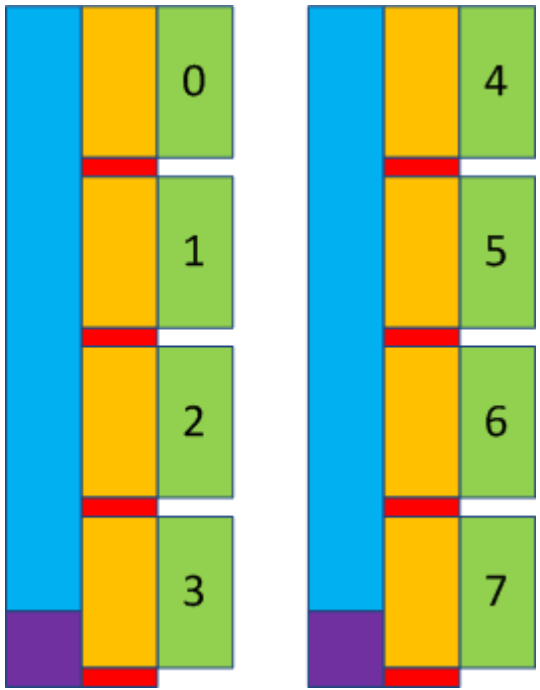
Fixed ECC Data Size Error Correction Performance



Fixed ECC Data Size

- All FEC Blocks the Same Size
- Minimum Flash Read BW
- Some Code Rate Flexibility
  - Integer Number of FEC blocks per Page
- Smaller FEC block size impacts ECC performance

Integer FEC per IOB Standard Alignment



- 4kB IOB
- Allow arbitrary FEC block size.
- All IOB have integer number of FEC blocks

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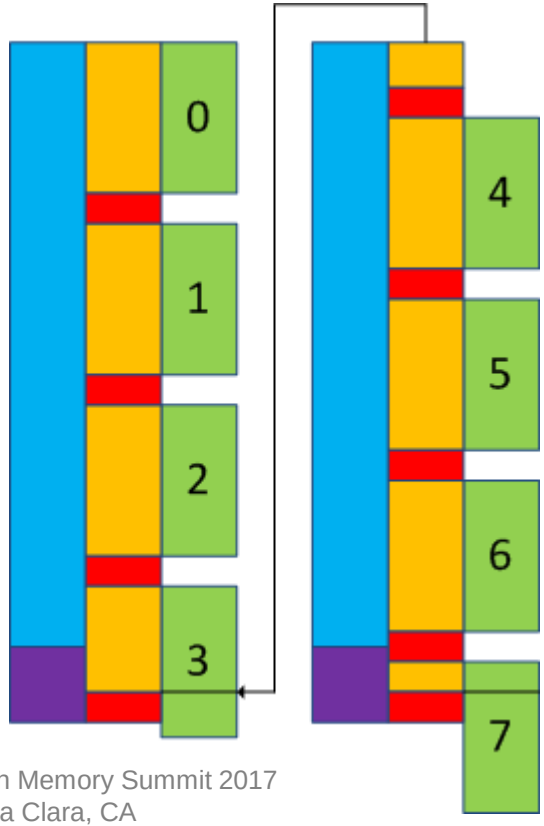
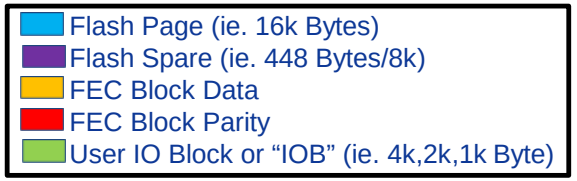
Integer FEC per IOB Reduced Code Rate





- Arbitrary choice of CR
- 3/4 of IOs are 1 FEC
- ¼ of IOs are 2 FEC

Integer FEC per IOB

- Good code rate support
- Good ECC performance
- Minimum flash read BW
- Require flexible solution for hardware, ECC and firmware
  - Our Controllers support all these methods

Summary

- Modern Flash devices require Good Code Rate configurability
- Integer FEC/IOB is best alignment solution.
  - All information read from Flash is used
  - Good ECC performance characteristics
- Must have flexible Hardware, ECC and Firmware Solution.