

Can Next-Generation 3D TLC NAND Extend Enterprise Applications?

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Can Next-Gen 3D TLC NAND Extend Enterprise Applications?

The First Generation of commercially available 3D TLC NAND:

- Demonstrated viable solution for Enterprise use
- Enabled higher monolithic density and lower Cost/GB than 2D MLC
- Exhibited excellent Program-Erase cycling endurance
- However, also exhibited higher Data Retention error rates relative to 2D MLC
 - Enterprise controller must adapt to manage new mechanism

Can the Next Generation of commercially available 3D TLC NAND improve on First Generation?

- In 2D MLC NAND, newer generations exhibited lower cycling endurance
- 2D NAND scaling relies on shrinking ground rules (increased CCI)
- 3D NAND scaling relies on increased word layers

Next-Gen 3D TLC NAND: Context of Study

Scope of Sampling

- First Gen 3D TLC NAND: best commercially available NAND flash at CS level (32-48 Layer)
- Next Gen 3D TLC NAND: best commercially available NAND flash at ES level (64-72 Layer)

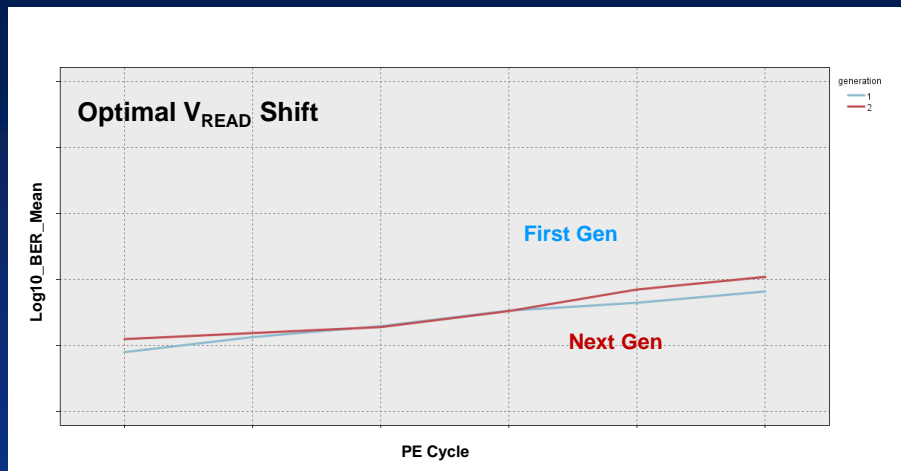
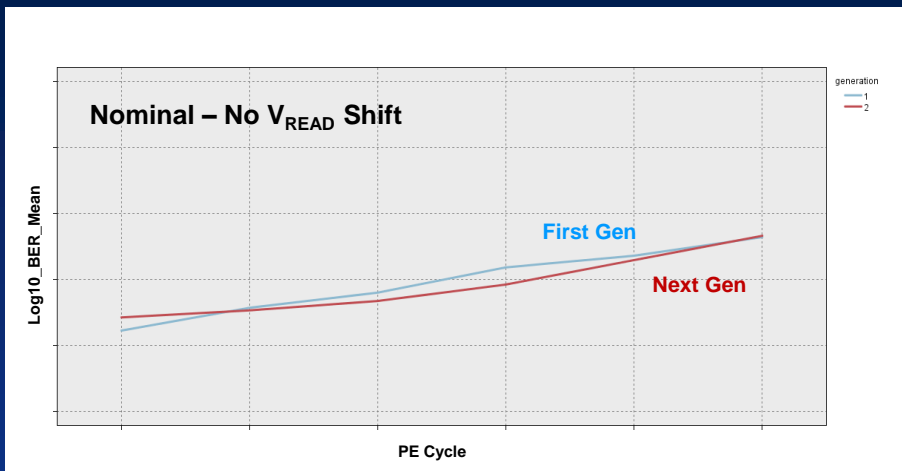
Parameters of Testing

- Arrhenius-based acceleration of PE Cycling and Data Retention bake
 - (use of Activation Energy - E_a)
- Target use case @40C
- All voltage read offsets moved simultaneously during characterization
 - Quick 1st order approximation of Optimal V_{READ} shift
 - Independent V_{READ} level shifting required for true optimal

Value Proposition

- There is value to common methodology employment across manufacturers/technologies

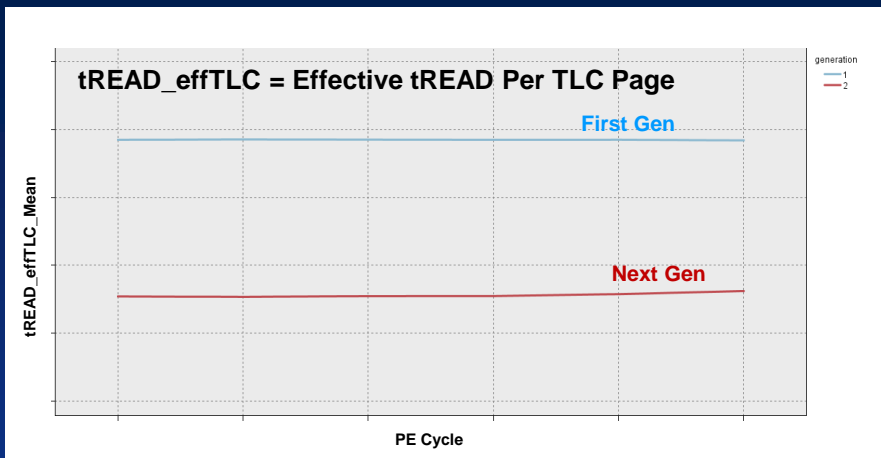
3D TLC NAND: First Gen v Next Gen – PE Cycling



Next Gen ES Shows Similar PE Cycling Endurance as First Gen CS

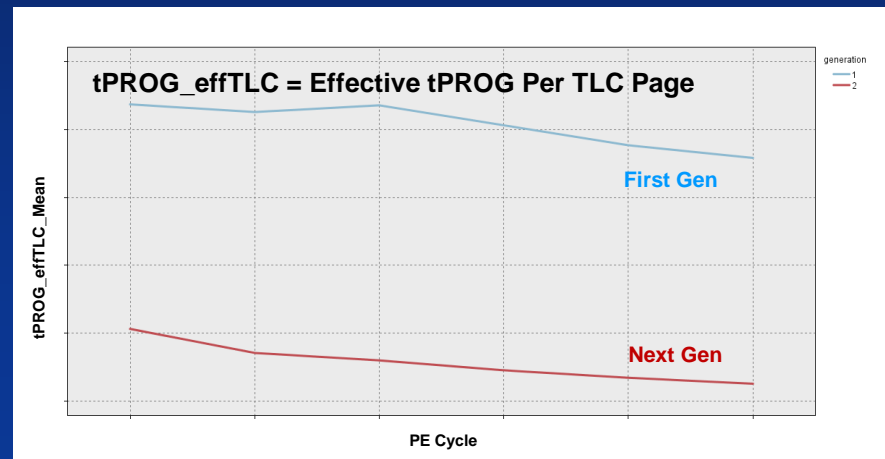
- Next Gen showing some indication of higher BER trajectory with increased PE cycling
- Next Gen CS should maintain or improve cycling endurance over ES

3D TLC NAND: First Gen v Next Gen – tREAD, tPROG

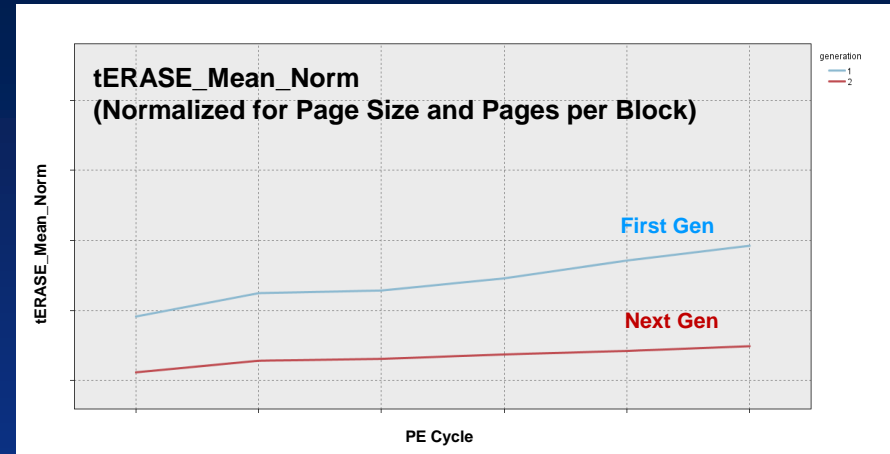
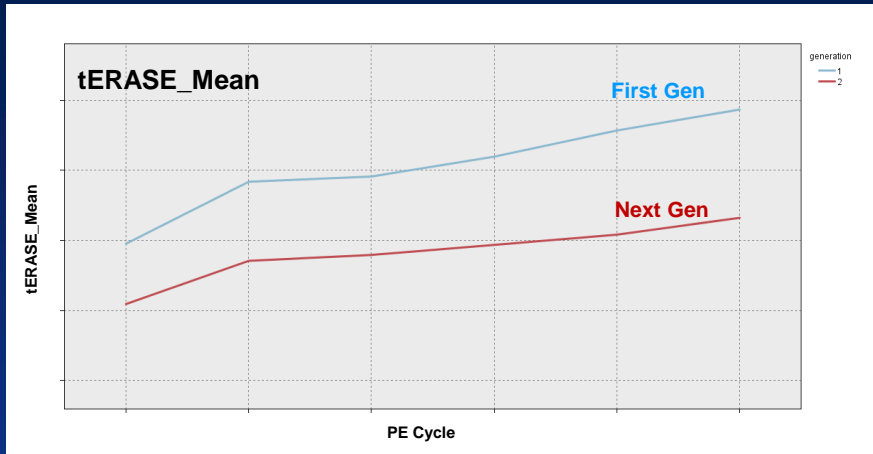


Significant (~25%) improvement in both tREAD and tPROG for Next Gen

- Next Gen CS tREAD/tPROG may increase over ES in trade-off for increased endurance



3D TLC NAND: First Gen v Next Gen – tERASE

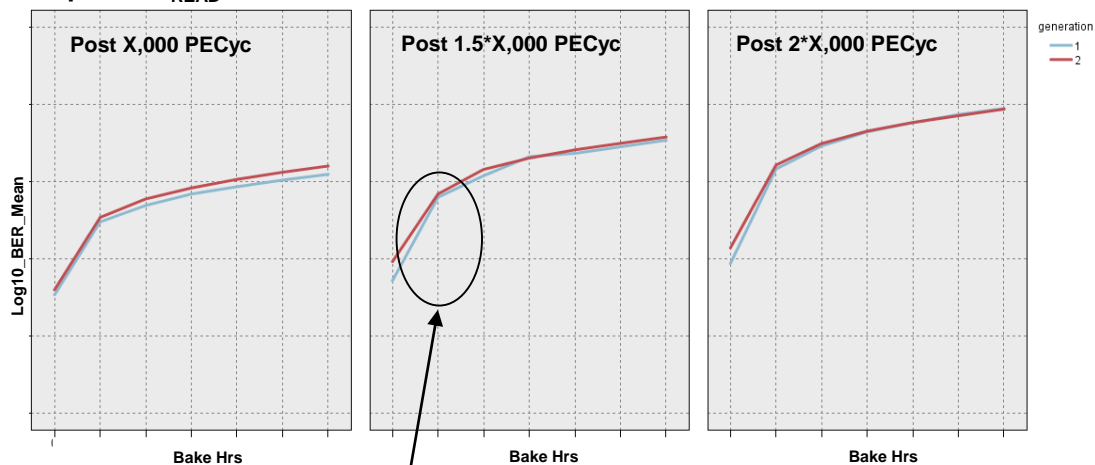


Significant (33-50%) improvement in tERASE for Next Gen

- Next Gen CS tERASE likely similar to ES

3D TLC NAND: First Gen v Next Gen – Post Cycle DR Bake

Optimal V_{READ} Shift

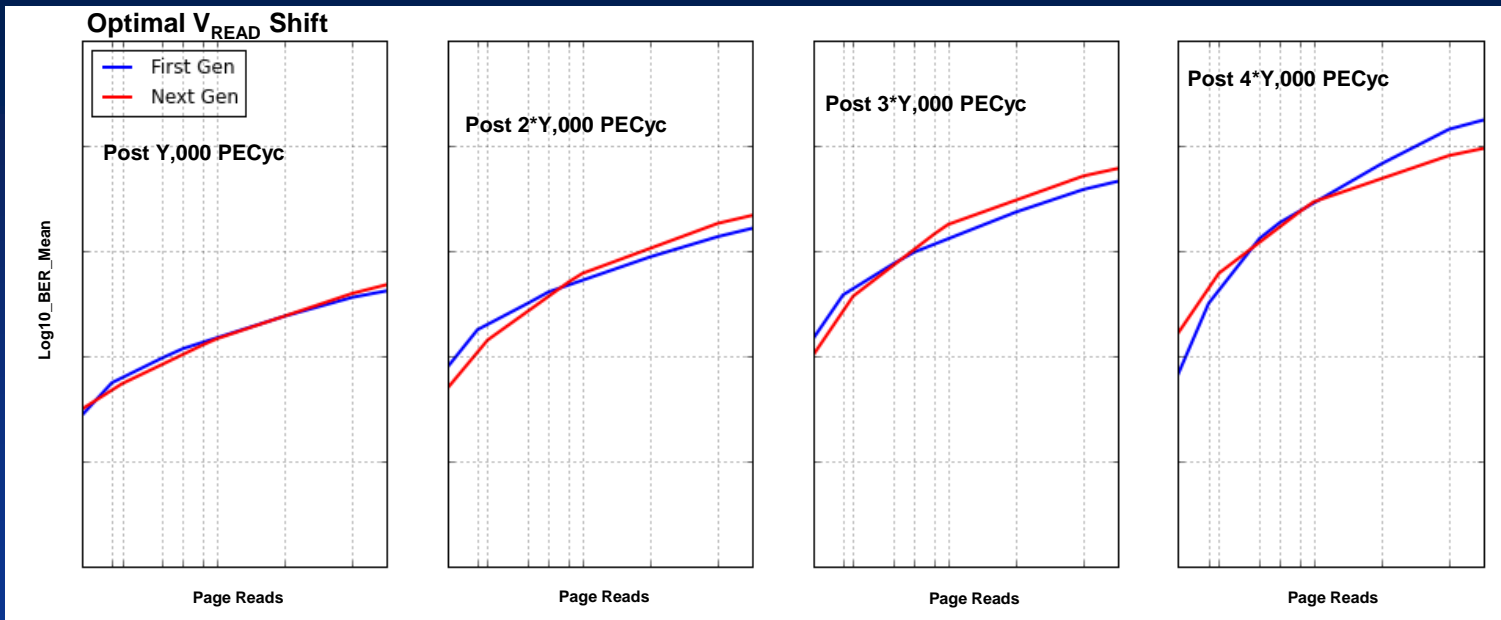


Next Gen ES shows similar post cycle Data Retention BER as First Gen CS

Consistently observe spike in BER at beginning of retention

- Spike in BER due to rapid shift in optimal V_{READ} thresholds
- Fast V_{READ} threshold shifts must be accommodated in Enterprise applications

3D TLC NAND: First Gen v Next Gen – Post Cycle Read Cycling



Next Gen ES shows similar post cycle Read Cycling BER as First Gen CS



Next-Gen 3D TLC NAND: Conclusions

Next-generation 3D TLC NAND continues to be viable solution for Enterprise use

- Comparable PE Cycling endurance, post cycle DR, post cycle Read Cycling to First Gen
- Short-term Data Retention continues to be a challenge
- Significantly improved array timings over First Gen

Initial conclusions based on Next Gen ES performance

- Final Next Gen CS performance may vary based on endurance/timing trade-offs



Thank You!

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