



Flash Memory Summit

Persistent Memory Forum R-12 3D XPoint: Current Implementations and Future Trends

Tech
Insights

XPoint Memory Comparison

Process & Architecture

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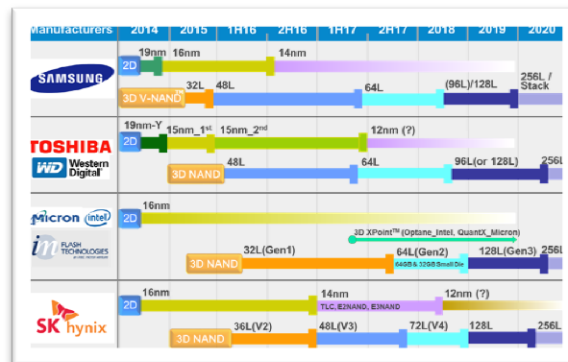
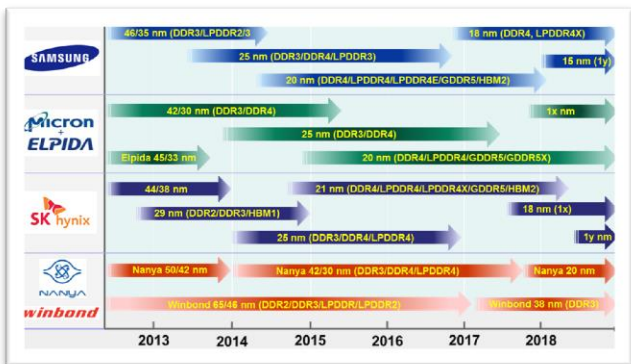
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 - Comparison with DRAM & 3D NAND



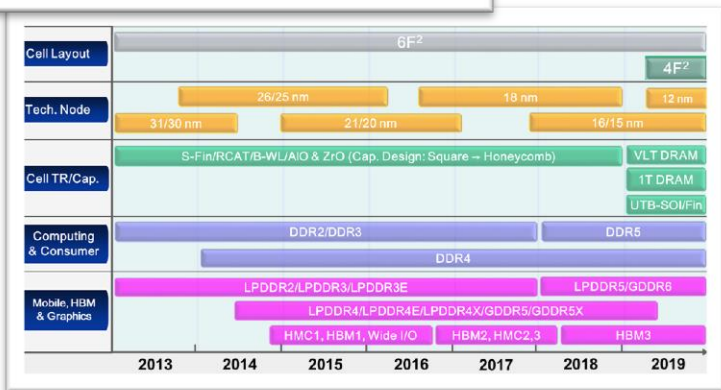
Memory Device Roadmap

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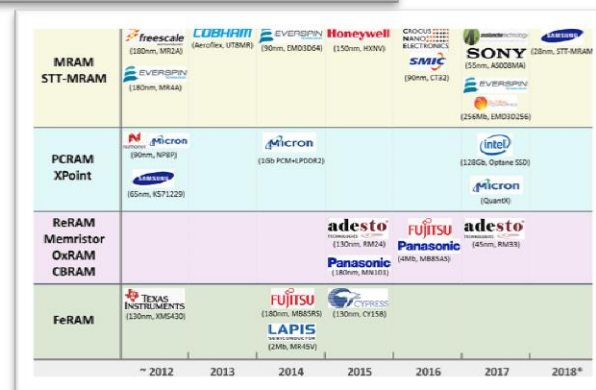


NAND

DRAM



Emerging Memory





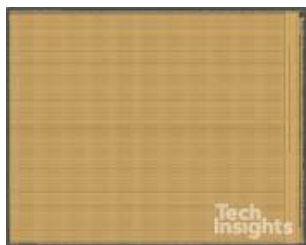
Questions About XPoint

- *PCM? Materials?
- *Selector? Ternary/Quaternary Phase? As doped?
- *Multi-Stacked?
- *Layouts? PCM patterning? Double patterning used?
- *Memory density? Memory array efficiency?
- *Overall memory cell design & architecture?
- *Technology Node?
- *Die floor plan?
- *CMOS under Memory Array?
- *Functional blocks? Circuits?
- *Top/Middle/Bottom electrodes connection?
- *Performance? Transistor parameters? Cell set/reset Current?
- *Replace NAND? Replace DRAM?
- *# Masks? # Process steps? Process sequence?
- *Cost? Cost effective product?
- *N+1?, N+2?
- *Differences from Micron QuantX?
- *Throughput? Yield?
- * etc.



XPoint Memory Overview

- 16GB single die in a PKG
- Memory efficiency: 91.4 %
- Memory density (/Die): 0.62 Gb/mm²
- Memory density (/Array): 0.69 Gb/mm²



Top Metal View



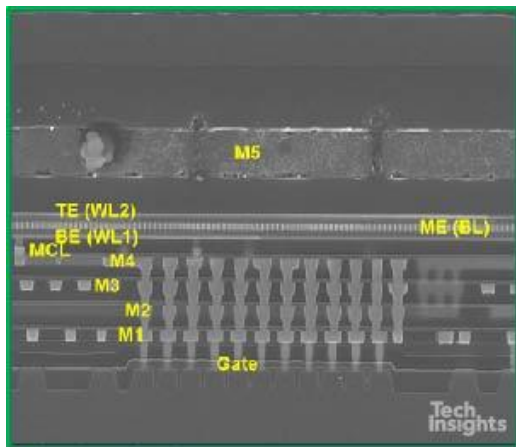
Bpoly Level View

Package dimensions	18.0 mm x 14.0 mm x 1.10 mm thick
Manufacturer, part number, downstream	Intel, MEMPEK1W016GAXT, Optane™ 16GB memory module
Wafer size, foundry, process type	300 mm, Intel, 3D XPoint memory cell over CMOS
Die markings	<Intel logo> S15C (M) © 2014
Die size (from die seal)	16.16 mm x 12.78 mm (206.5 mm ²)
Die thickness	220 μm
Number, type of metals	5, 4 Cu and 1 Al and W used as word and bit lines
Minimum observed contacted logic gate pitch	0.38 μm
Minimum observed logic transistor gate length	0.086 μm
Minimum metal pitch	84 nm
3D XPoint memory bit line (word line) pitch	38.5 nm
3D XPoint memory word line (bit line) pitch	40 nm
Memory cell area	0.0015 μm ²
Technology generation	20 nm
Feature measured to determine process generation	Half bit line (word line) pitch

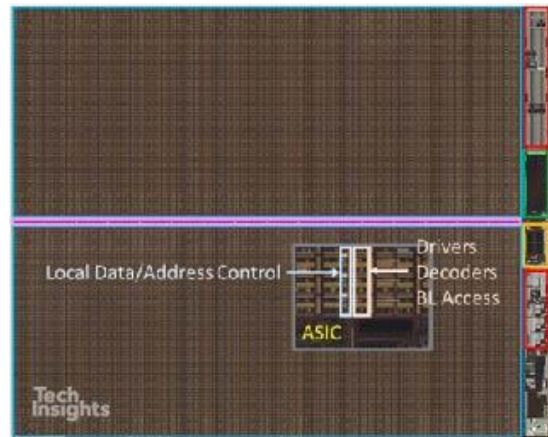


XPoint: Process Integration

- GST-based PCM (Phase Change Memory) between M4 and M5
- Storage layer vertically stacked on Selector
- Se-Ge-Si ternary phased OTS Selector with As doped
- Double memory cell stacked
- 1 Poly Si (Co-silicide), 5 Metals (excluding memory/WL/BL layers)



SEM X-Section (Array)



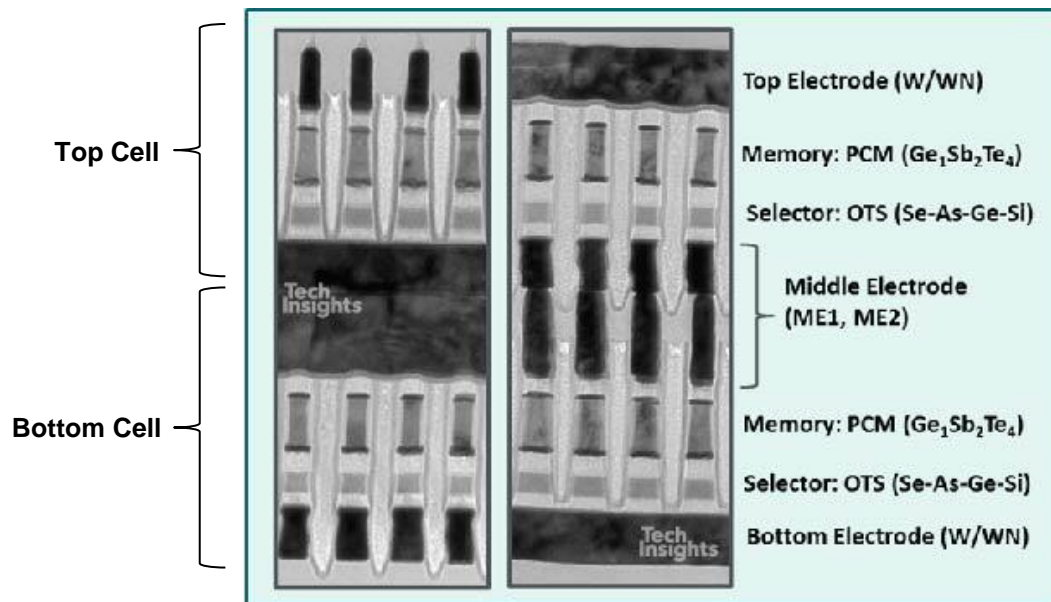
Suggested Functional Blocks (Bpoly View)

- Voltage Pumps or Regulators
- Digital Control Block (ASIC)
- Data Input/Output Cache Circuits
- I/O Circuits Pads, Buffers
- Memory Block Peripherals Row/Column Drivers Decoders, BL Access
- Local Address/Data Control (ASIC)
- Local Data Cache



XPoint: Memory/OTS Elements

- Top & bottom cell stacked
- TWL/TE/PCM/ME/OTS/BE/BL2/BL1/TE/PCM/ME/OTS/BE/BWL
- PCM: $\text{Ge}_{0.12}\text{Sb}_{0.29}\text{Te}_{0.54}(\text{Si}_{0.05})$, OTS: $\text{Se}_{0.44}\text{As}_{0.29}\text{Ge}_{0.1}\text{Si}_{0.17}$,





XPoint, could be

✓ 1,000 times faster than NAND Flash

✓ 10 times denser than DRAM



Really?

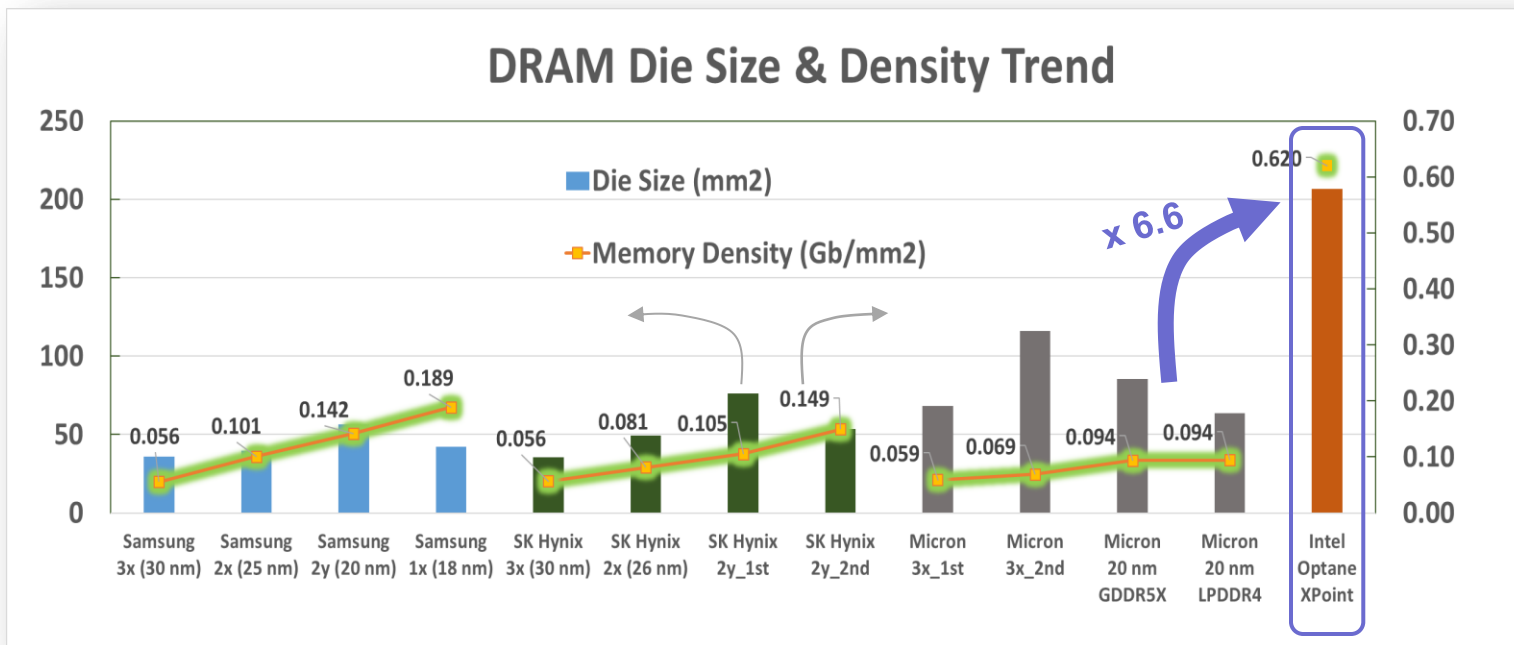
✓ 1,000 times better endurance than NAND

vs. 3D NAND?



XPoint vs. DRAM: Memory Density

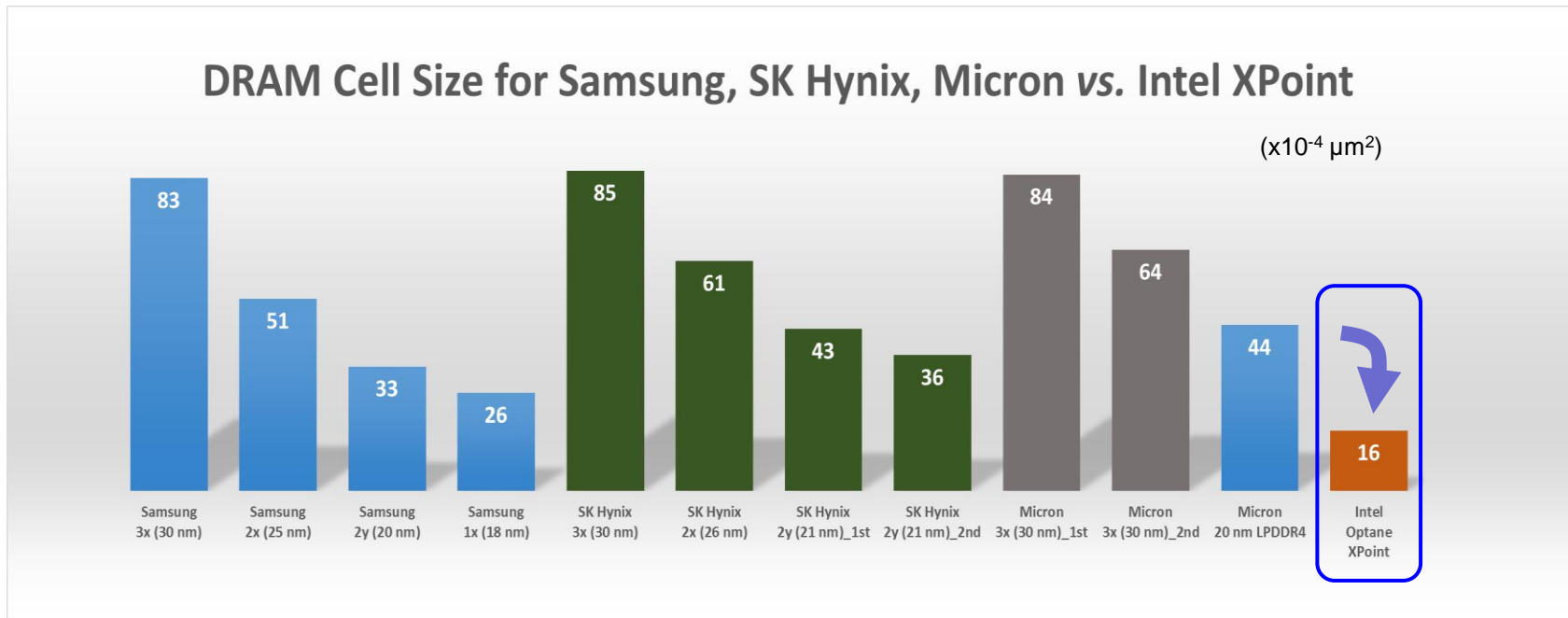
- Memory Density: x3.2 (vs. SS 18nm DRAM), x6.6 (vs. M 20nm DRAM)





XPoint vs. DRAM: Cell Size

- Memory Cell Size: 58% (vs. SS 18nm DRAM), 36% (vs. M 20nm DRAM)

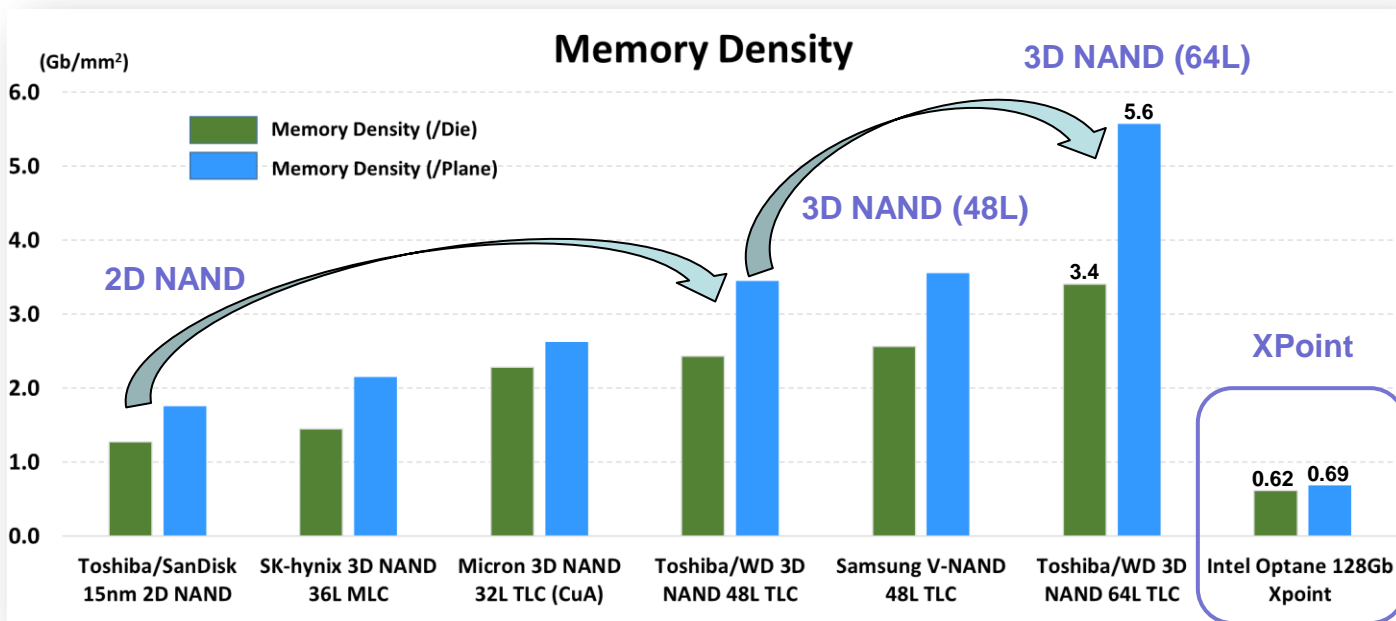




XPoint vs. 3D NAND: Memory Density Tech Insights

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- Memory Density: 24% (vs. SS 48L V-NAND TLC), 18% (vs. Toshiba/SanDisk 64L)



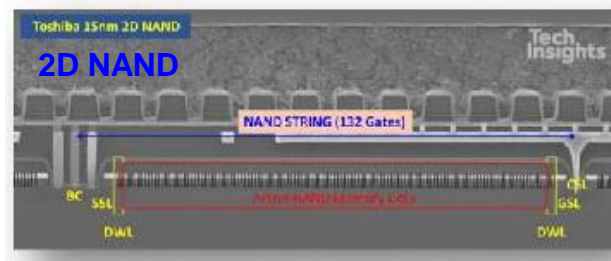
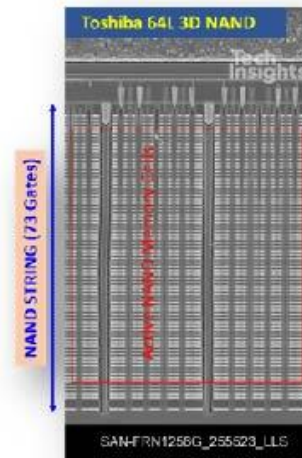
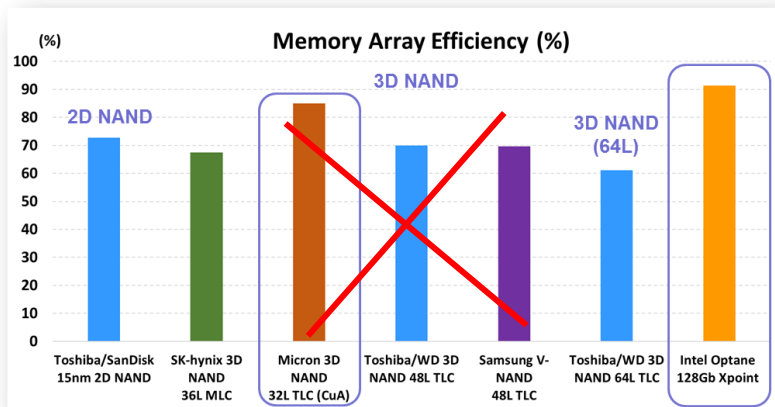


XPoint vs. 3D NAND: Array Efficiency

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- Memory Array Efficiency ... may not represent

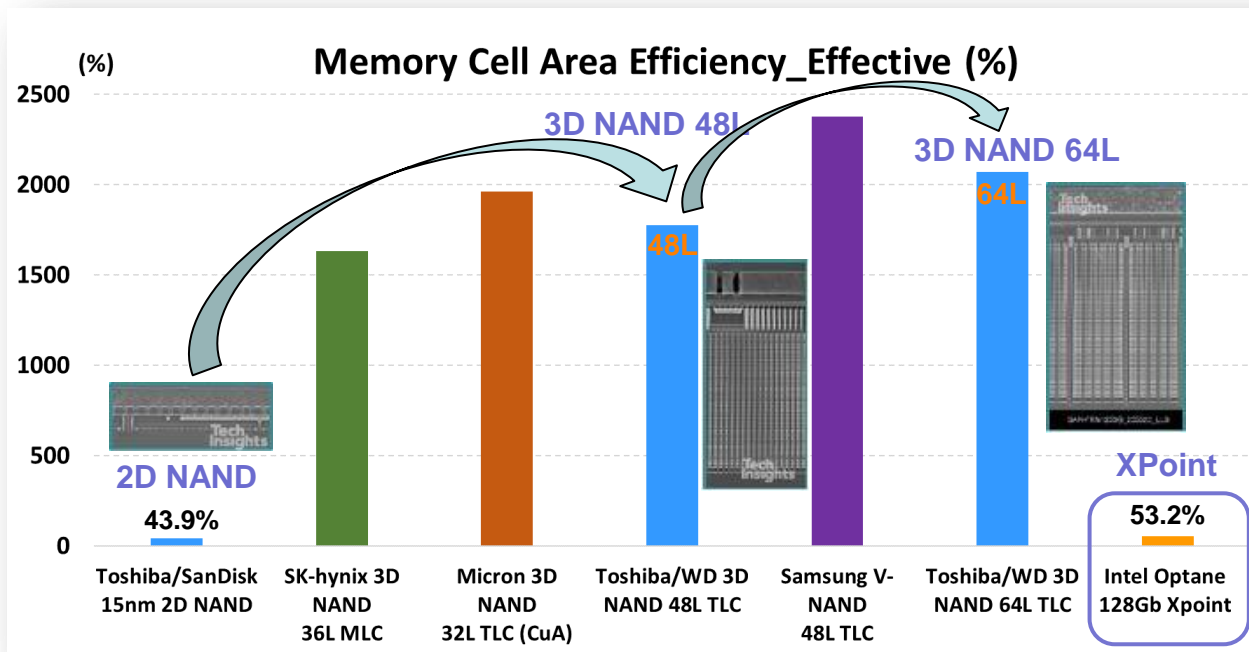
Effective Memory Cell Area Efficiency





XPoint vs. 3D NAND: Array Efficiency

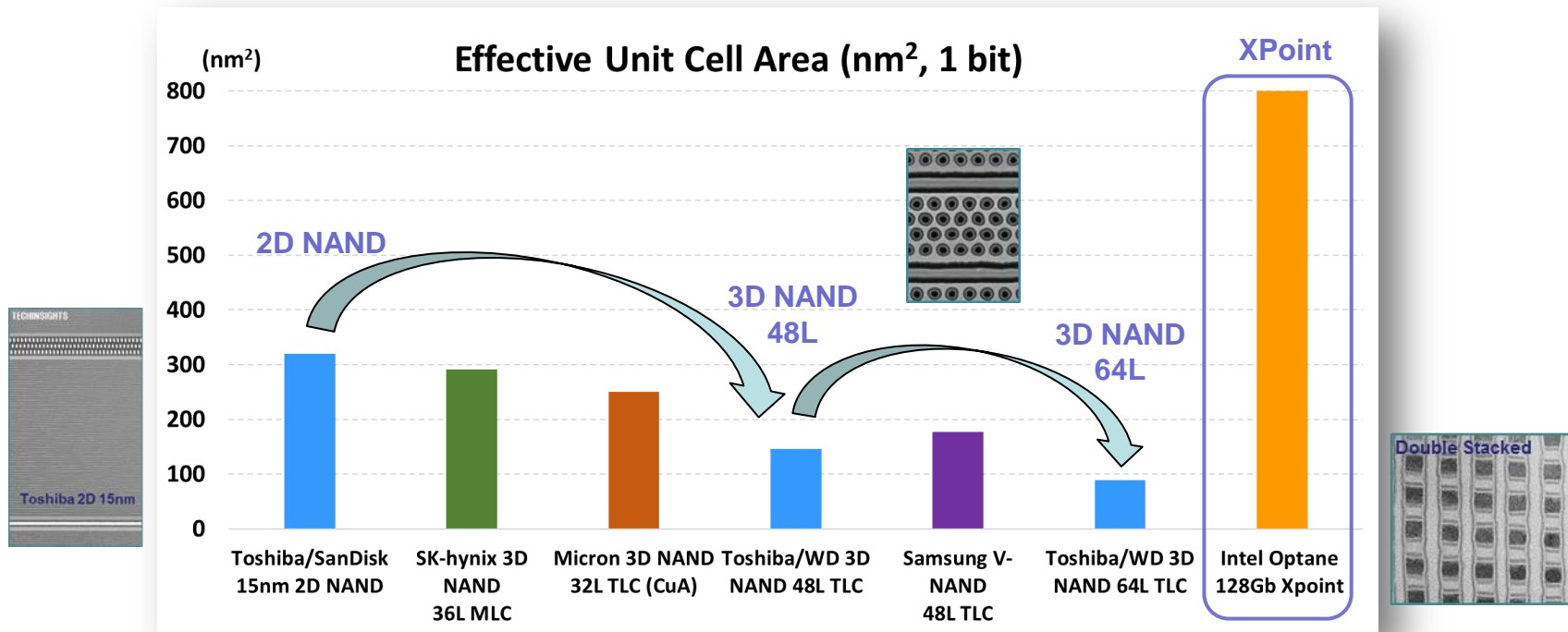
- Comparison of Effective Memory Cell Area Efficiency: Higher the better





XPoint vs. 3D NAND: Unit Cell Area

- Comparison of Effective Unit Cell Area: Lower the better





XPoint is

vs. DRAM

6 times denser than Micron 20 nm DRAM

3 times denser than Samsung 1x DRAM

vs. NAND

18% memory density of Toshiba/SanDisk 64L NAND

Higher memory cell area efficiency than 2D NAND

Relatively lower cell area efficiency than 3D NAND