PHISON
Knows What You Need

Improving the Design of DRAM-Less PCIe SSD

Session 101-A: Consumer Applications

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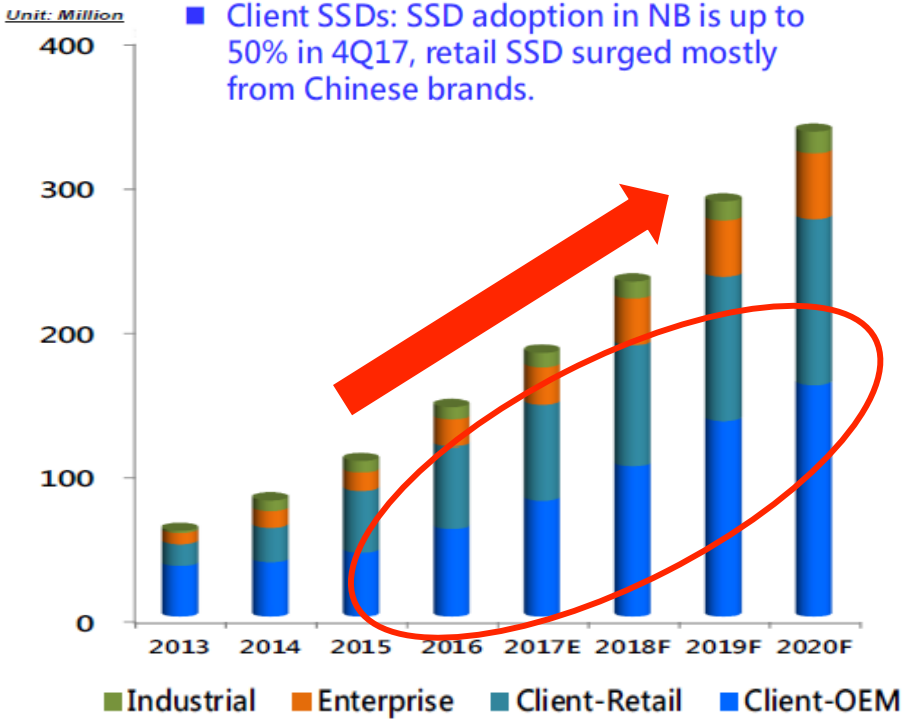
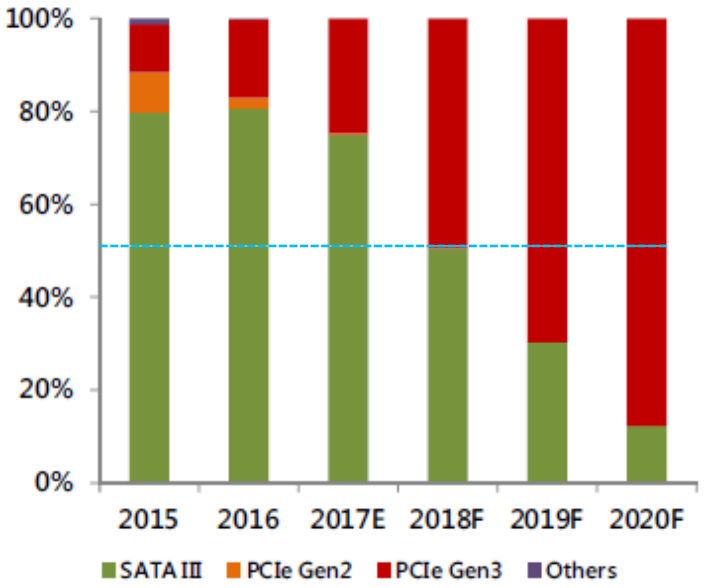
SSD Market Trend

- Client SSDs: SSD adoption in NB is up to 50% in 4Q17, retail SSD surged mostly from Chinese brands.

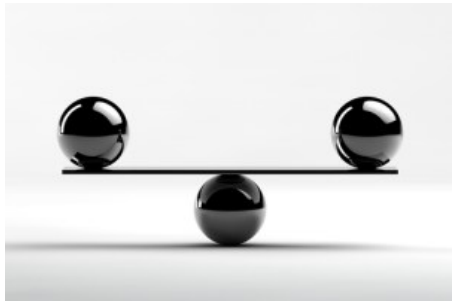


- The adoption rate of PCIe Gen3 in Client SSD market is estimated to be 50% in 2018



Source: DRAMeXchange, 2017

Concerns of Client SSD

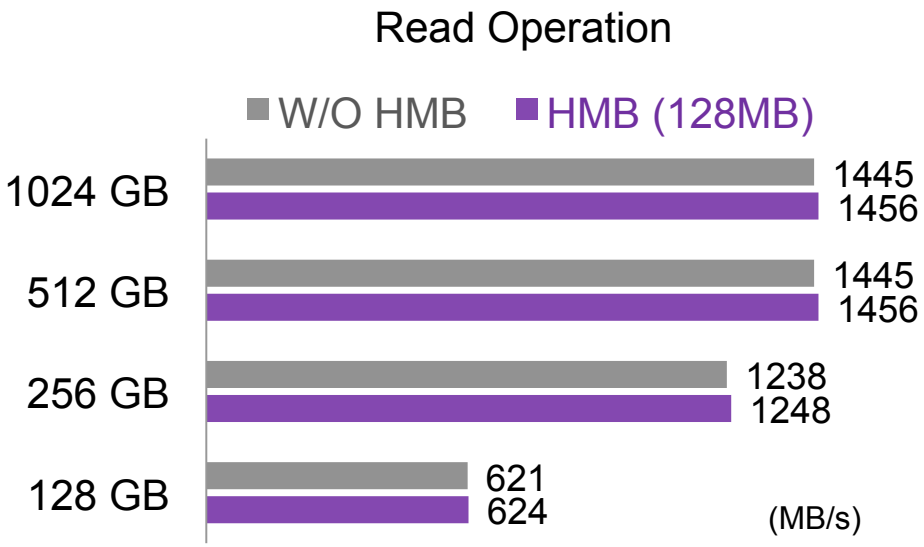


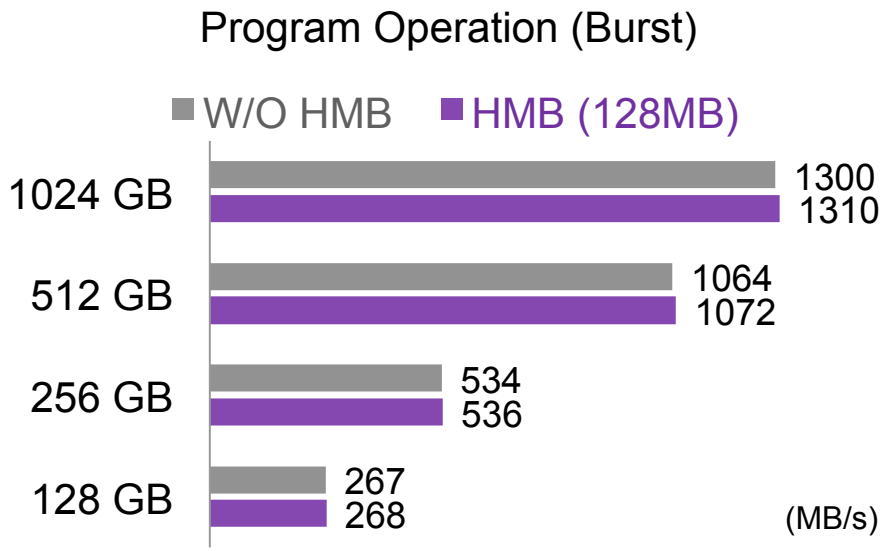
Host Memory Buffer (HMB)

- Since NVMe Protocol v1.2 (Optional)
- Allow the Host driver to allocate system memory for the SSD's exclusive utilization
- Quick Notes
  - ✓Enabled / Disabled by Host
  - ✓Preserve / Reassign buffer after Runtime D3 or any other events requiring Host to reclaim the assigned buffer
  - ✓Device is allowed to specify minimum and allowable buffer size
  - ✓Controller has to ensure there is no data loss or data corruption in the event of a surprise removal

HMB Enablement

Sequential Pattern

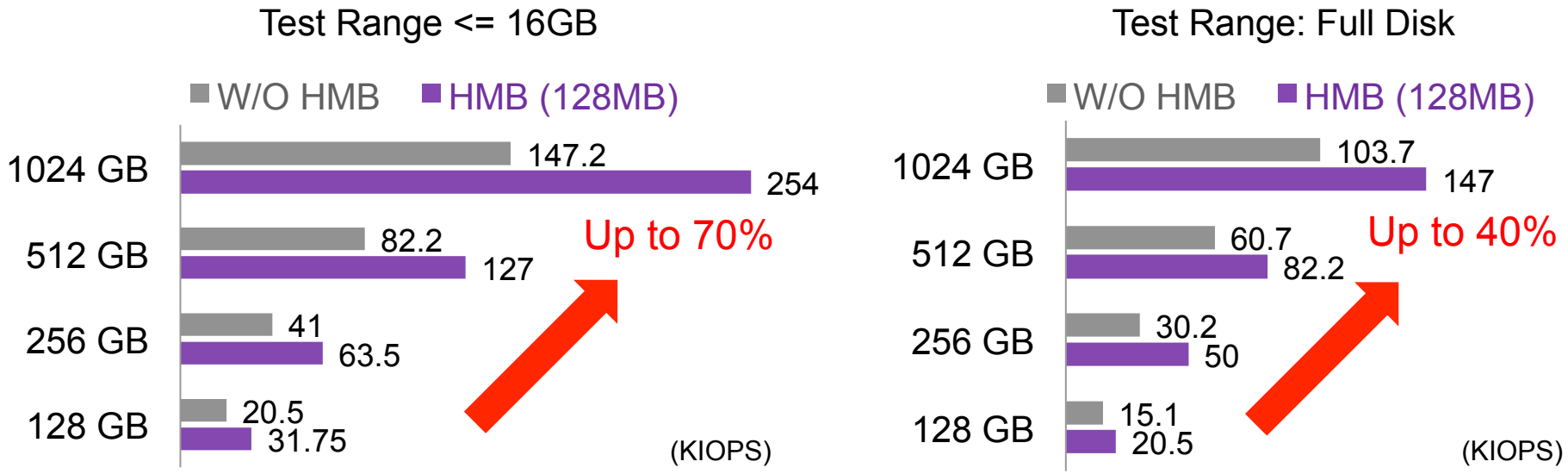




HMB does NOT improve performance on Seq. Pattern significantly

HMB Enablement

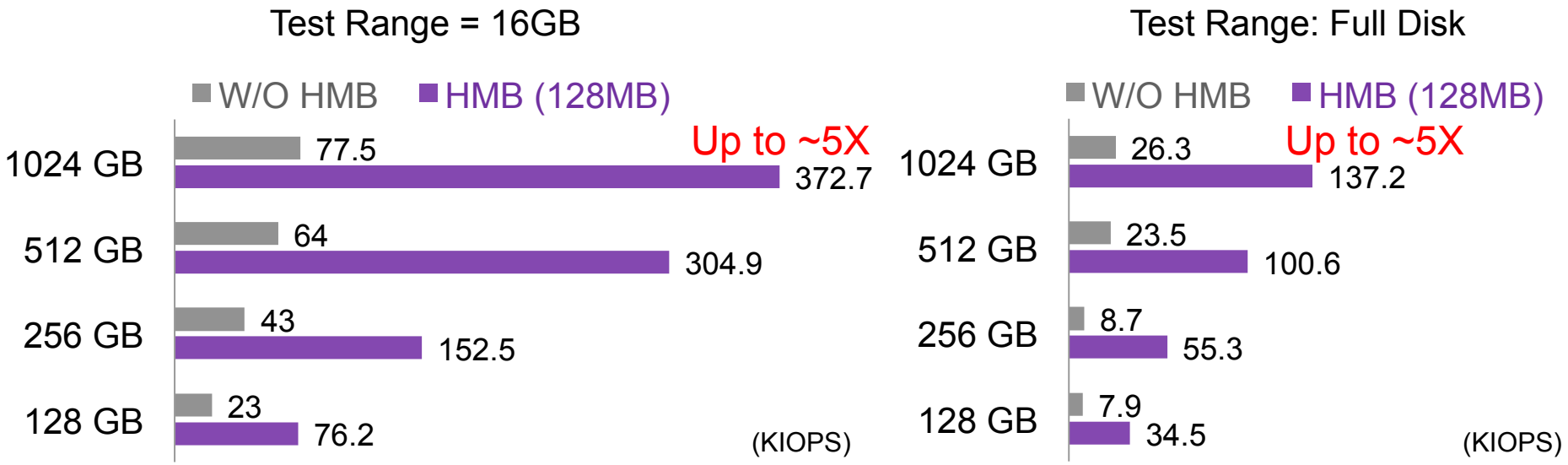
Random Pattern (Read)



Main benefit due to HMB is on Ran. Pattern

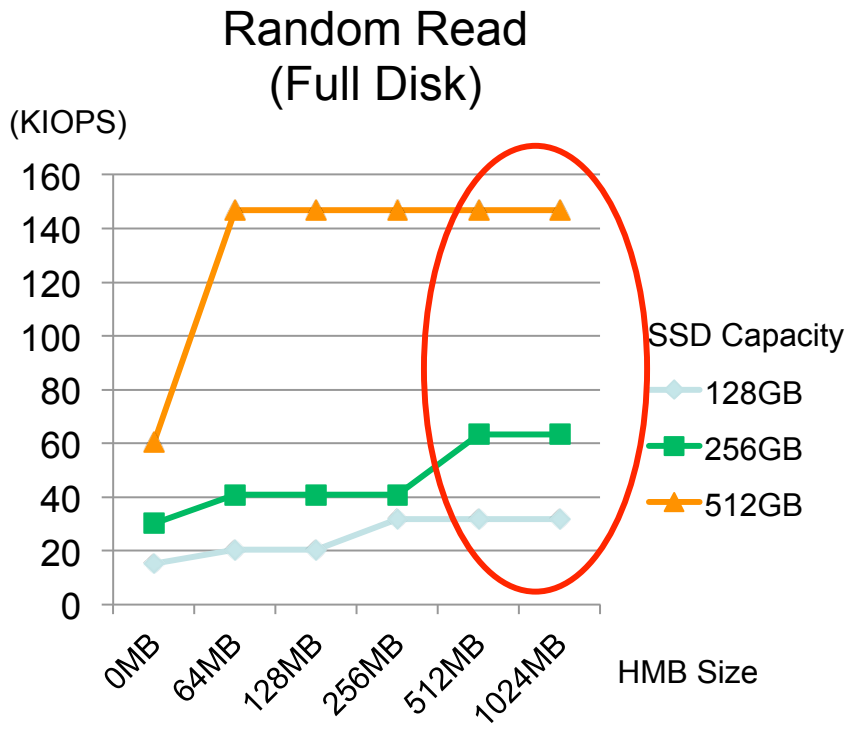
HMB Enablement

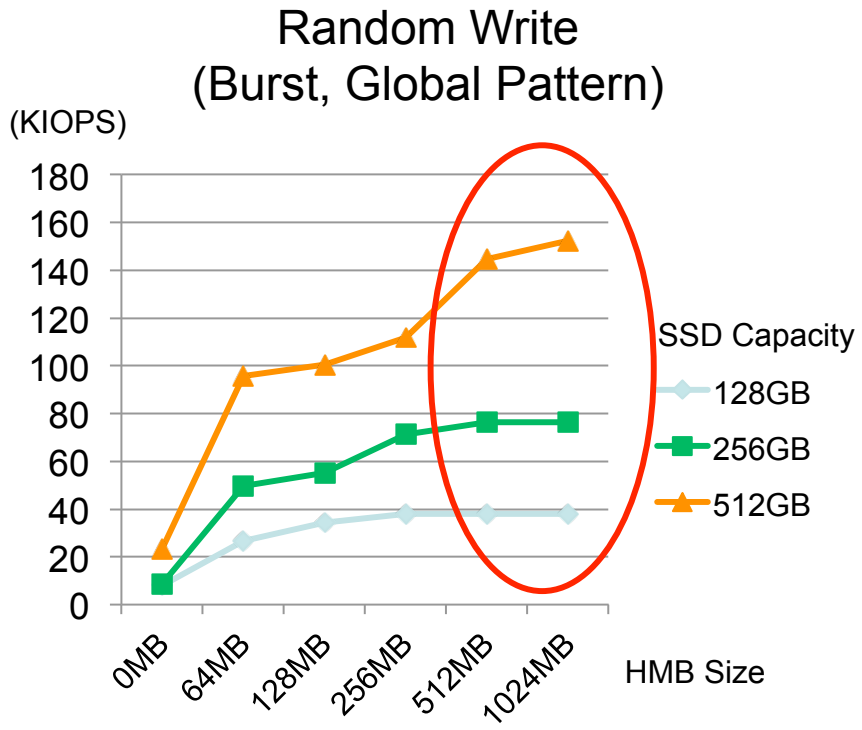
Random Pattern (Write, Burst)



Ran. Write operations can gain more from HMB

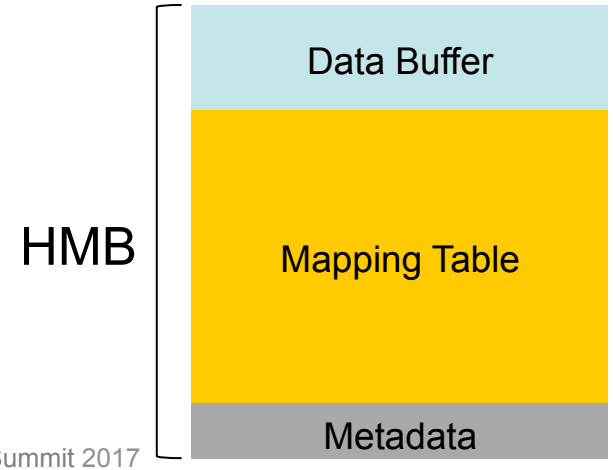
Random Performance vs. HMB Size



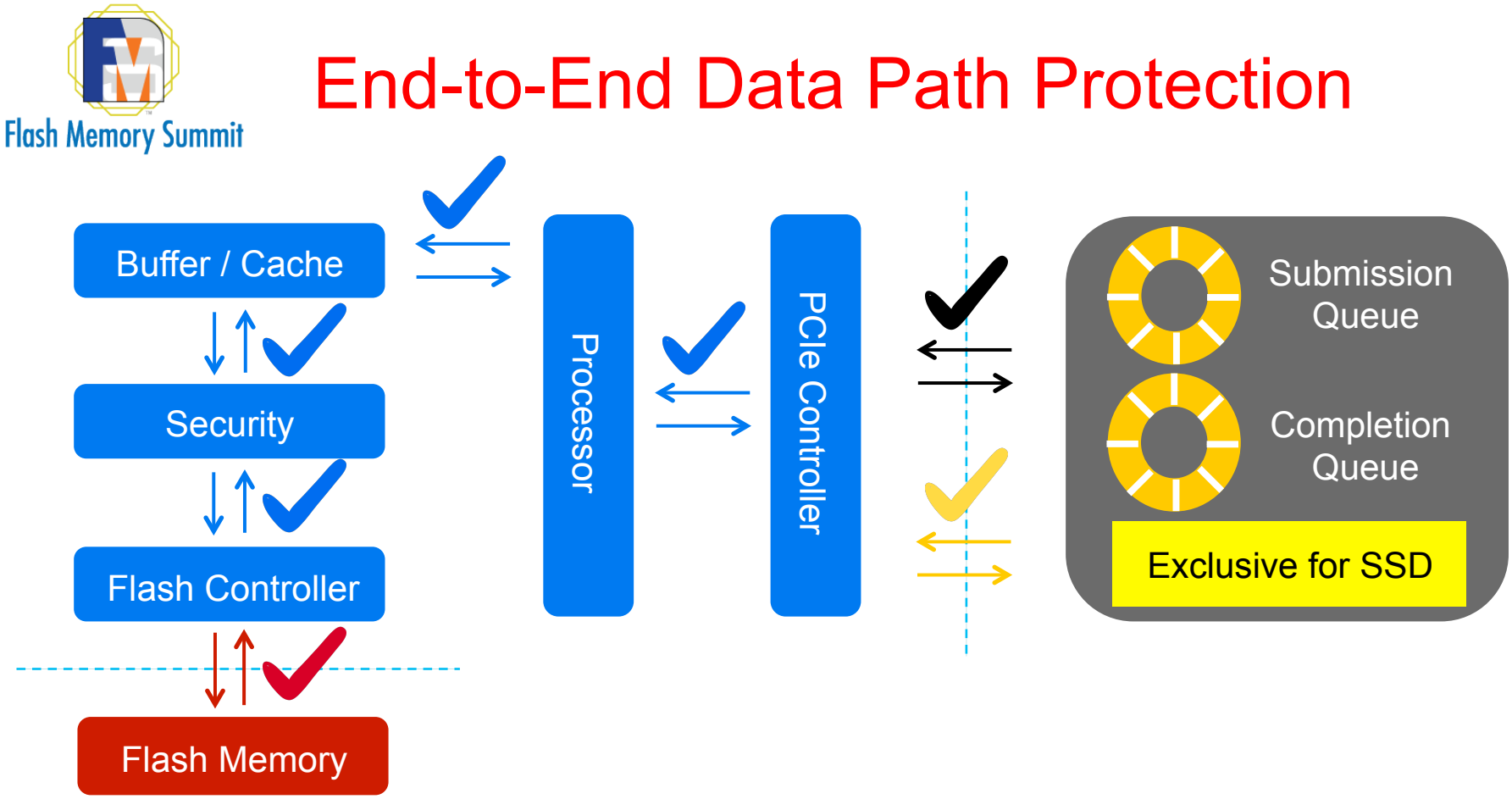


Data Integrity for HMB Support

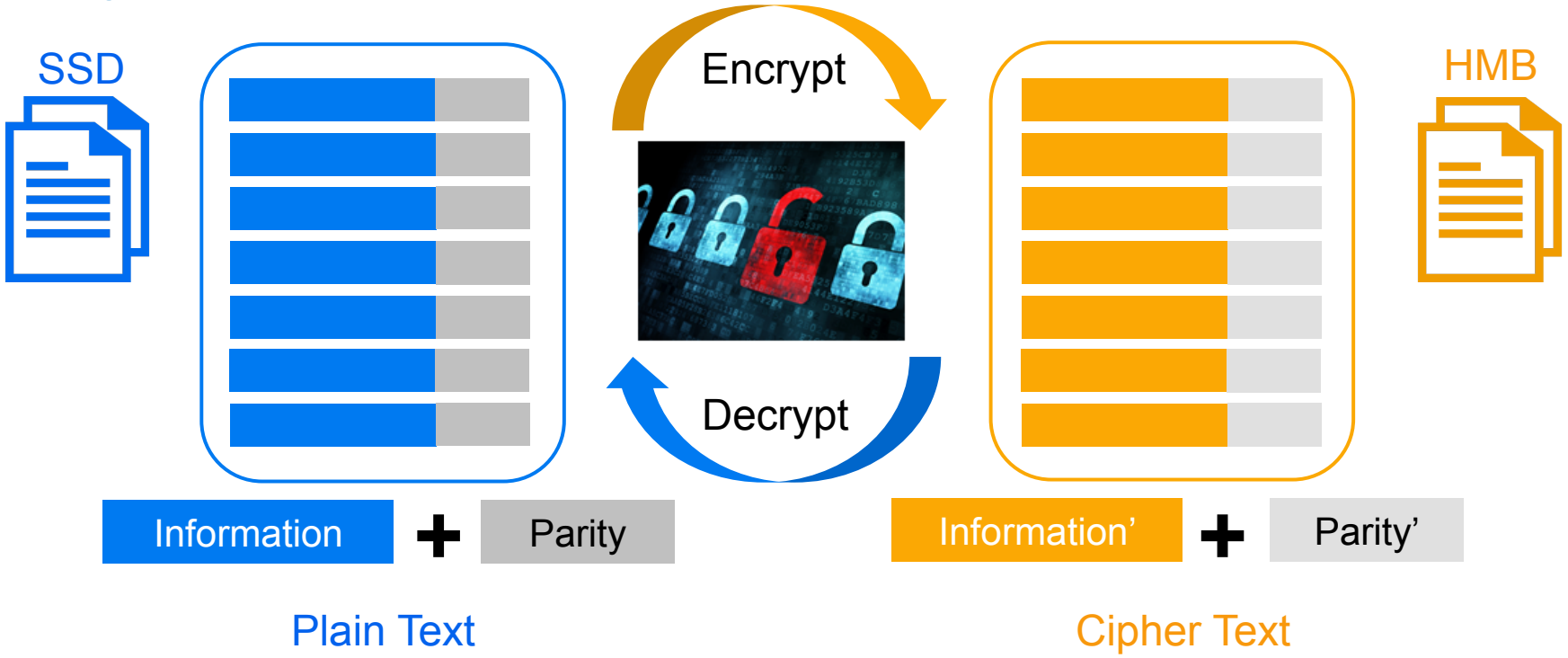
- Can we 100% trust the contents in HMB?
  - Ideally, YES; Practically, Be Careful
  - NVMe v1.2
    The controller shall ensure that there is no data loss or data corruption in the event of a surprise removal while the Host Memory Buffer feature is being utilized.



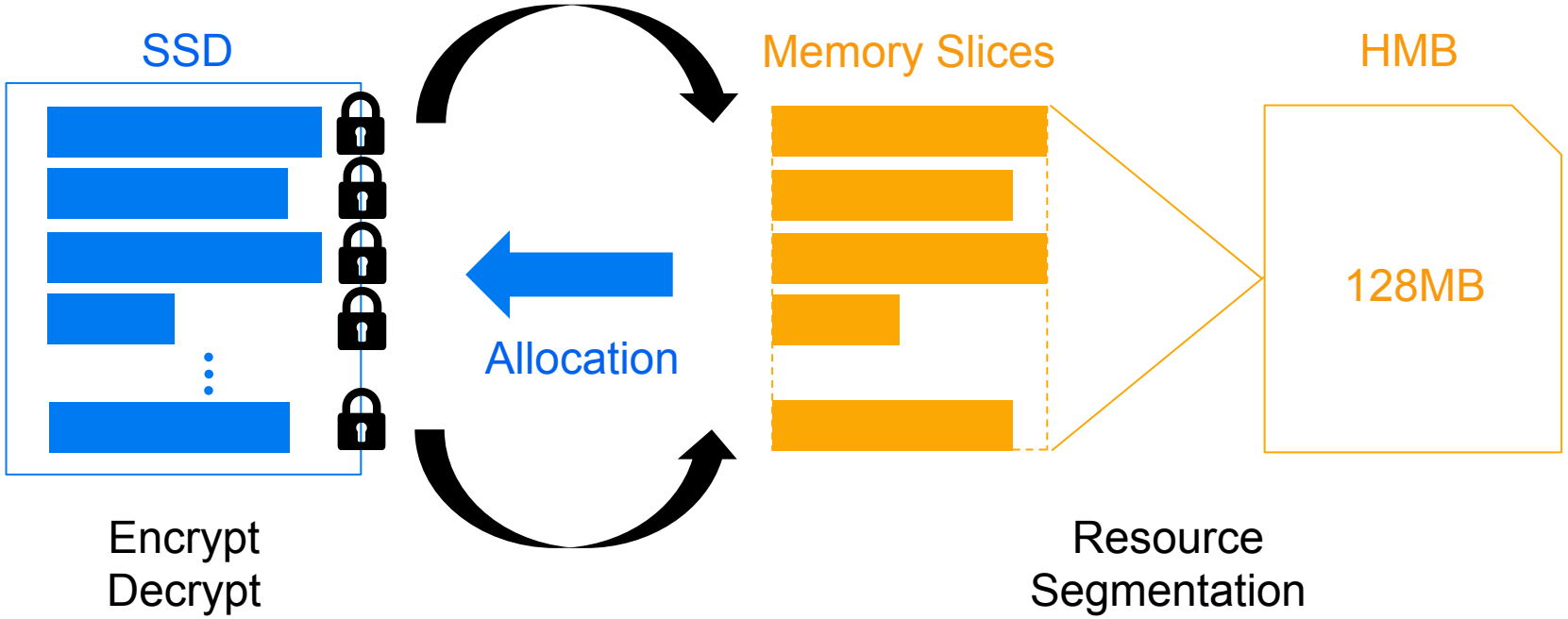
- ✓ Surprise Removal
- ✓ Unexpected Host Events
- ✓ Data Transmission Errors


Flash Memory Summit
End-to-End Data Path Protection
Buffer / Cache
Security
Flash Controller
Flash Memory
Processor
PCIe Controller
Submission Queue
Completion Queue
Exclusive for SSD

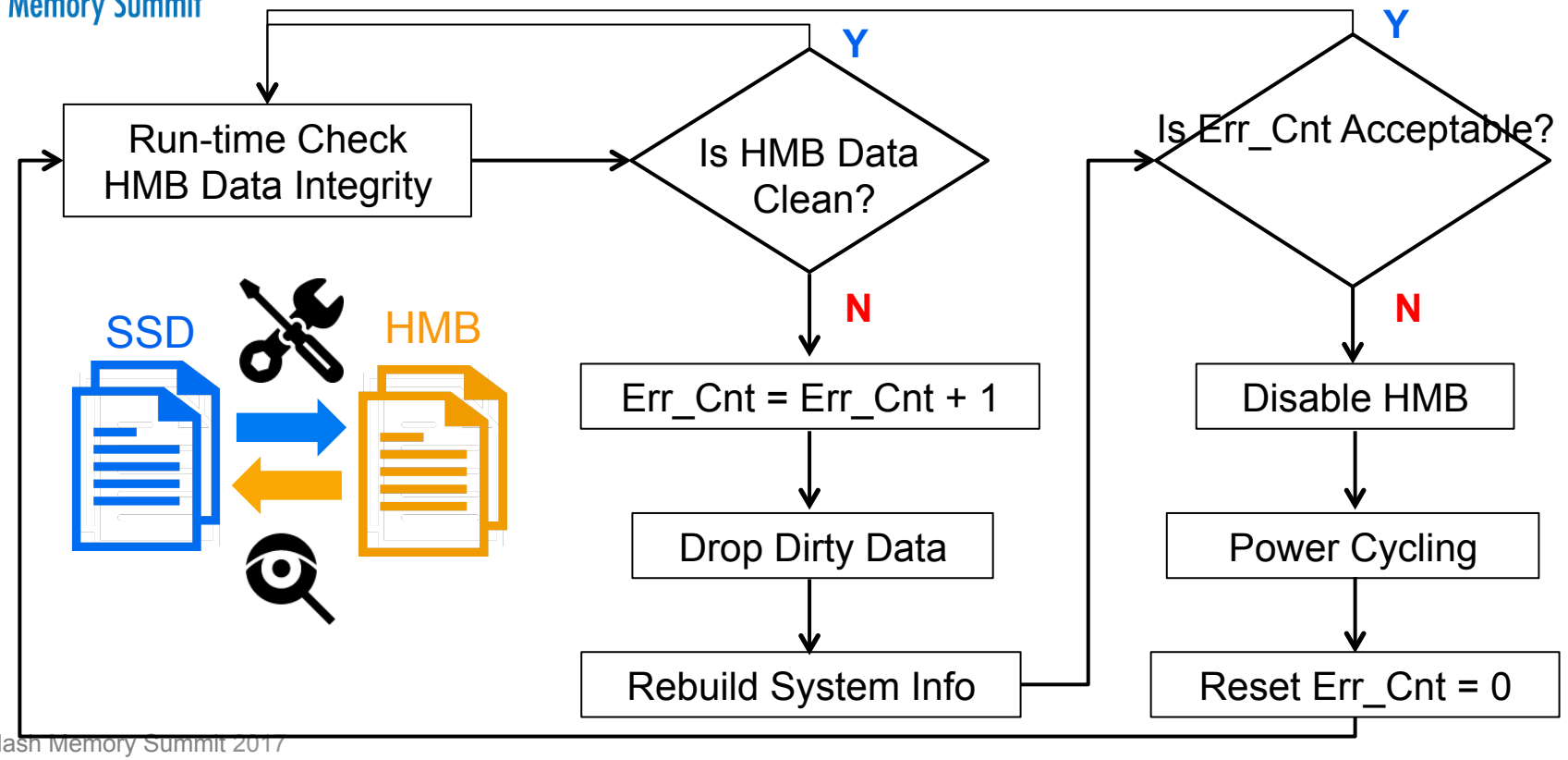
Error Detection and Data Protection



Multi-Level HMB Data Protection



Error Handling Flow



Key Takeaways

- HMB is a key feature to increase the performance as well as the market share of DRAM-L SSD in PCIe SSD product line
- DRAM-L SSD supporting HMB is suggested to be able to accommodate with different RAM sizes shared by host
- Flash Translation Table Management is the key of DRAM-L SSD performance, especially with HMB support
- E2EDPP is suggested to extend for covering HMB data path

Brand New PCIe SSD Solution

- PCIe Gen3 x2
- NVMe / AHCI
- DRAM-L
- Host Memory Buffer
- StrongECC™
- SmartECC™
- OPAL 2.0
- Low Power Management
- Flexible Flash Support
- Seq. R/W: 1600/1100 (MB/s)

Visit PHISON at Booth #614

DRAM-Less
1113 / 1620
Up to 256GB

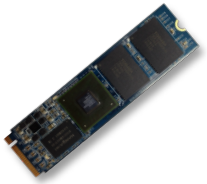
PCIe BGA SSD

DRAM-less
22x30

DRAM
22x42

Up to 512GB

M.2 2230 M.2 2242



DRAM
22x80 mm²
Up to 1024GB

M.2 2280

DRAM-Less
Up to 512GB

CFX™

Thank You!