Microsemi

SSD Lifetime Extension Using Multi-Code-Rate LDPC with Multi-Dimensional LLR Tables

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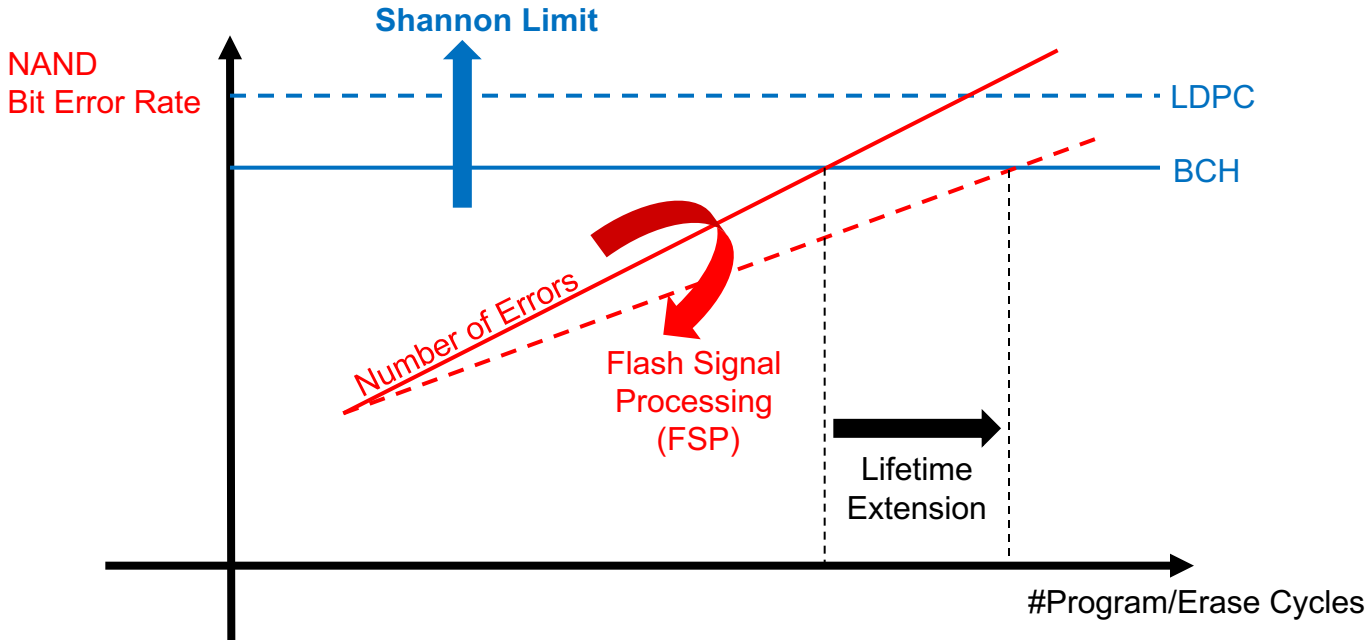
Flash Memories Wear Out

- NAND flash memories wear out: in other words, the NAND bit error rate is a function of the number of program/erase cycles
- Error correction codes and flash signal processing can extend NAND's lifetime and, therefore, SSD's lifetime
- LDPC can recover more errors than BCH by leveraging soft decoding

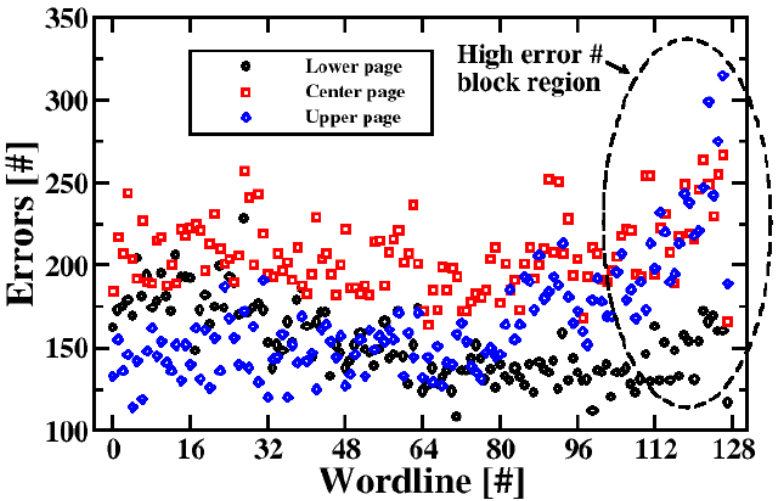
ECC and FSP



- Error Correction Codes and Flash Signal Processing can extend the number of Program/Erase cycles

TLC Pages

- Not all TLC pages exhibit the same BER
- With 3D architectures, there is also a dependency of the NAND raw BER from the layer number



C. Zambelli et al., IRPS 2017

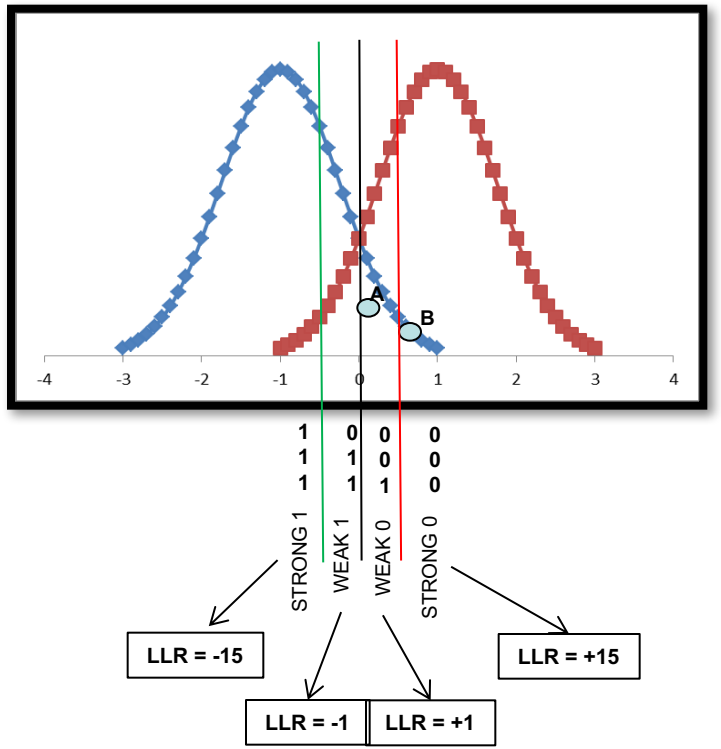
Multi-Code-Rate ECC

- Code Rate = User Data / (User Data + Parity)
- A lower CR means more Parity, i.e. less useful memory area to store User Data
- Average CR = $(CR_{LOWER} + CR_{CENTER} + CR_{UPPER})/3$
- A Flash Controller supporting multiple Code Rates is critical to maximize the storage area, because it allows reducing the Average CR

LDPC and LLRs

- LDPC can use soft decoding
- Point A is more likely to be in error than point B
- Soft LDPC uses LLRs to measure reliability

$$L(u_i) = \log\left[\frac{P(u_i = 0 \mid y)}{P(u_i = 1 \mid y)}\right]$$



LLR Values During Life

- As LLRs measure the reliability of the information read from the NAND, their values change as a function of:
  - Number of program/erase cycles
  - Retention time
  - Number of read cycles
- The “quality” of LLR values impacts LDPC correction performances

Multiple LLR Tables

- LLR values are stored in Tables
- There is a Table per reference voltage
- As LLR values change during NAND's life, multi-dimensional Tables are required: these tables must be stored and properly addressed without time penalties, especially in enterprise applications
- Number of Program/Erase Cycles, Number of Read Cycles, and Retention Time can be viewed as "additional" dimensions

Summary

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- NAND raw BER is not uniform across TLC pages and 3D layers, and this will become even worse with QLC storage
- A Flash Controller supporting multiple Code Rates is critical to maximize the storage area in the 3D NAND era
- Lifetime of NAND can be extended using Soft LDPC and thus LLR Tables which change dynamically as the NAND ages
- Flash Controllers capable of supporting multiple Code Rates and multiple LLR Tables in the same drive can simultaneously maximize 3D SSD's lifetime and User storage area