ECC Approach for Correcting Errors Not Handled by RAID Recovery

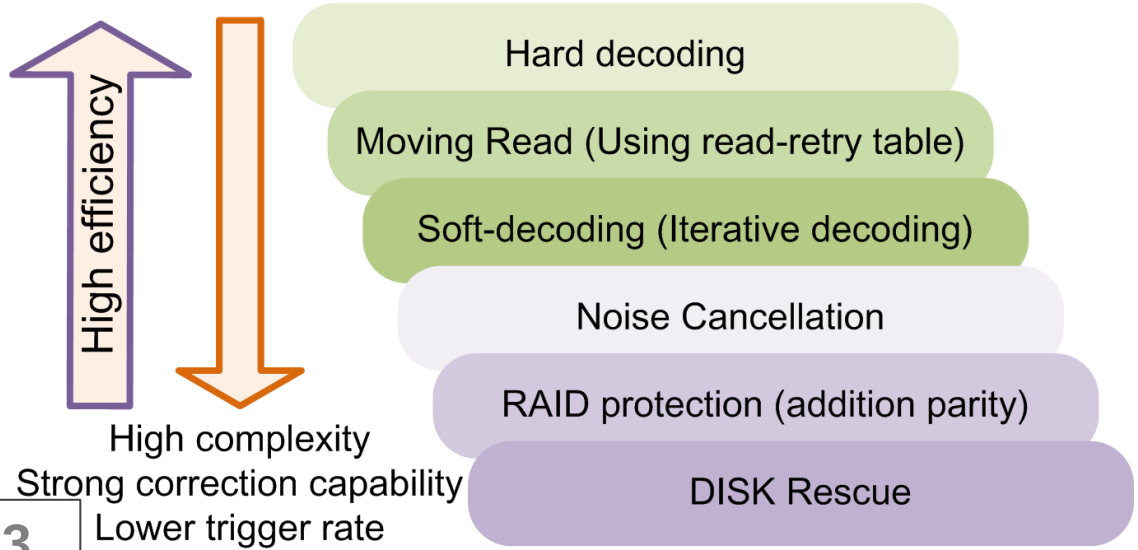
Jeff Yang

Siliconmotion

Note: All the material are the concept proof and simulation.s It is not the real Siliconmotion's fianl product.

Traditional Error recovery flow

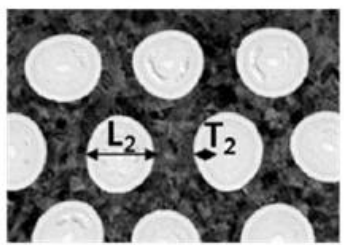
Error recovery flow

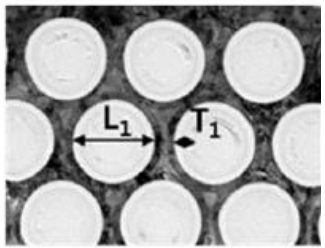


Flash Memory Summit 2013
Santa Clara, CA

3D NAND Challenges

- Each 3D generation will increase the layer number by 30~50%.
- High-aspect ratio channel hole etch.
- Cell current reduction is seriously concerned.
- Reduce the read-voltage to improve the read-count (degradation the read-disturbance) make cell current worse.
- Different cell characteristics for each WL. (program-speed, cell-to-cell interference, retention)
- Poor retention characteristics.





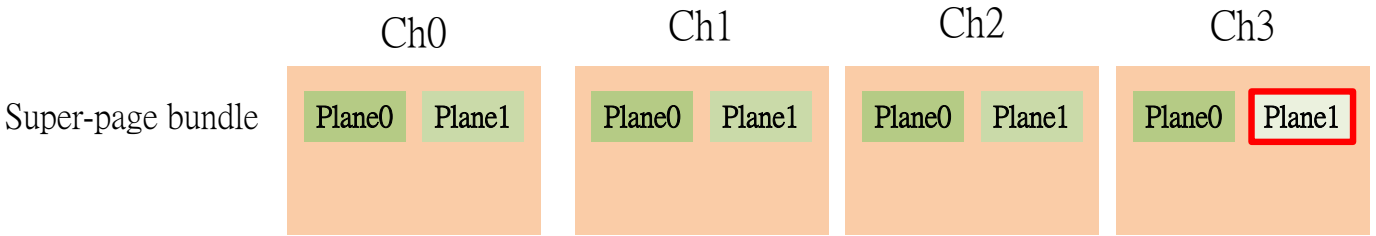
Not easy to screen out some defects

Especially on bit-column related defect.

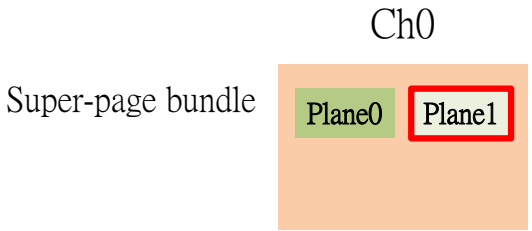
Ref: Evolution of NAND flash memory: from 2D to 3D… 2017 IMW

RAID is good, but….

- Put the data from the same failure range into the different RAID protection group.
- Add more write overhead, because the additional parity will be written.
- If the failure range cross the block, a plan based protection range is needed.

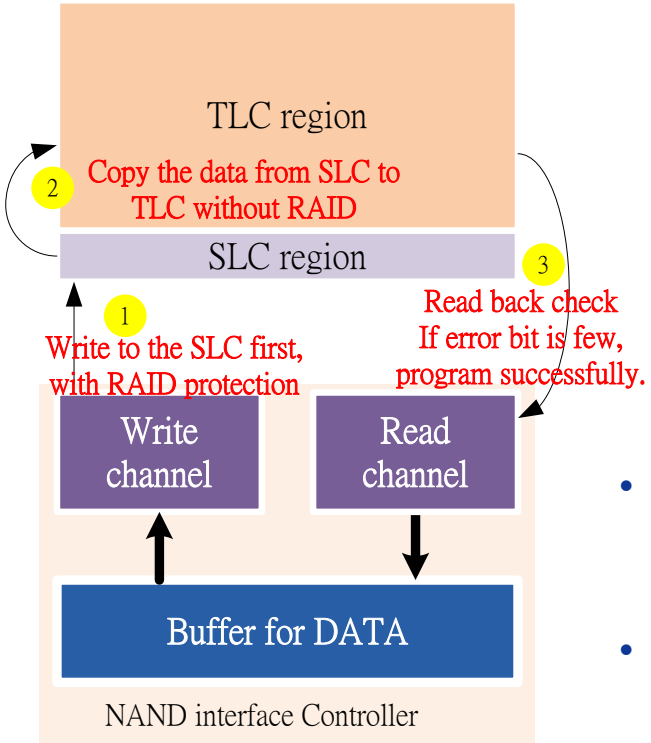


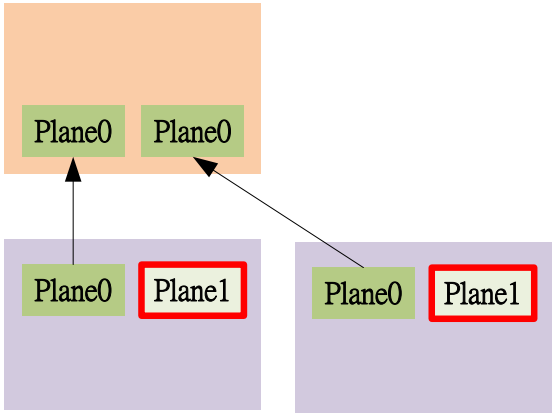
12.5% overhead



50% overhead in single chip applications

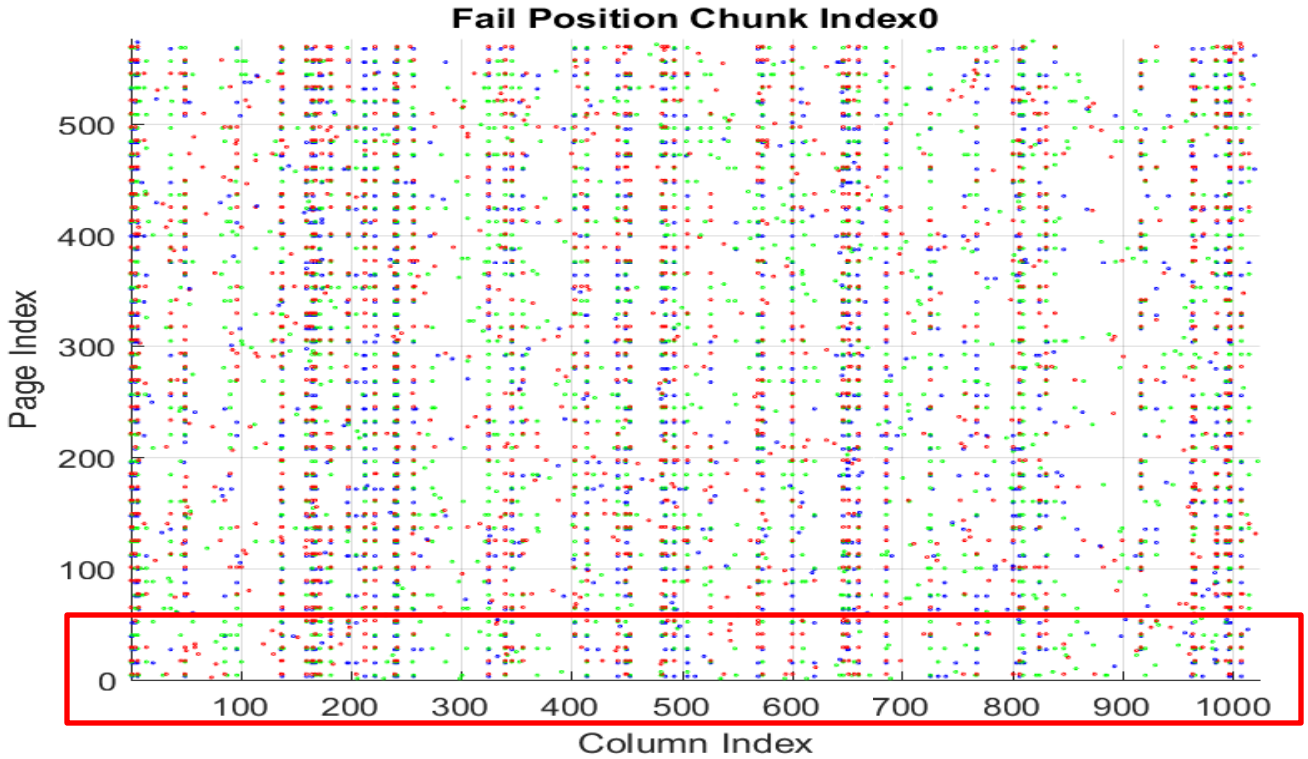
A read back verify scheme



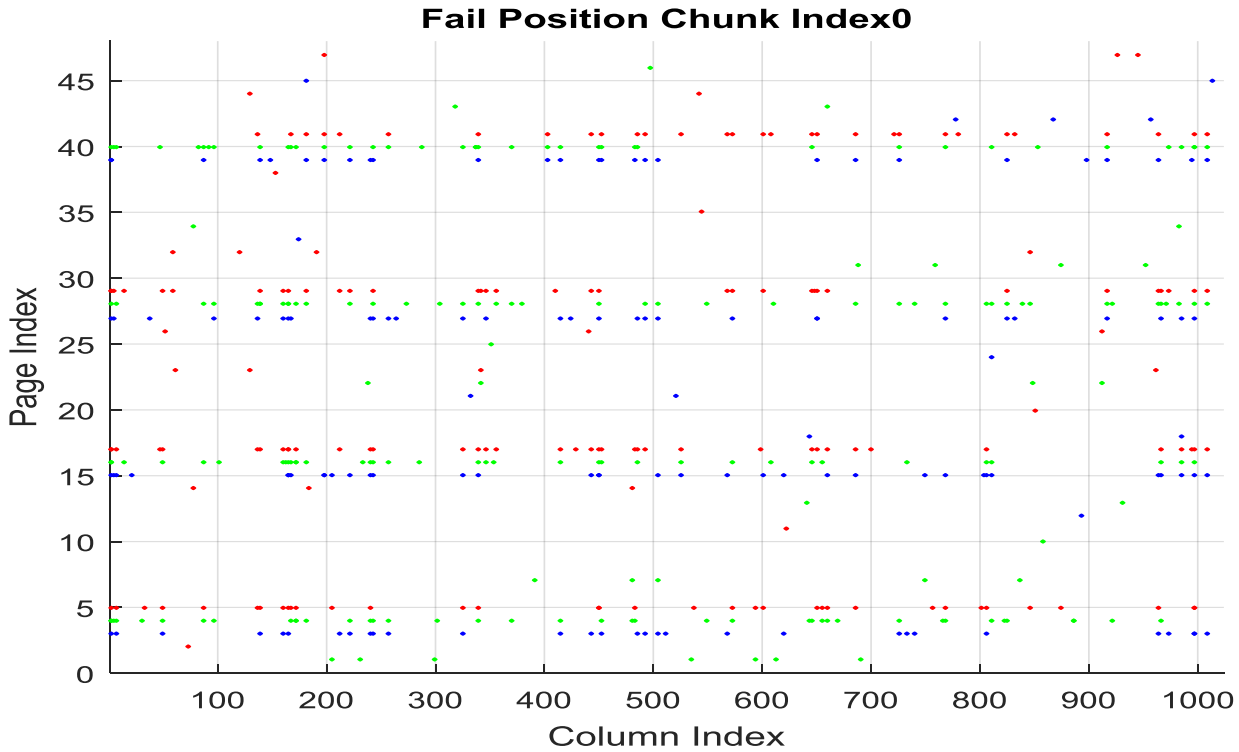


- The SLC to TLC internal copy will be use to accelerate the write performance and power saving. (cause some random error bit.)
- If the TLC write complete, there is still a probability on TLC read fail from read-disturbance, X-temp, or Data-retention.

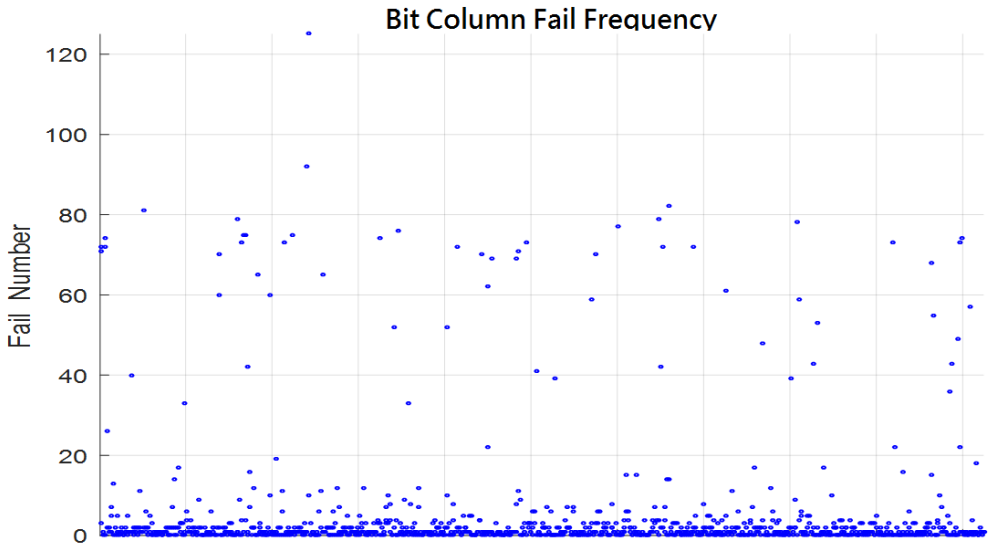
Bit column related Failure



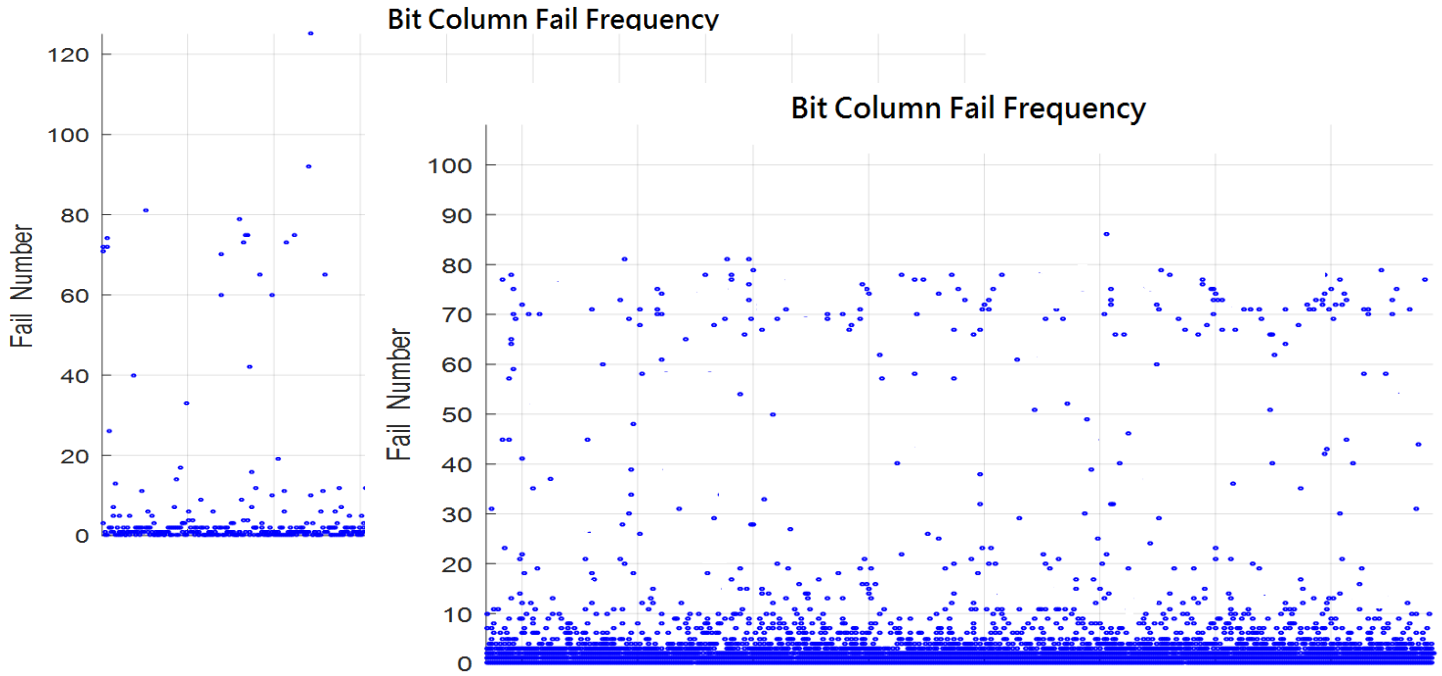
Bit column related Failure(Zoom-in)



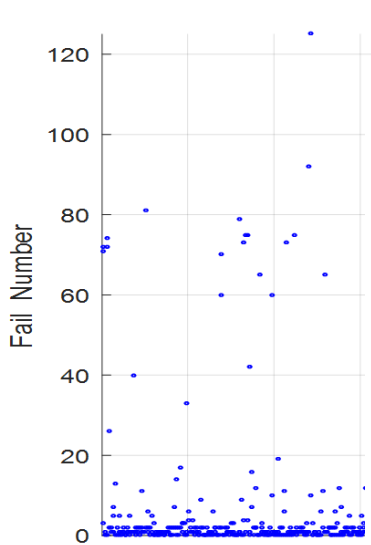
Column fail after Low P/E cycle

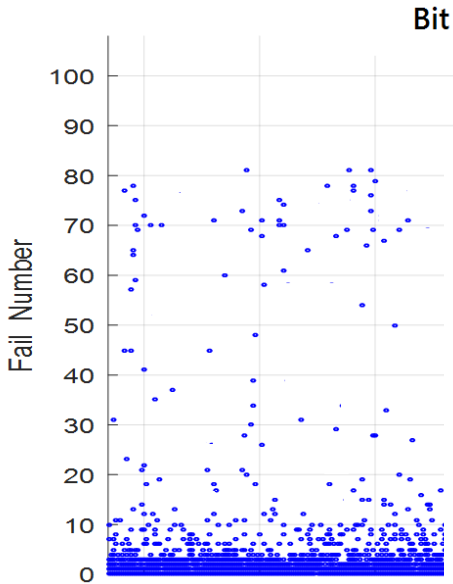


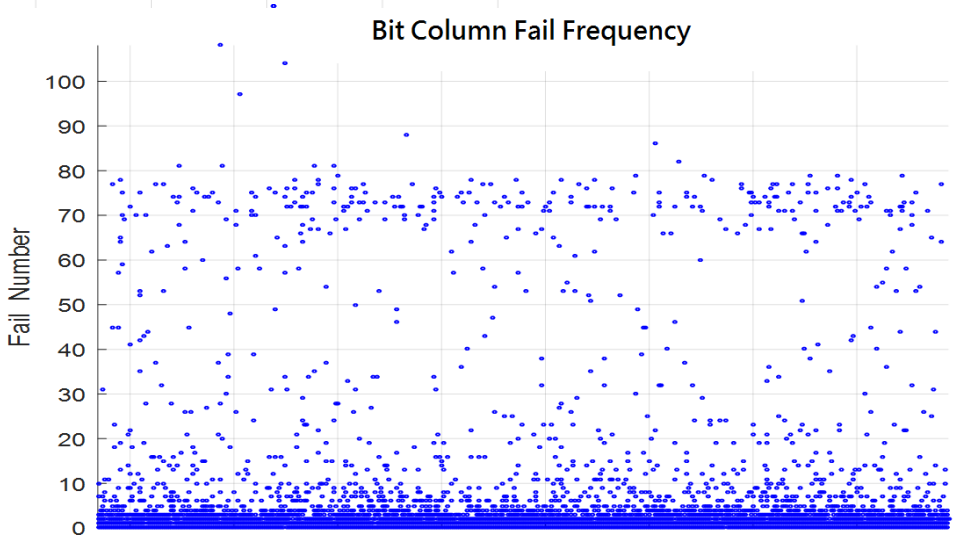
Column fail after median P/E cycle



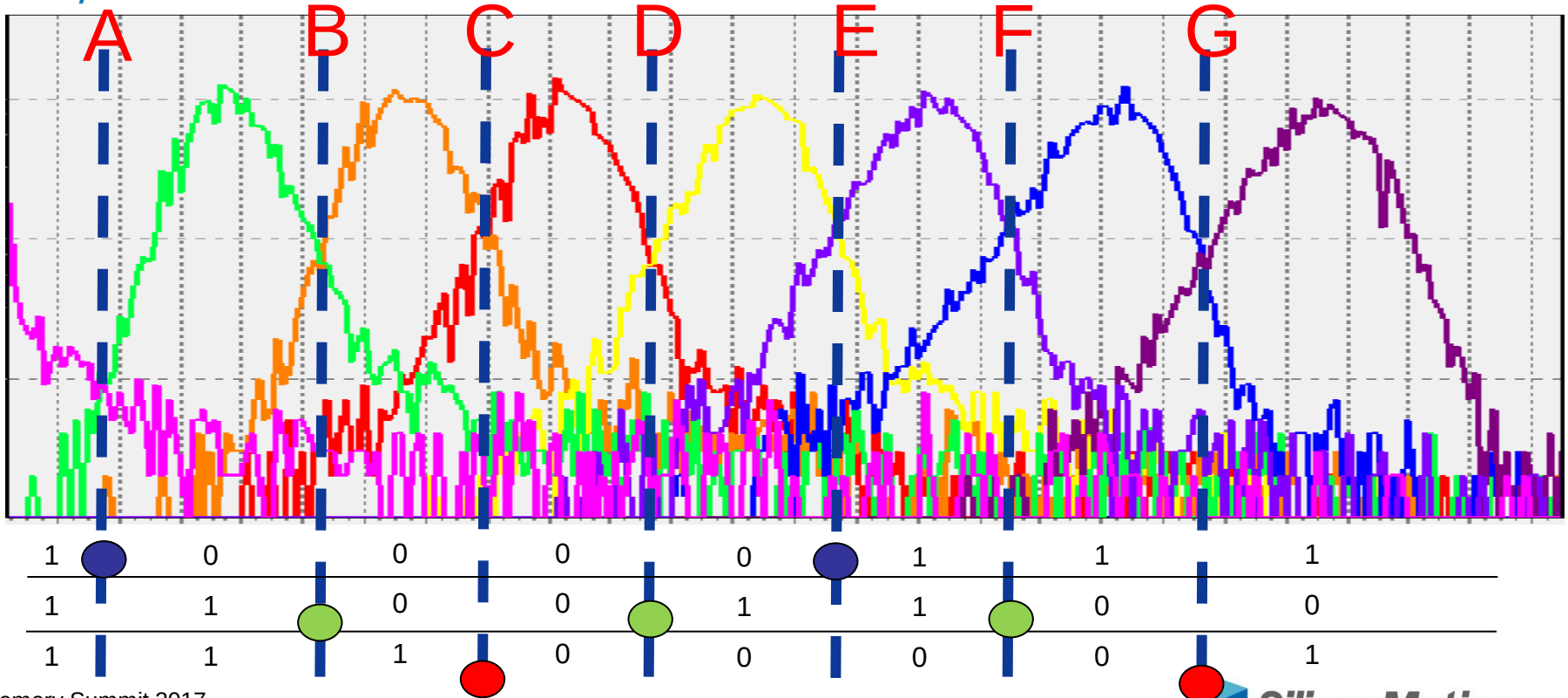
Column fail after high P/E cycle



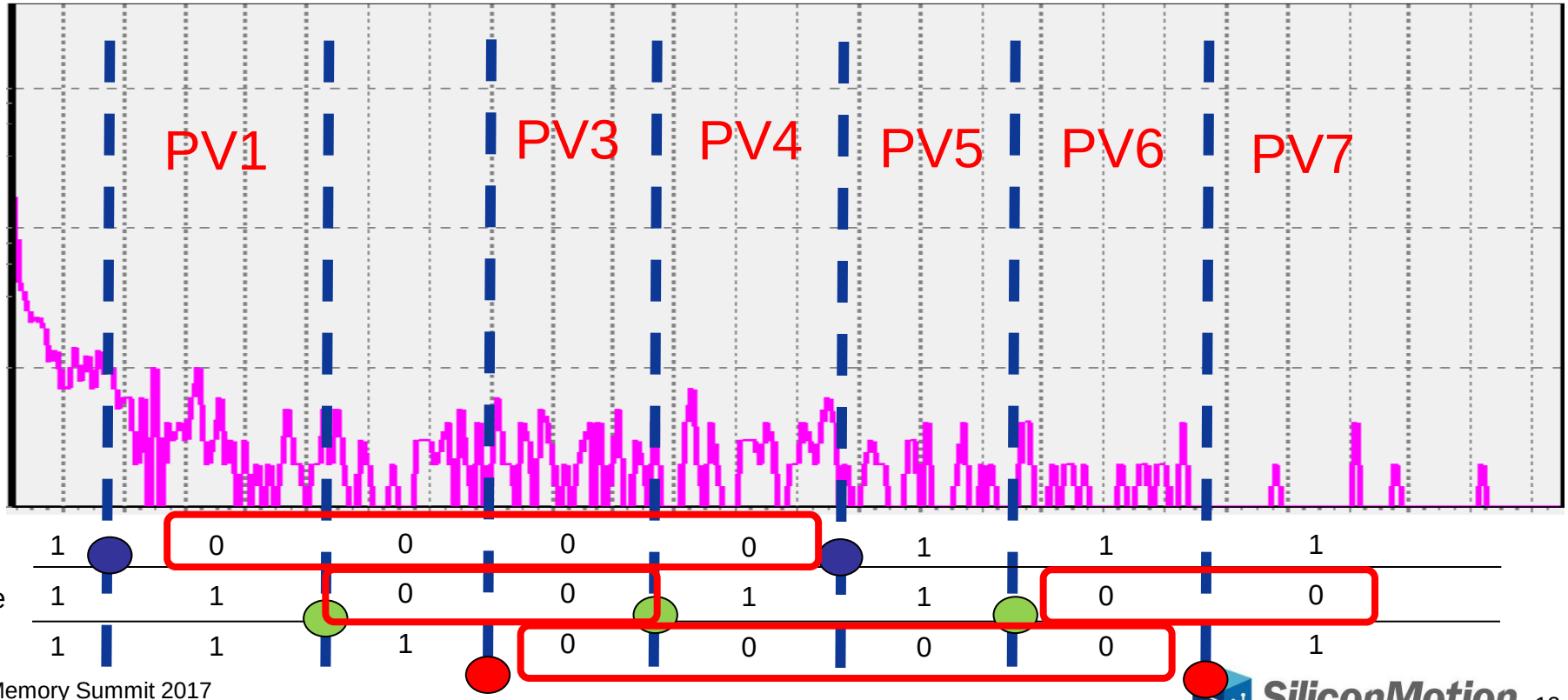




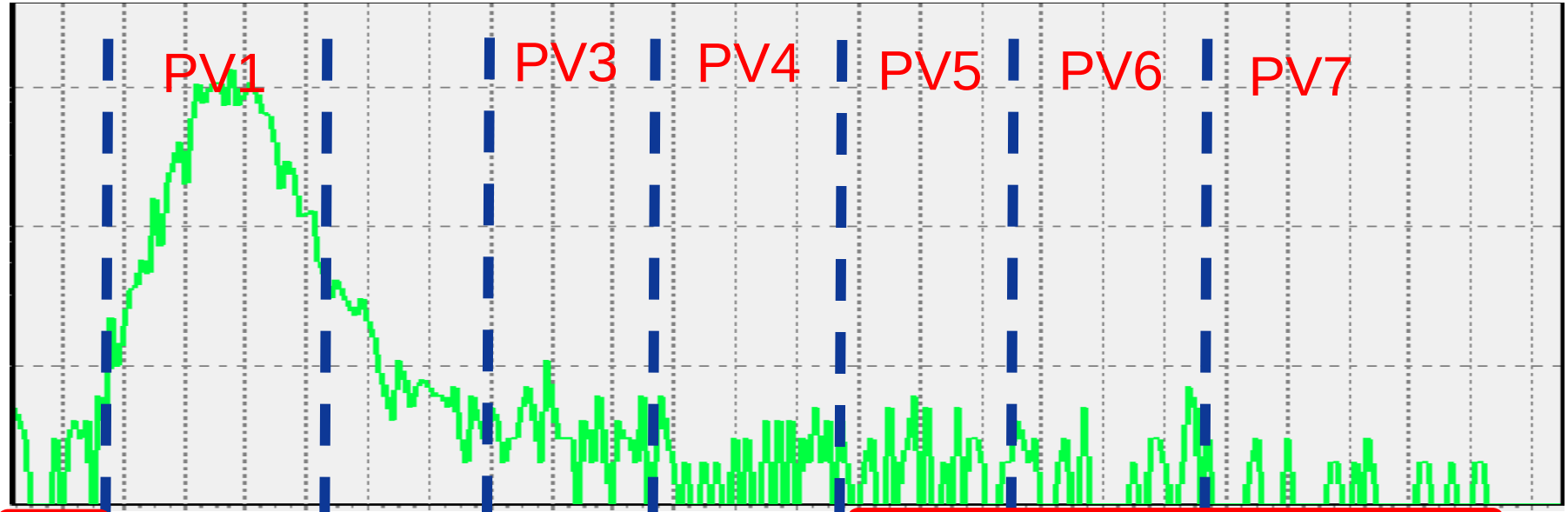
Vth plot after the P/E cycle



Erase Vth plot after the P/E cycle

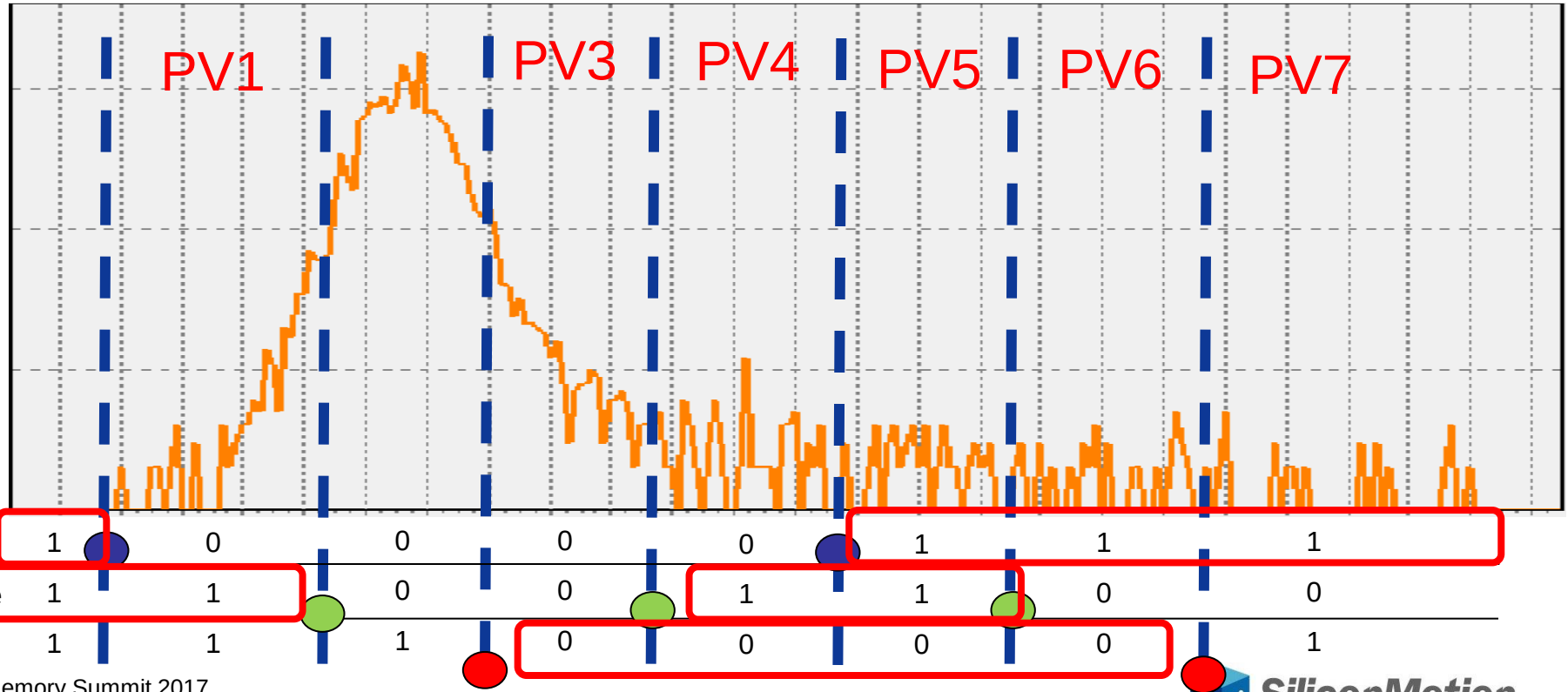


PV1 Vth plot after the P/E cycle

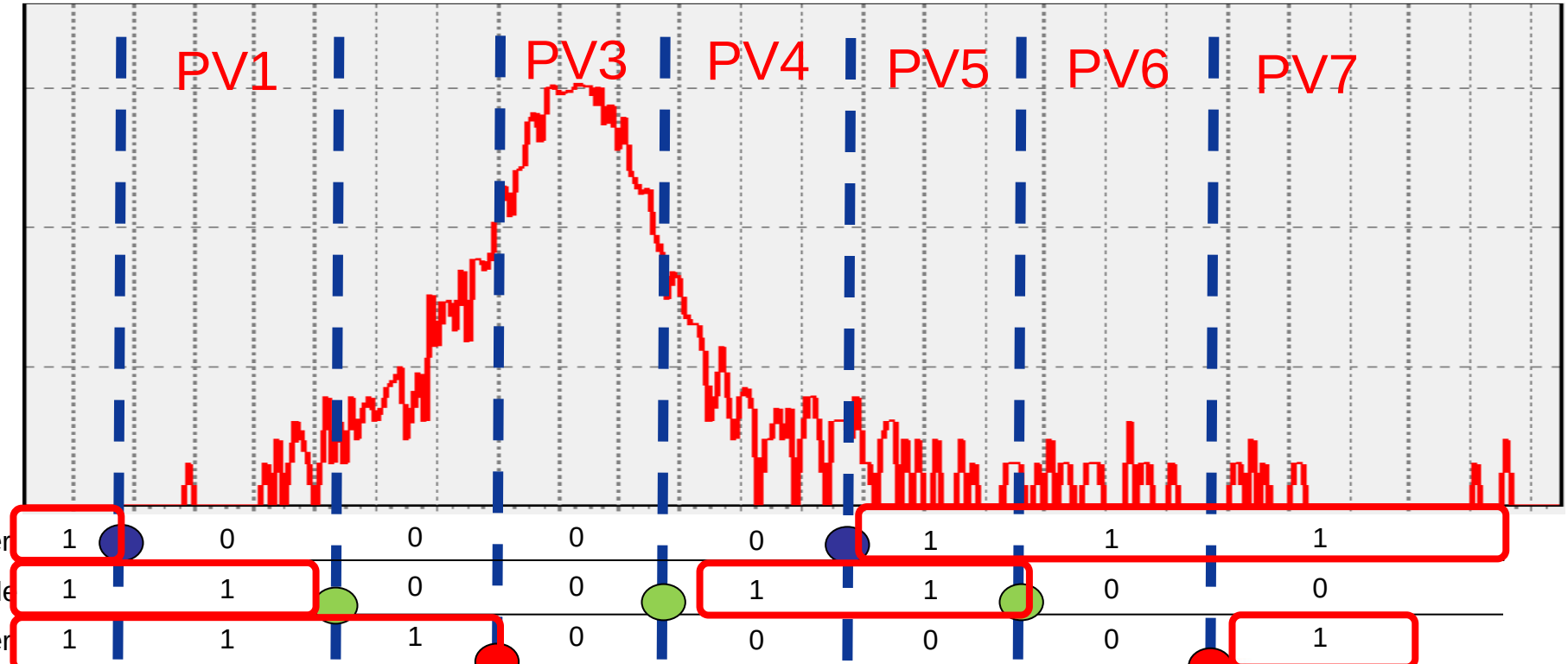


Lower	1	0	0	0	0	1	1	1
Middle	1	1	0	0	1	1	0	0
Upper	1	1	1	0	0	0	0	1

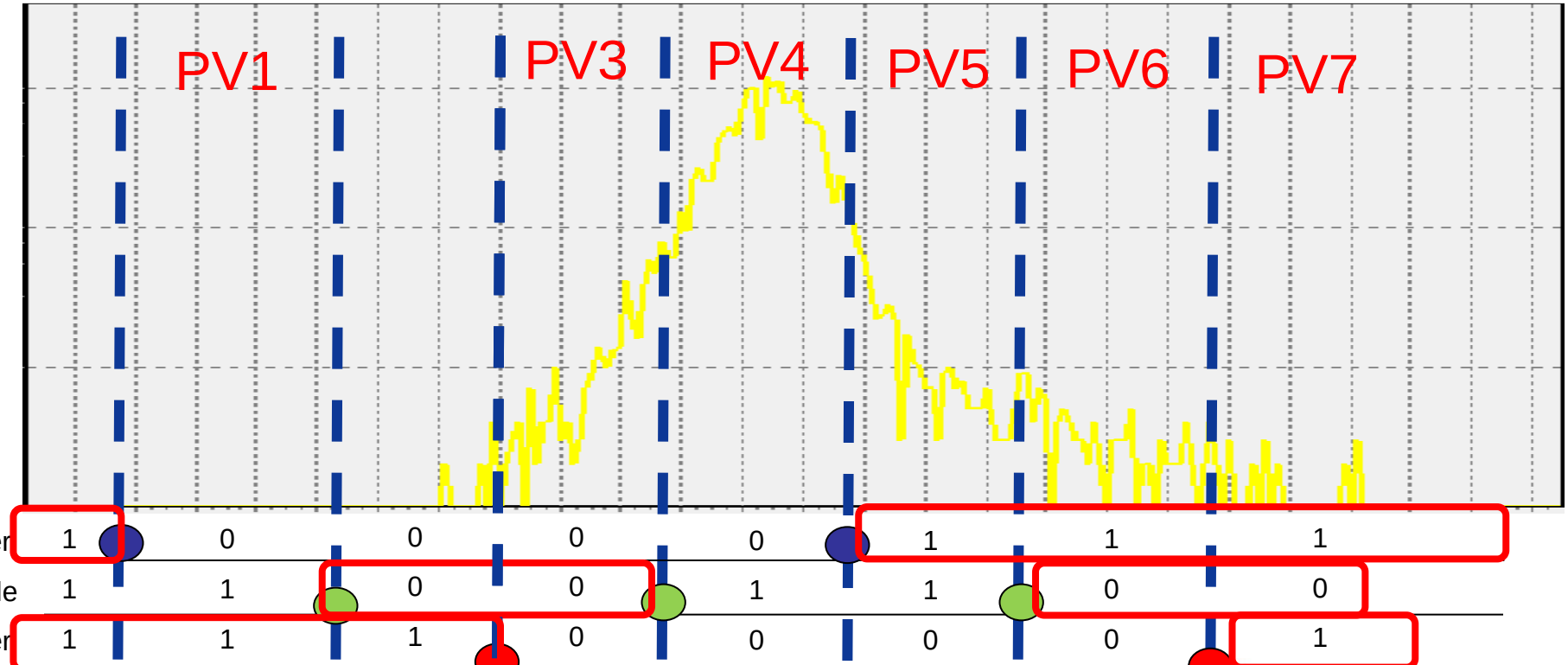
PV2 Vth plot after the P/E cycle



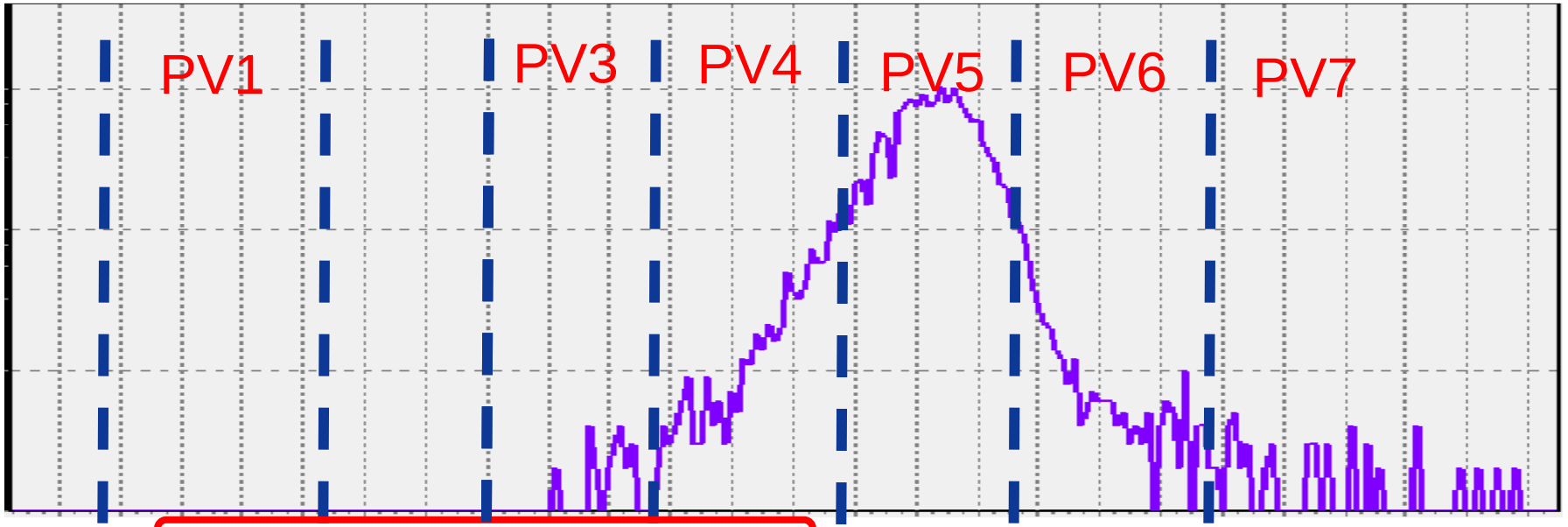
PV3 Vth plot after the P/E cycle



PV4 Vth plot after the P/E cycle

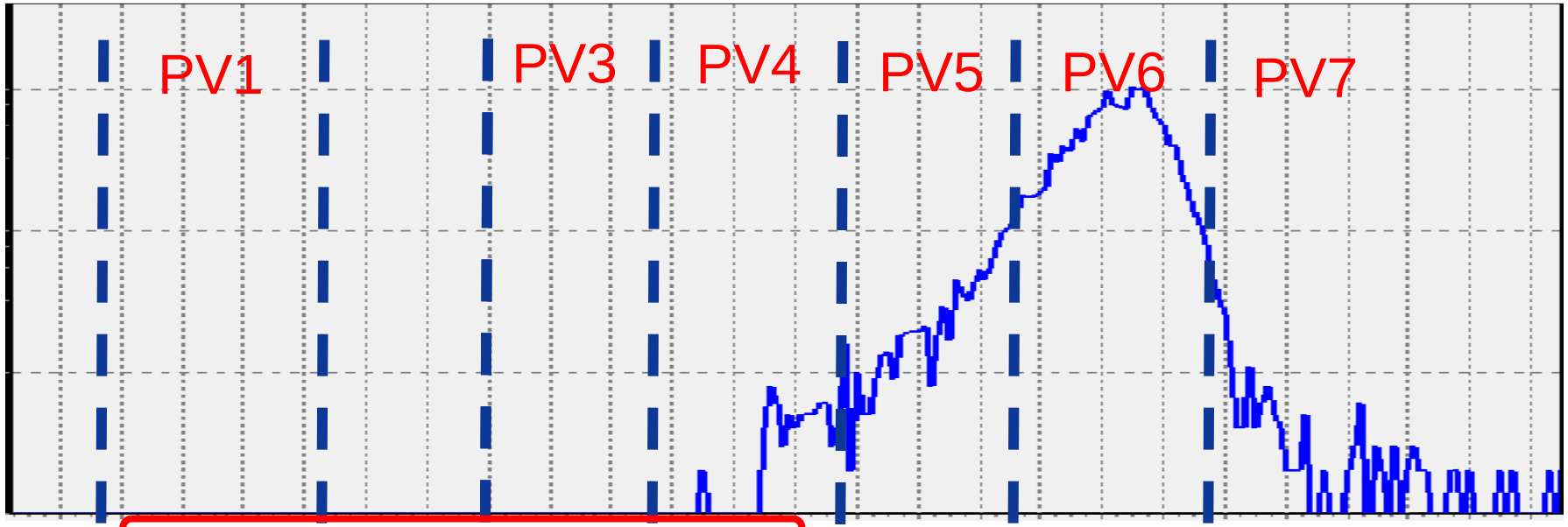


PV5 Vth plot after the P/E cycle



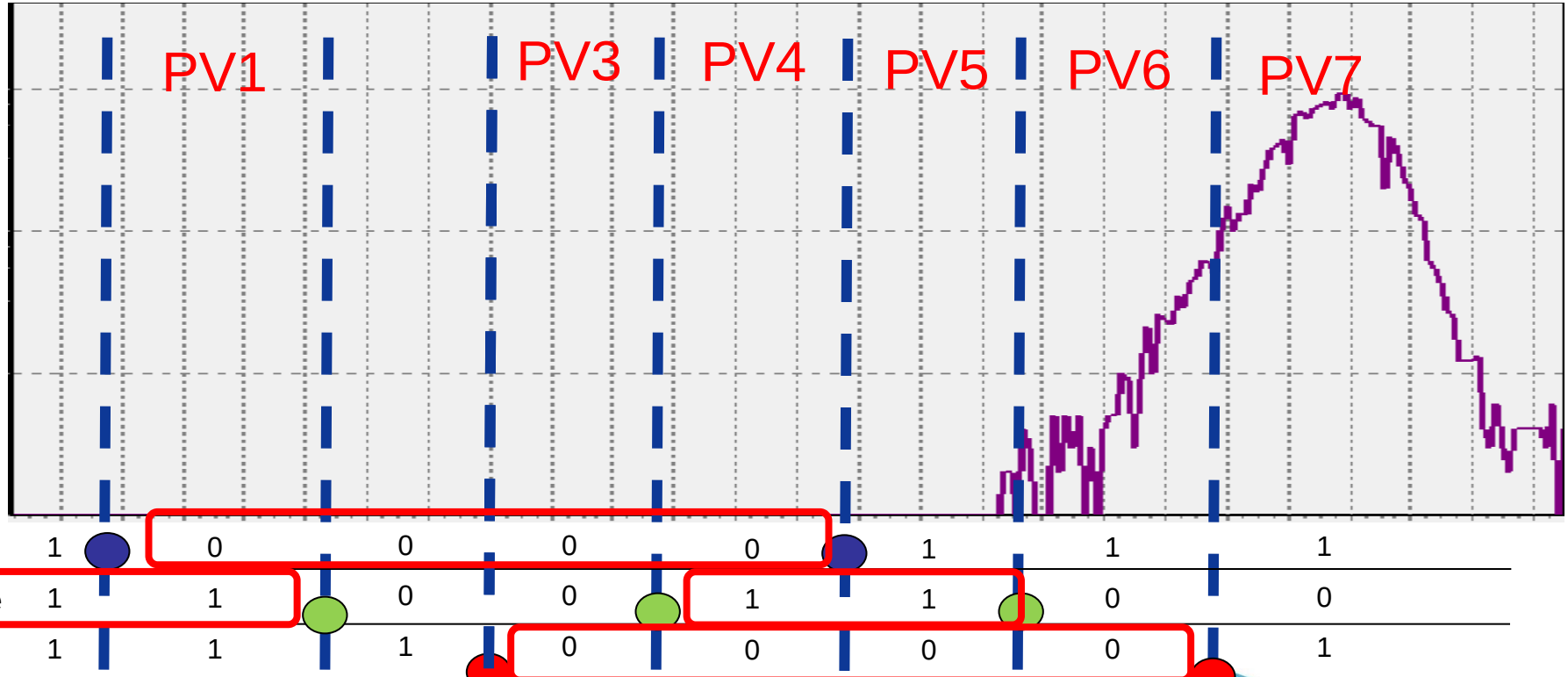
Lower	1	0	0	0	0	1	1	1
Middle	1	1	0	0	1	1	0	0
Upper	1	1	1	0	0	0	0	1

PV6 Vth plot after the P/E cycle



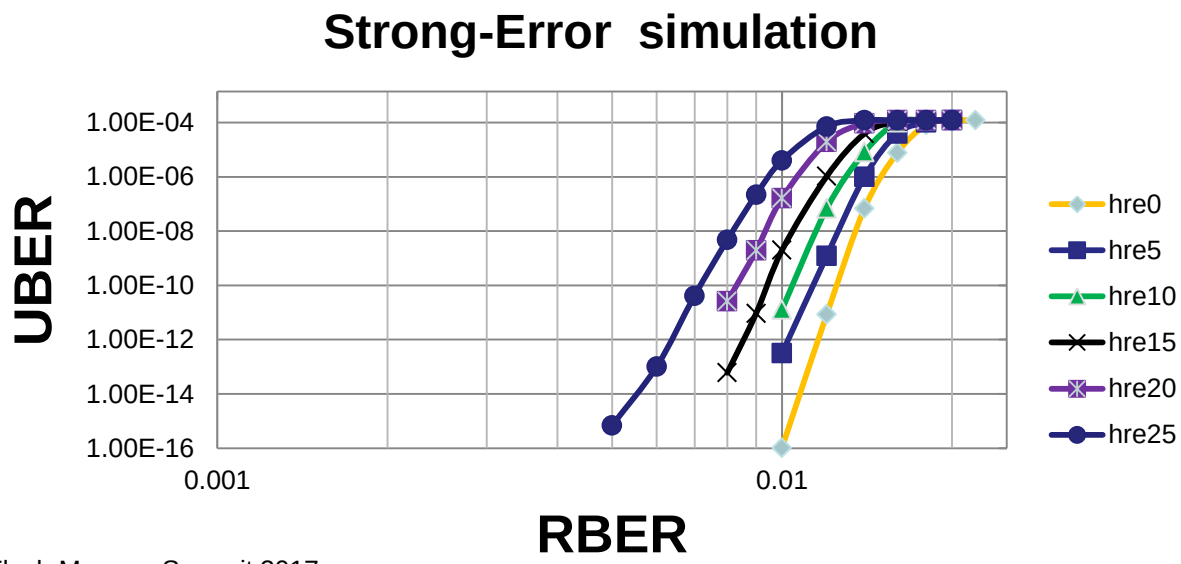
Lower	1	0	0	0	0	1	1	1
Middle	1	1	0	0	1	1	0	0
Upper	1	1	1	0	0	0	0	1

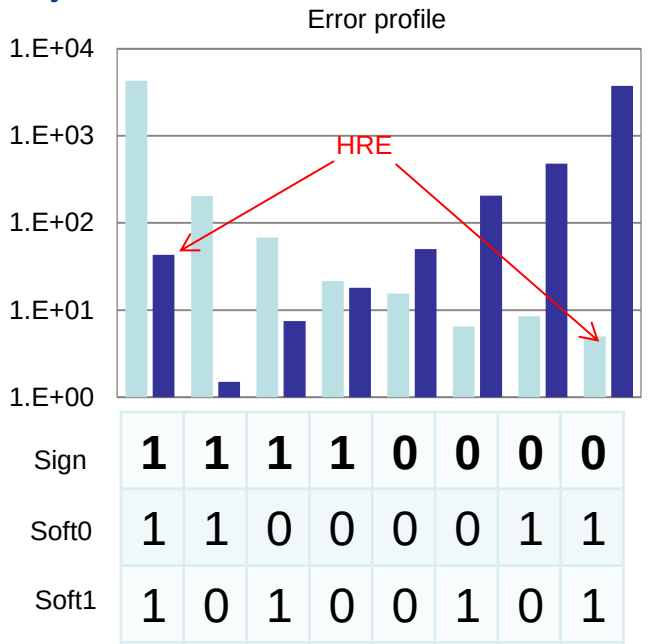
PV7 Vth plot after the P/E cycle



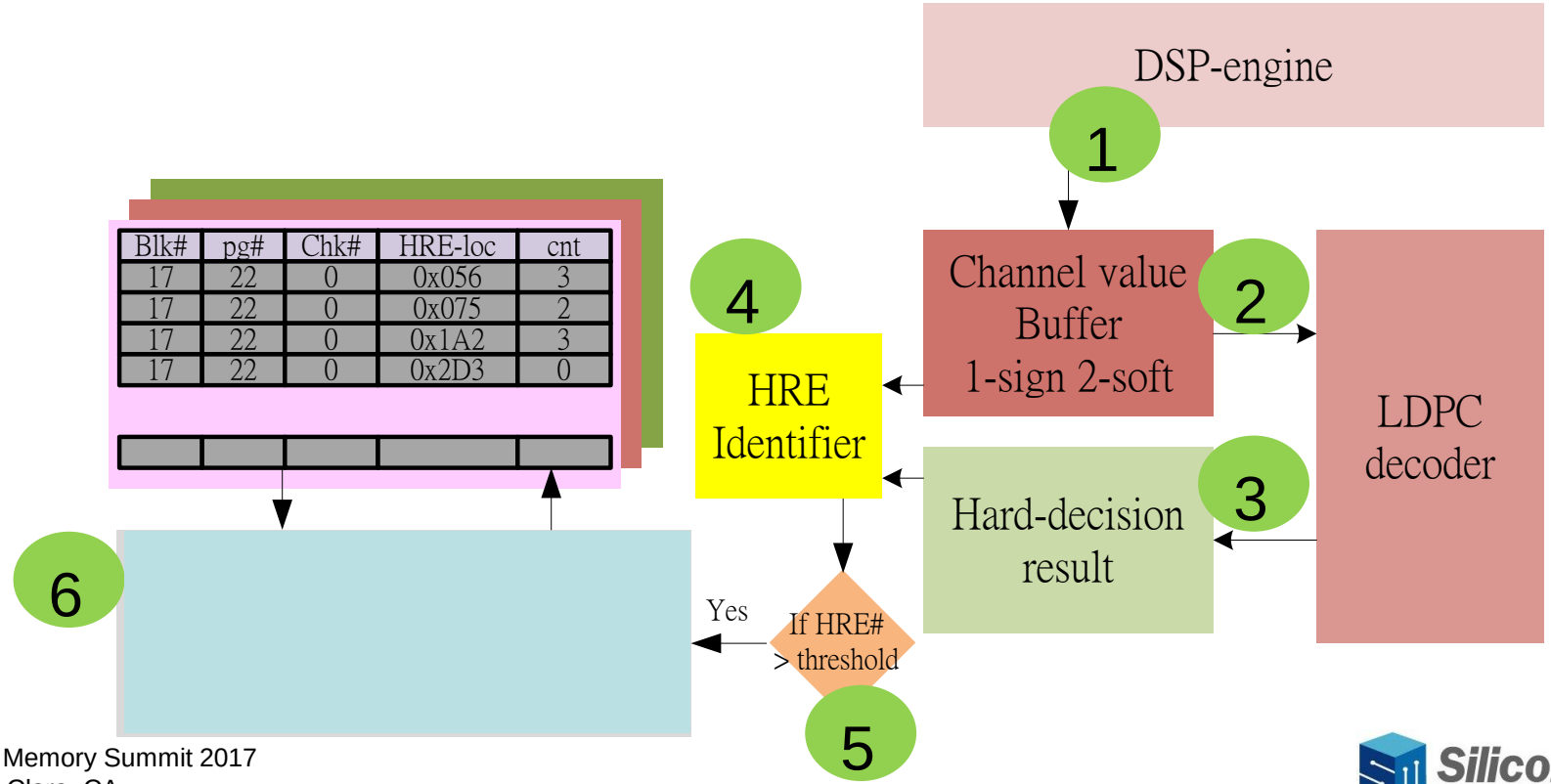
Soft-decoding vs. HRE

- These strong error(high reliability error, HRE) is grow with the P/E.
- HRE will dominate the LDPC engine's decoding capability.
- These kinds of HRE is predictable and recordable.

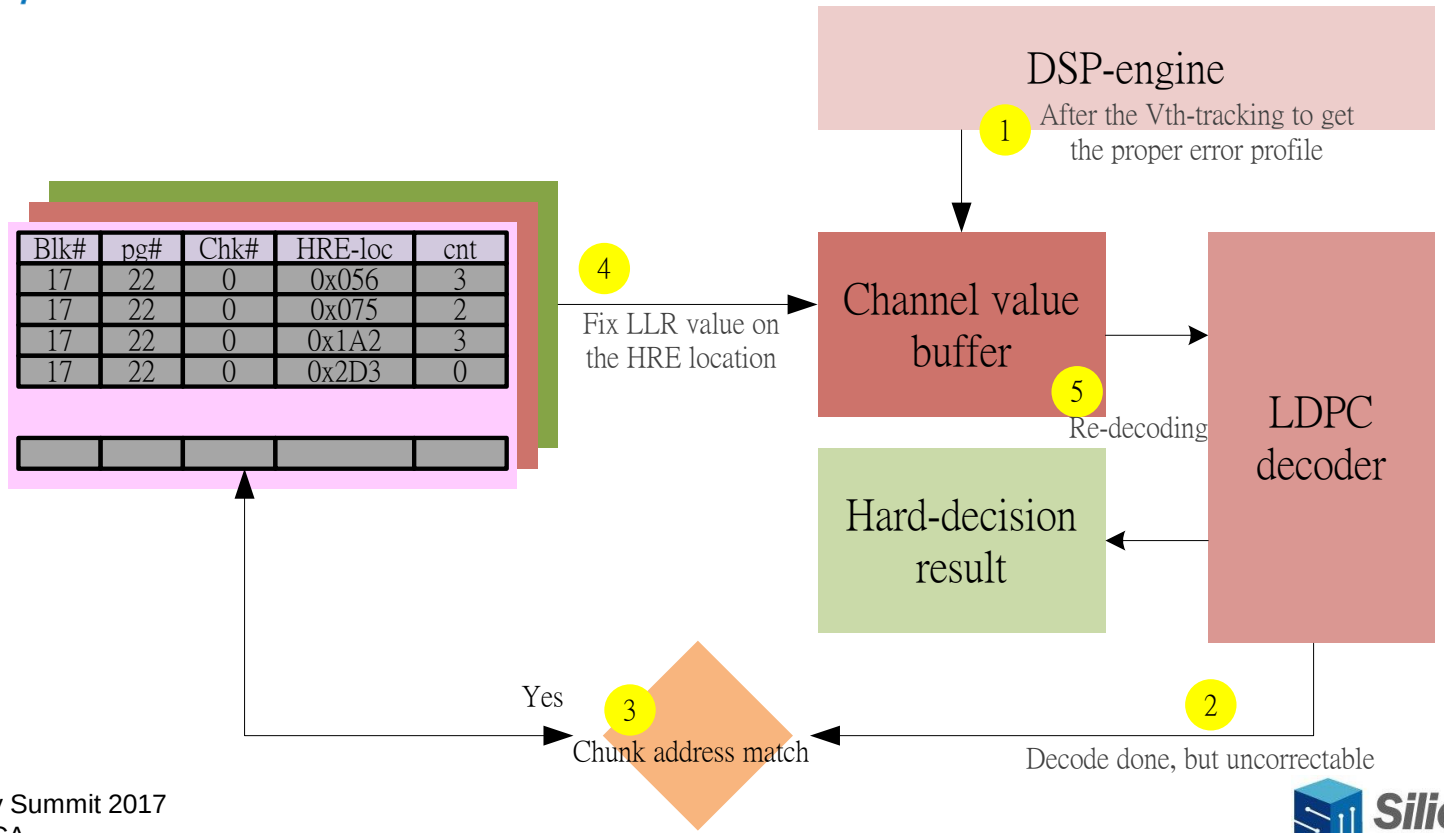




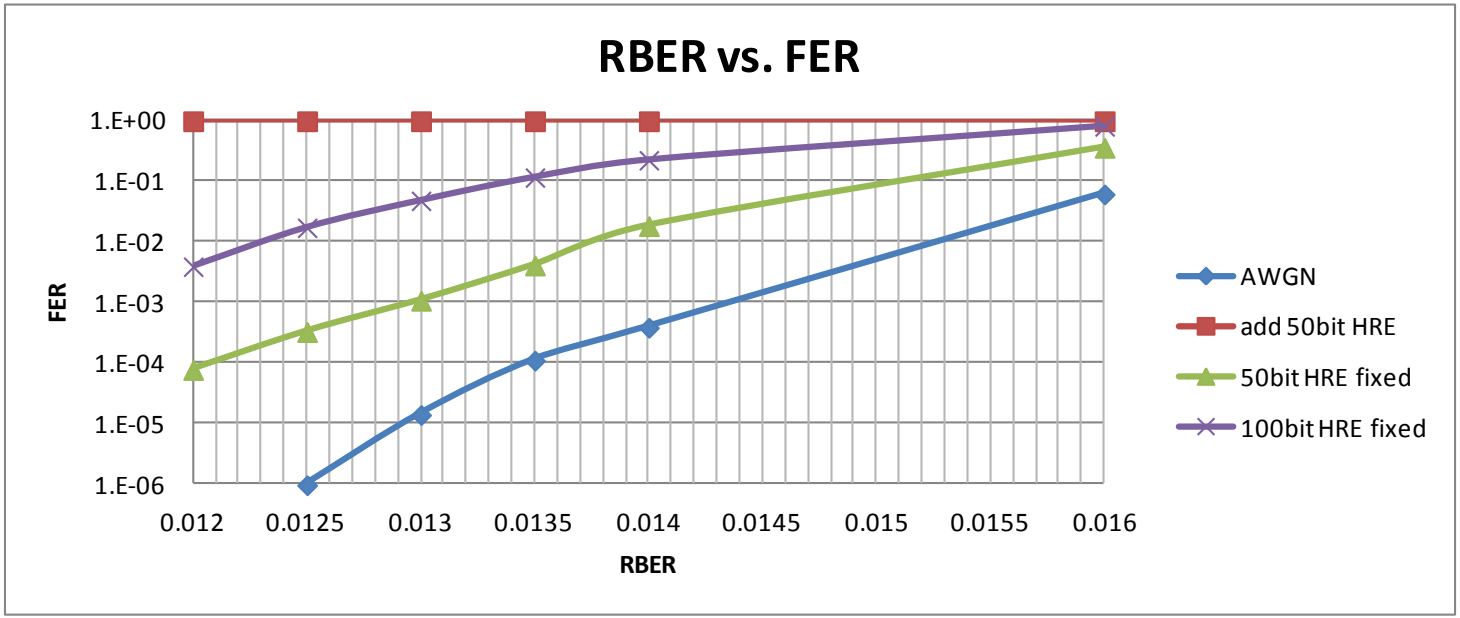
Caching system to record the high frequency HRE location



When HRE cause the Decoding fail

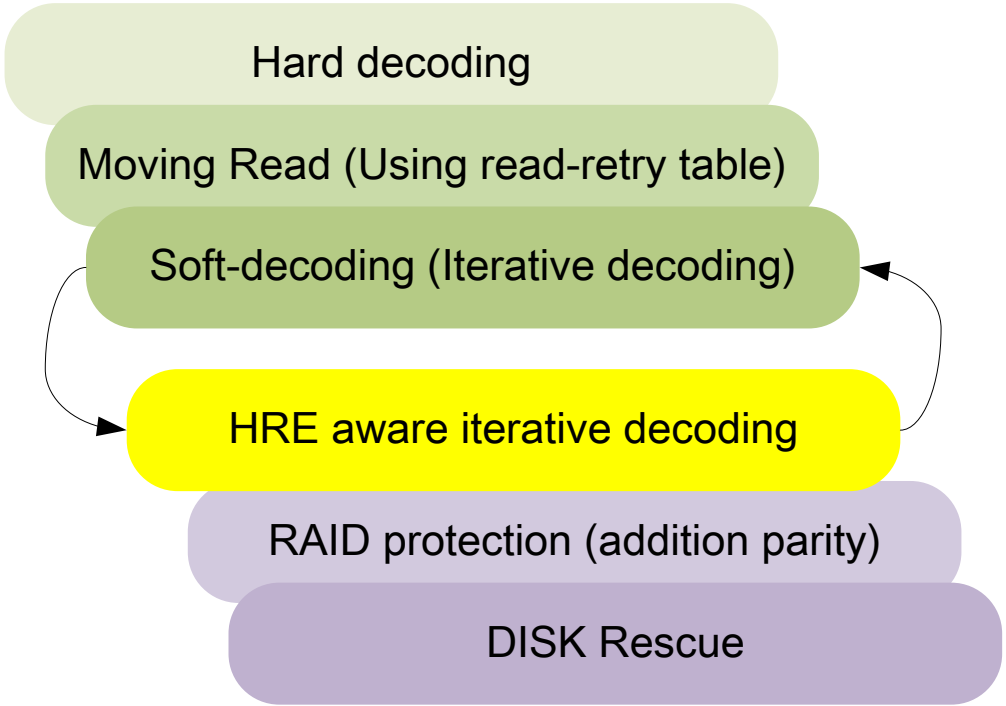


1KB LDPC simulation result



- The HRE location will be logged.
  - RBER= 1.25% with 50bit HRE: ~99.9% become correctable.
  - RBER =1.25% with 100bit HRE: ~98% become correctable.

HRE aware iterative decoding



Thanks

- Q&A
- Jeff.yang@siliconmotion.com