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Controller Technologies for Managing 3D NAND Flash Memories

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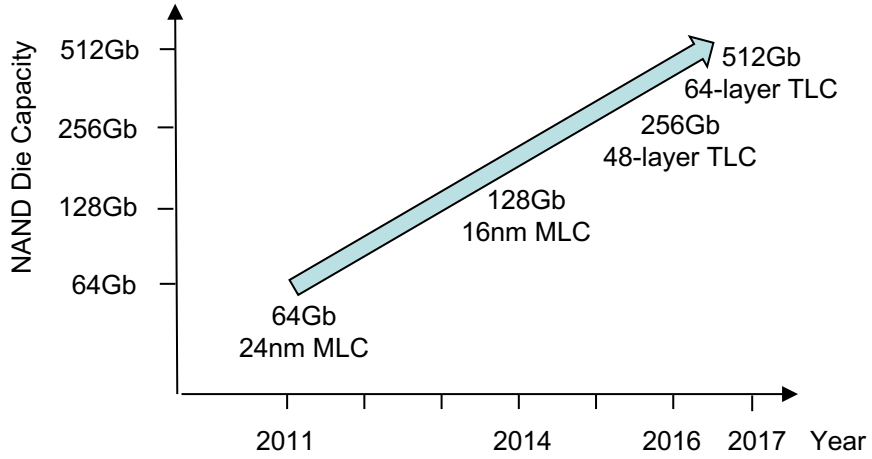
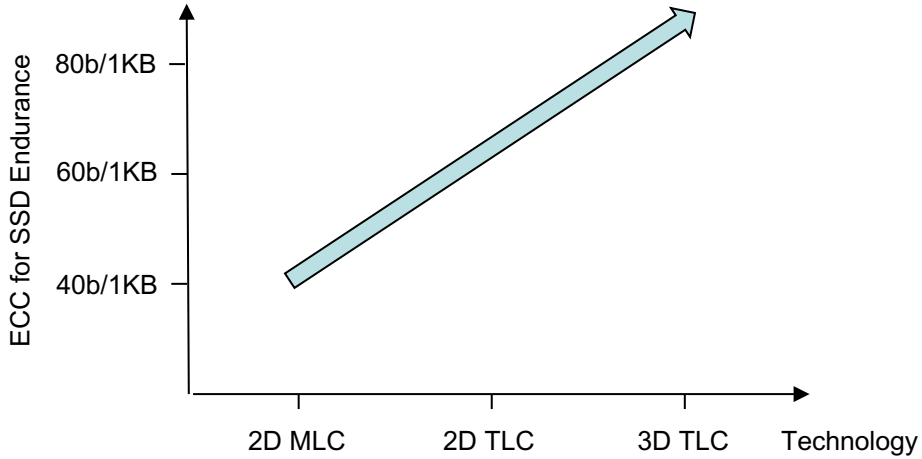
Outline

- 3D NAND Flash Scaling Trends
- 3D NAND Impairments and Mitigation Techniques
- Multi-Level Error Correction
- LDPC with Hard and Soft Decision Decoding
- Adaptive Code Rates
- Read Voltage Calibration
- Redundant Silicon Elements
- Summary

NAND Scaling Trends

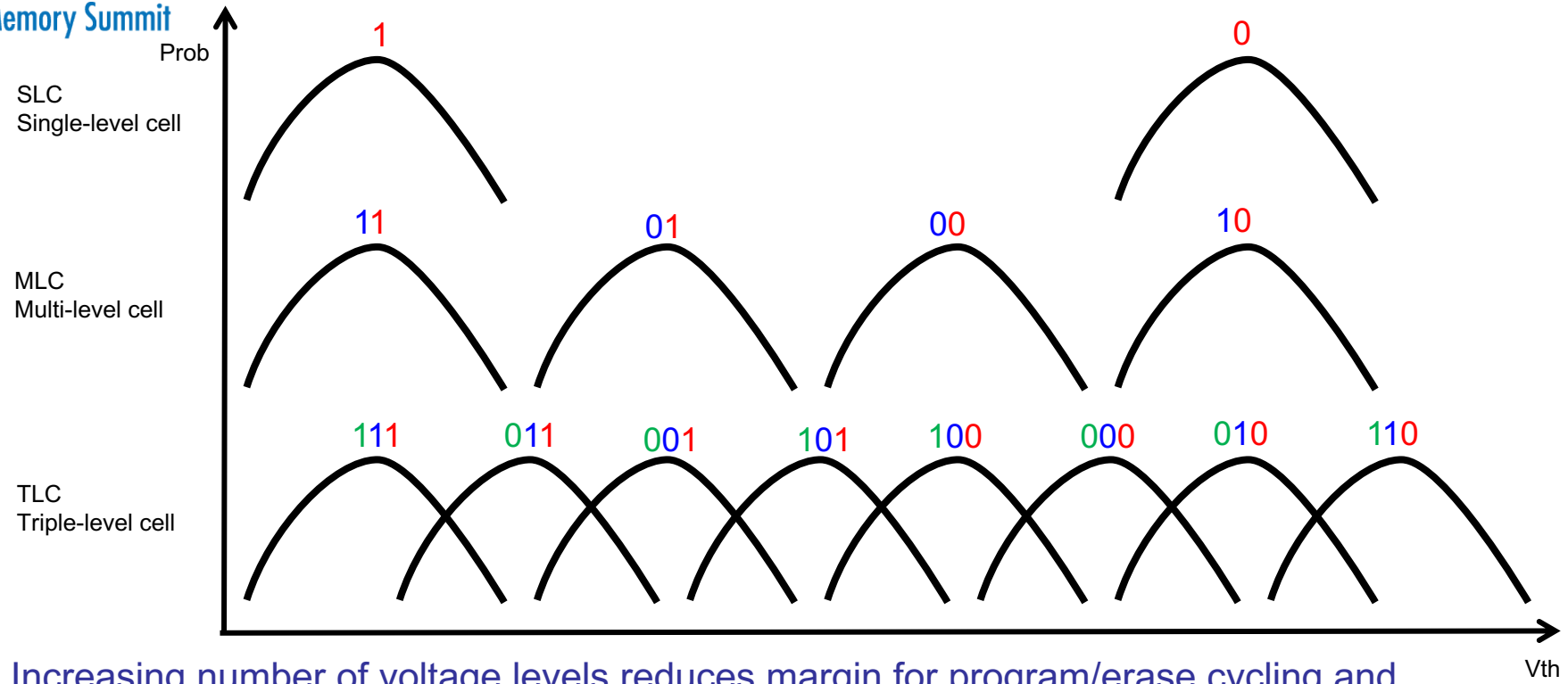




- 3D NAND may extend beyond 100 layers
- 3D NAND extends scaling towards 1Tb die capacity

- Required ECC for SSD-grade endurance exceeds 60b/1KB for 2D TLC
- 3D NAND relies on strong ECC to make TLC mainstream for SSDs

SLC, MLC and TLC NAND Flash

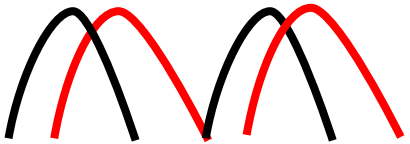


Increasing number of voltage levels reduces margin for program/erase cycling and retention capability

NAND Impairments

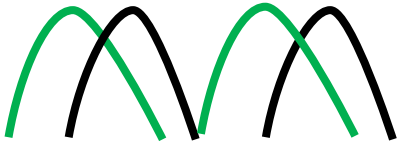
- Program/erase cycling

Voltage distributions before/after cycling:



- Retention

Voltage distributions before/after retention:



- Read disturb

Voltage distributions before/after read disturb:

- Media defects

Page/block/plane/die failures

Mitigation Techniques

Impairment	ECC	Recycling	Read Voltage Calibration	Redundant Silicon Elements
Program/Erase Cycling	X		X	
Retention	X	X	X	
Read Disturb	X	X	X	
Media Defects				X

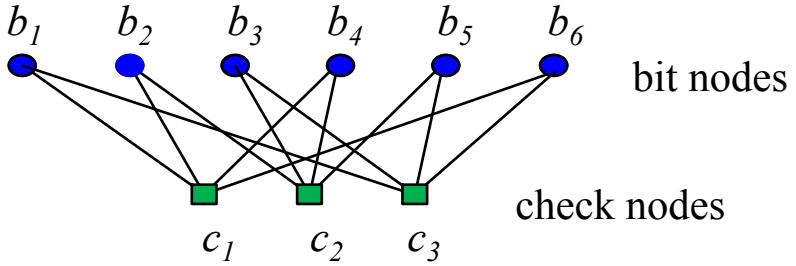
- Capacity, reliability, performance, and QoS behavior depend on choice of mitigation techniques

Low-Density Parity Check (LDPC) Codes

- Defined by a sparse (low density) parity check matrix H
- Are represented with a bi-partite graph
- Support hard and soft decision decoding

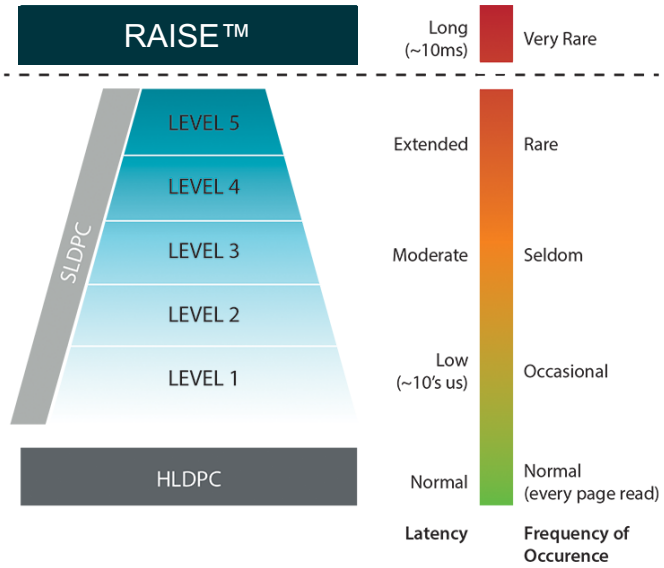
$$H = \begin{array}{c} \begin{matrix} b_1 & b_2 & b_3 & b_4 & b_5 & b_6 \end{matrix} \\ \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 & 1 \end{bmatrix} \end{array} \begin{matrix} c_1 \\ c_2 \\ c_3 \end{matrix}$$

Bi-Partite Graph:



Multi-Level Error Correction

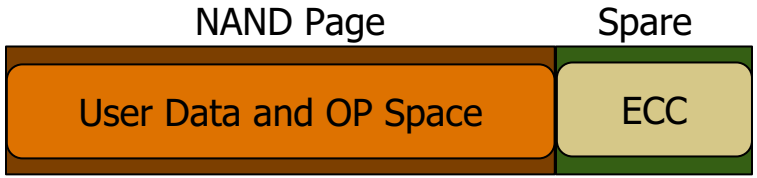
- Hard-decision LDPC decoding is on-the-fly error correction method
- Progressively apply stronger decoding methods such as soft-decision LDPC decoding and signal processing
- Specialized noise handling techniques for P/E cycling, retention, read disturb, etc.
- Optimize time-to-data



Adaptive Code Rates

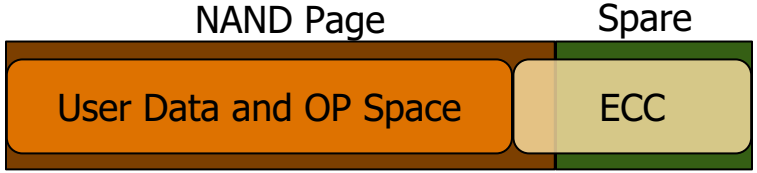
- Beginning of Life: use less ECC to increase overprovisioning
- End of life: increase ECC to maintain reliability

Conventional Error Correction:
Stores fixed ECC in spare field



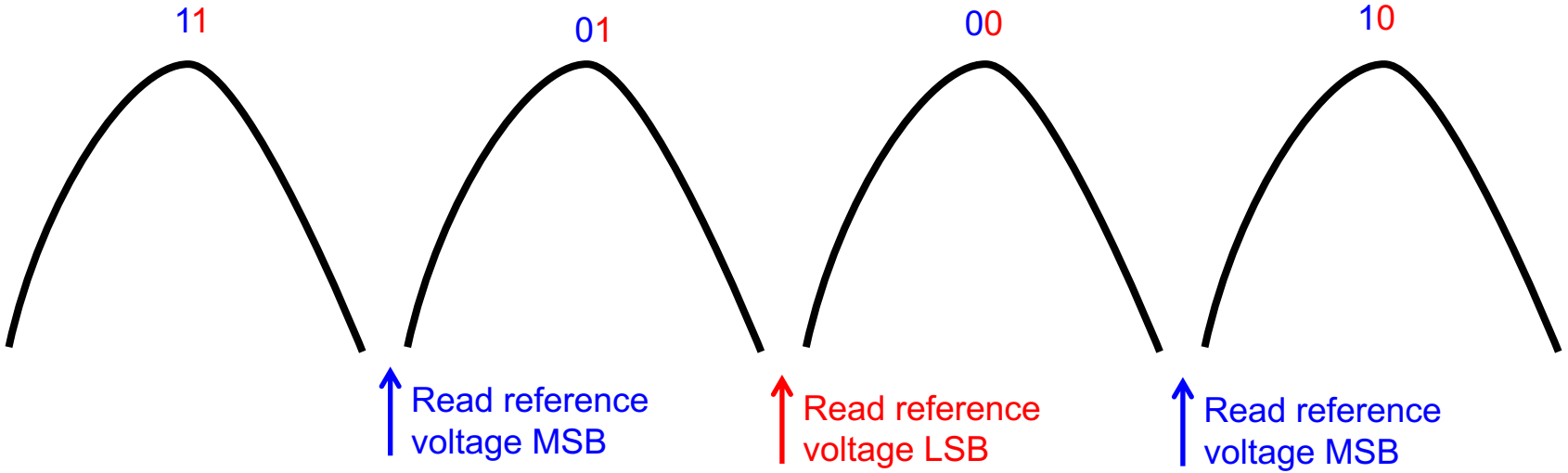
Adaptive ECC (BOL):
Stores ECC in a portion of spare field and increase OP

Adaptive ECC (EOL):
Stores ECC in spare field and uses some of the NAND page



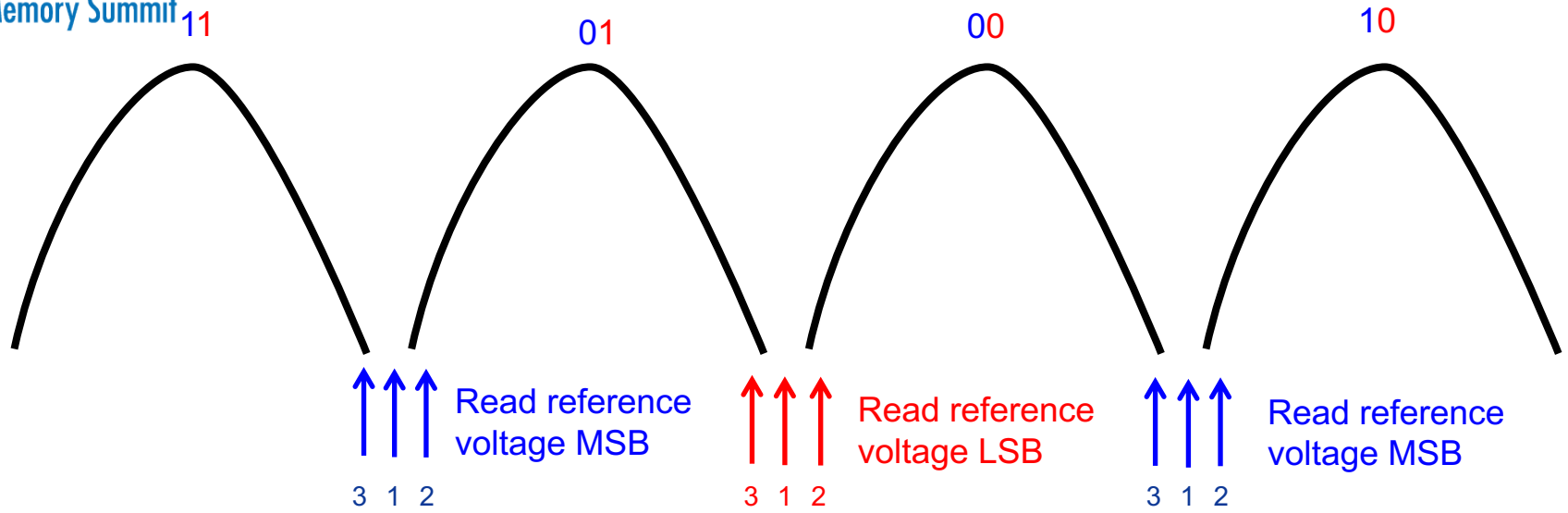
Adaptive ECC allows for more free space @ BOL = More OP and less write amplification

Reading from Flash: Hard Decision Decoding



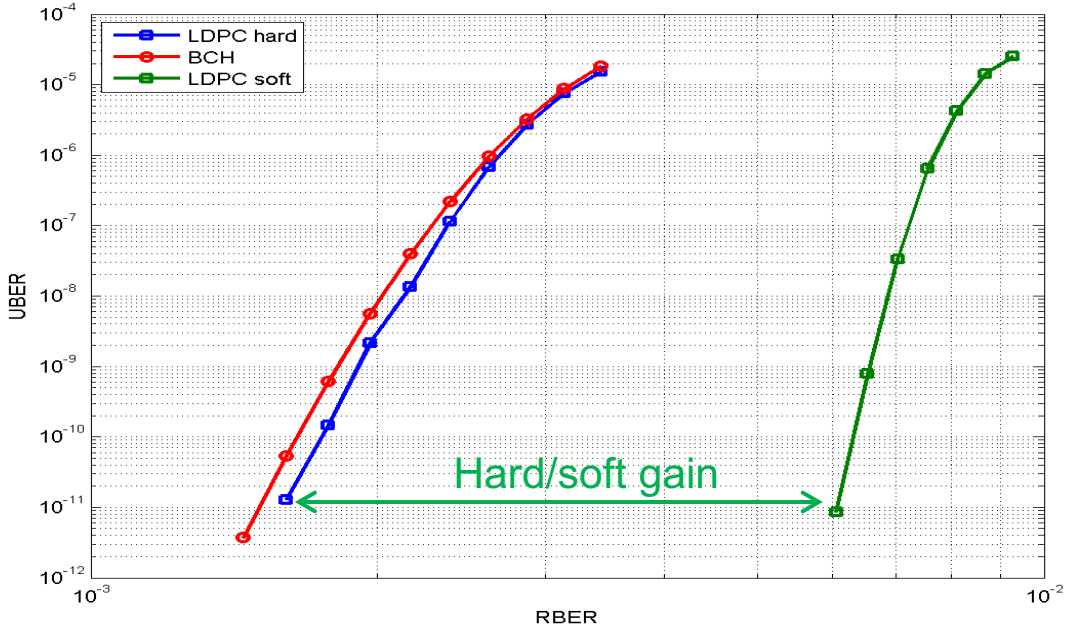
- NAND Flash Memory compares read voltage with read reference voltage to generate hard decision
- One reference voltage for LSB page, 2 reference voltages for MSB page
- Hard decision is used for decoding

Soft Decision Decoding



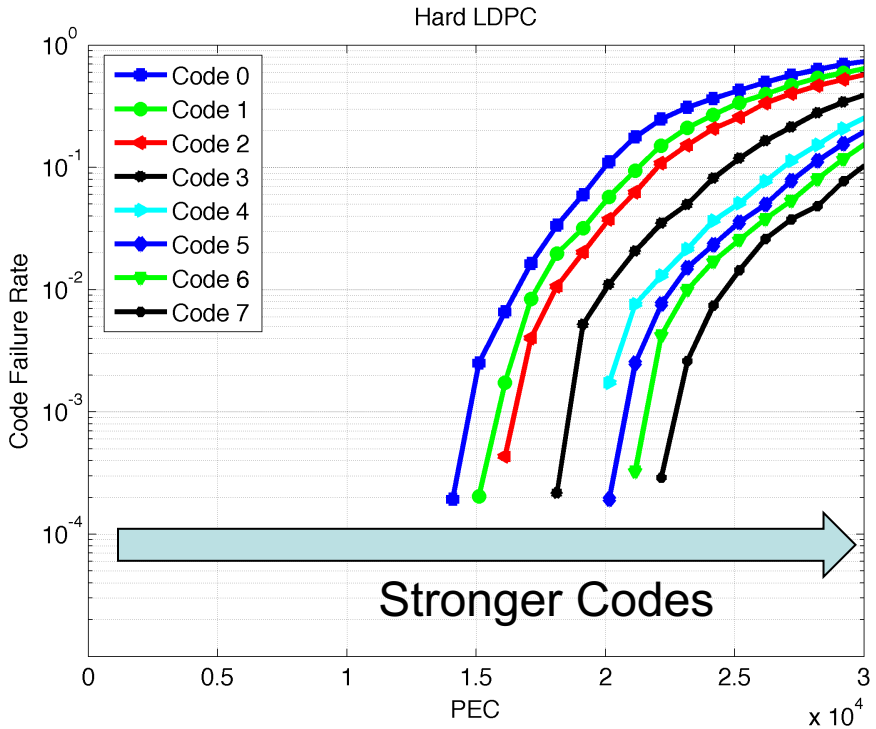
- Sequence of read operations with different read reference voltages to generate soft decision
- Computation of soft information (LLRs) based on multiple read decisions
- LDPC decoder uses soft decision during error recovery

Hard/Soft LDPC vs. BCH



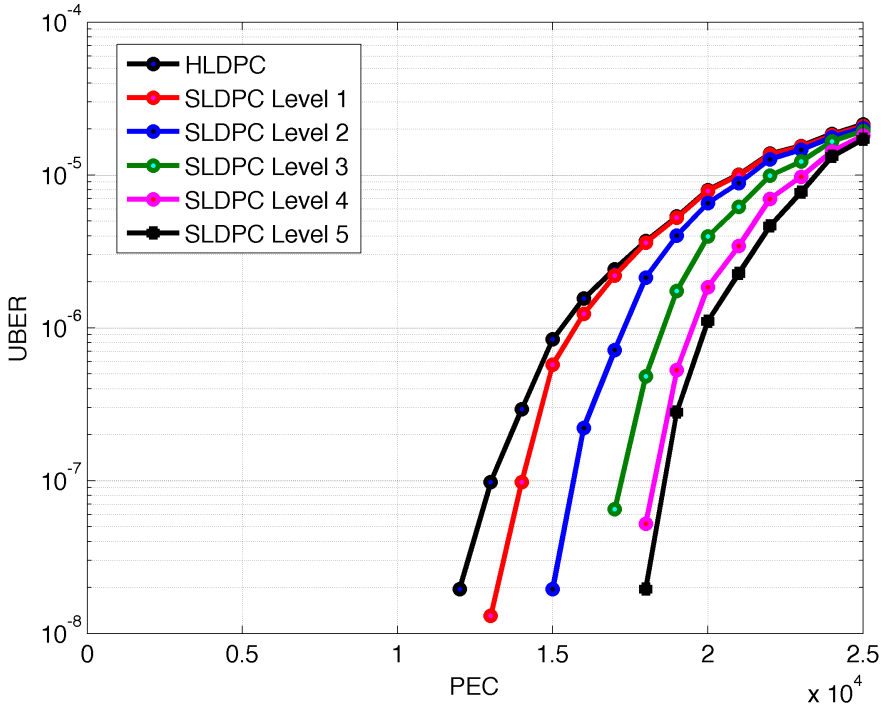
- Soft-decision LDPC decoding has significantly better error correction than BCH decoding

Experimental Benefit of Hard LDPC



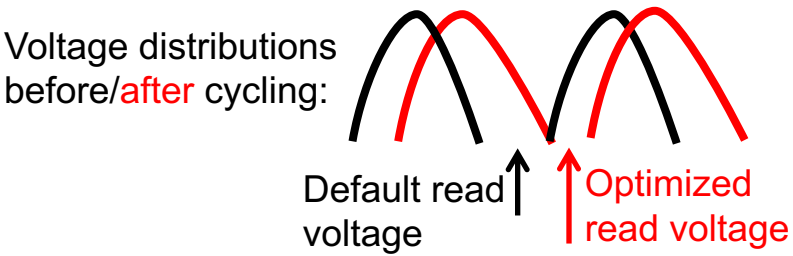
- Measured with controller silicon and firmware for 3D NAND flash
- Multiple LDPC codes cover wide RBER range
- As NAND flash ages, controller switches to the next stronger code
- Read performance improves, since stronger LDPC codes decode data faster

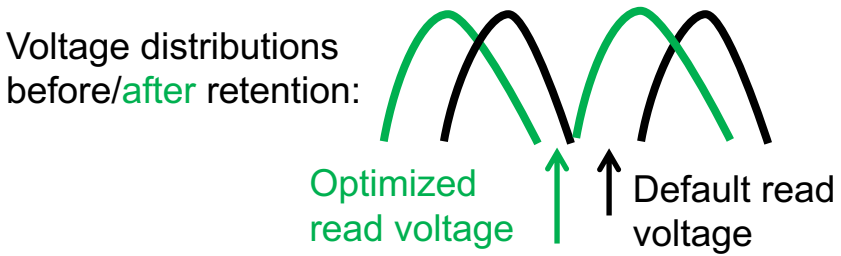
Experimental Benefit of Soft LDPC



- Measured with controller silicon and firmware for 3D NAND flash
- Significant error rate improvement with soft LDPC decoding

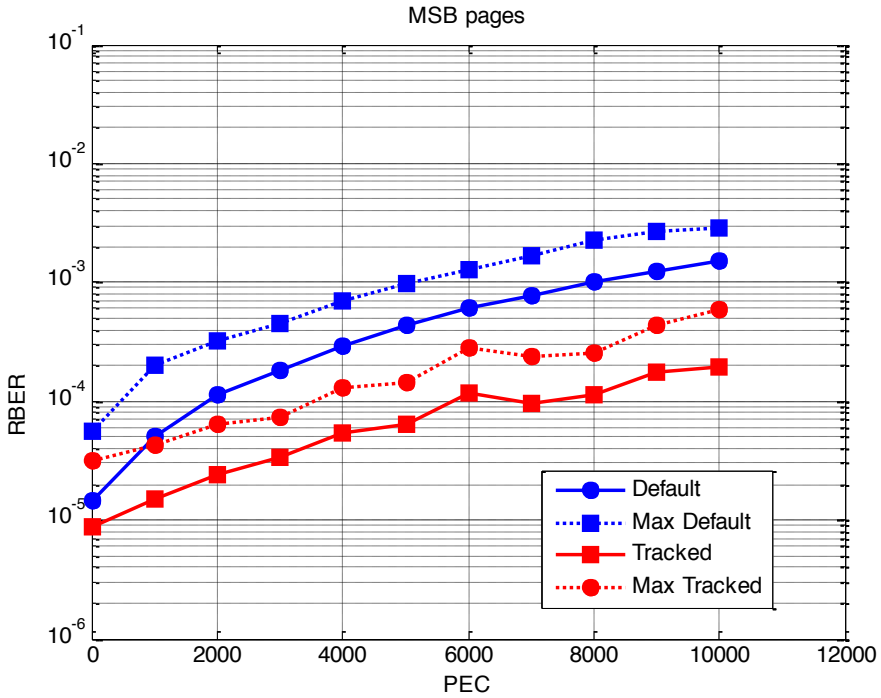
Read Voltage Calibration





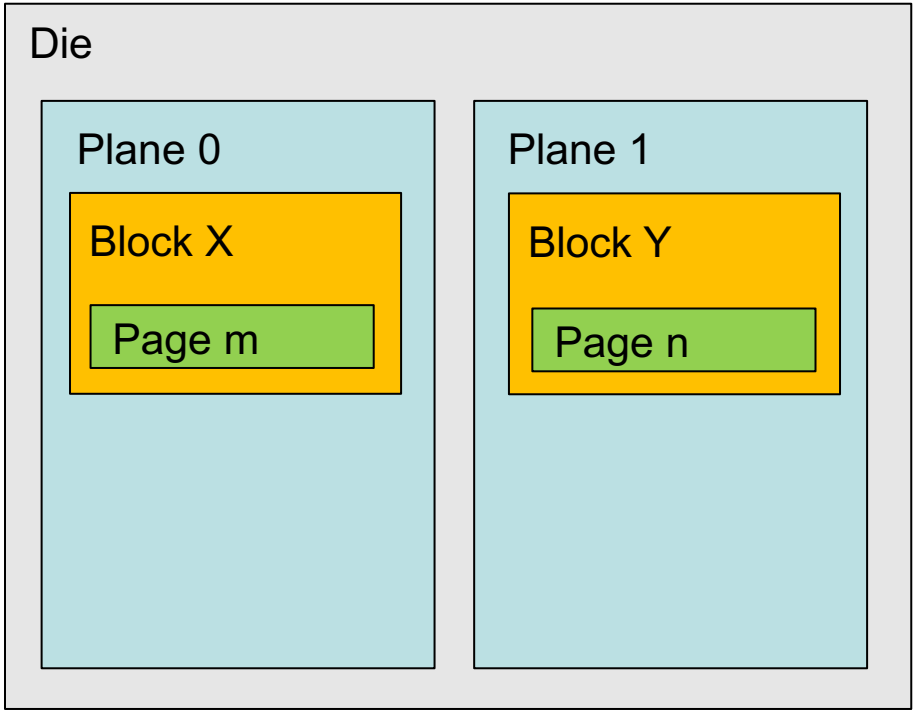
- Optimum read voltages shift as a function of program/erase cycling, retention and read disturb
- Optimized read voltages reduce retry rate and extend endurance

Experimental Benefit of Read Voltage Calibration



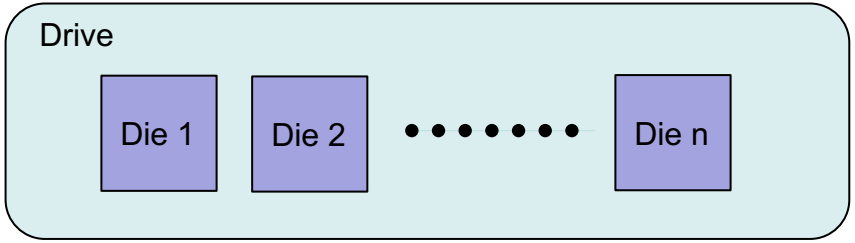
- Measured with controller silicon and firmware for 3D NAND flash
- Significant improvement in RBER after read voltage calibration

Media Failures



- Pages, blocks, planes or the whole die can fail
- ECC cannot recover data from such catastrophic failures
- Need RAID-like protection inside SSD

RAISE™: Redundant Array of Independent Silicon Elements



- RAID-like data protection within the drive
- Write data across multiple dies with additional protection
- Corrects full page, block or die failures when all soft LDPC steps fail

Conclusion

- Industry is transitioning from planar to 3D NAND technology
- 3D NAND and TLC technology will increase capacities of SSDs much further
- 3D NAND will still rely on strong ECC and advanced NAND management features to achieve SSD grade endurance and reliability

Thank You! Questions?

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