Power-Efficient LDPC Technology for High Performance SSDs

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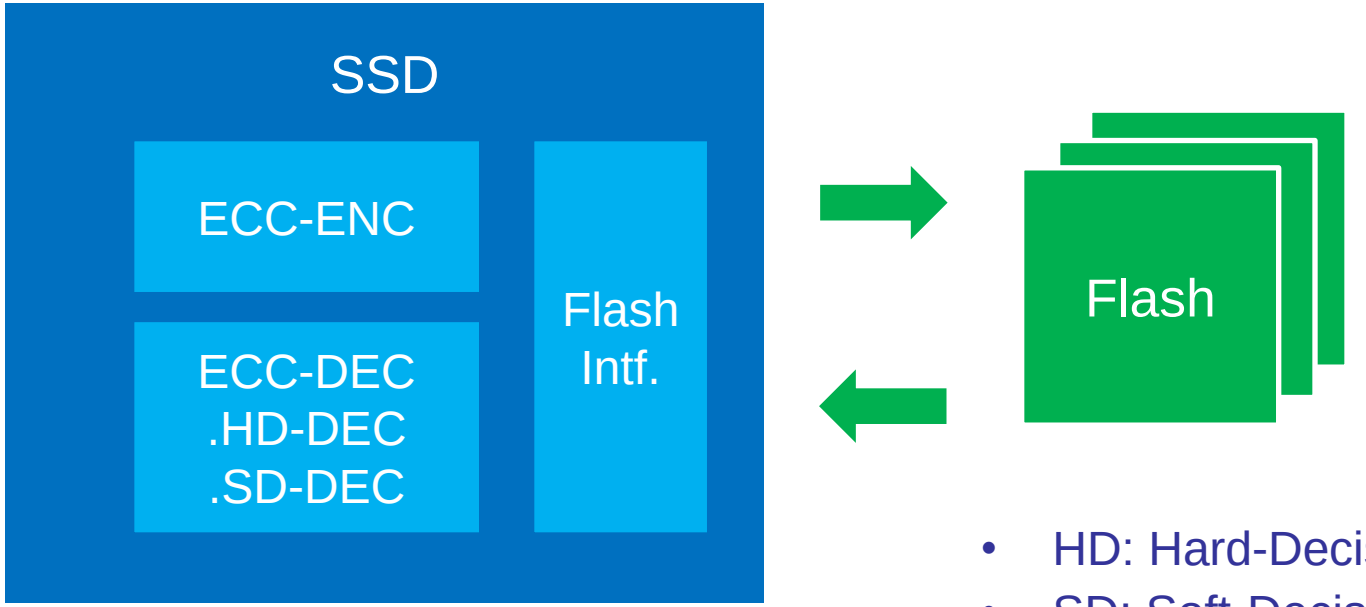
Introduction

- Power Consumption is a big concern for employing LDPC engines in SSD
- LDPC Power can be efficient
  - Algorithm
  - Architecture and Implementation
  - Backend P&R

SSD: Overview

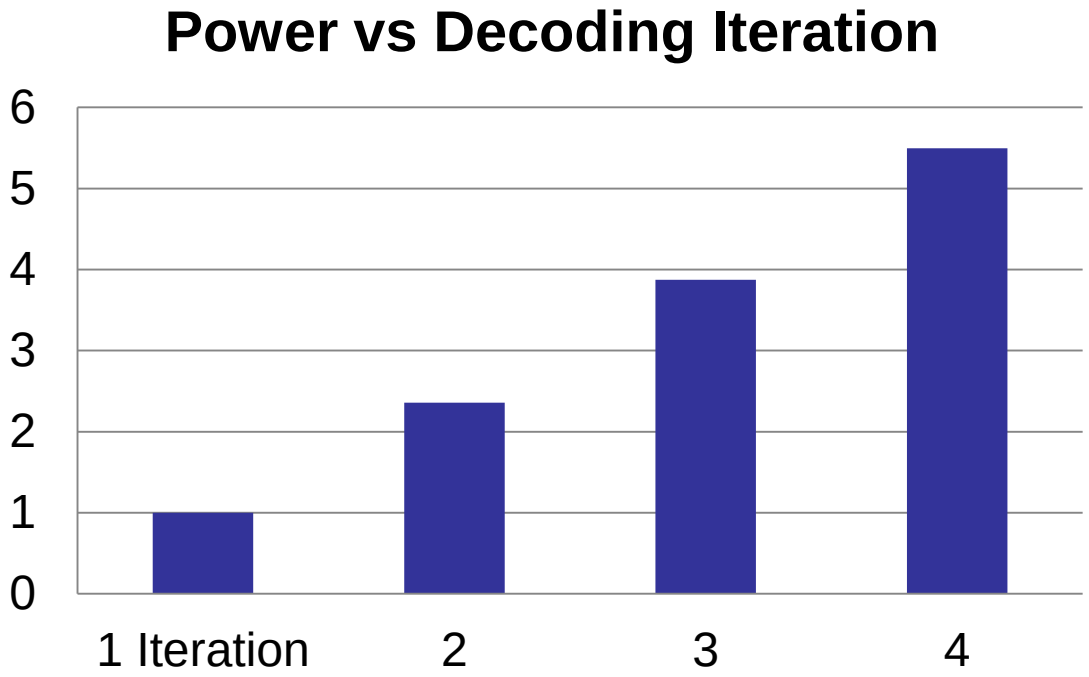


- HD: Hard-Decision
- SD: Soft-Decision

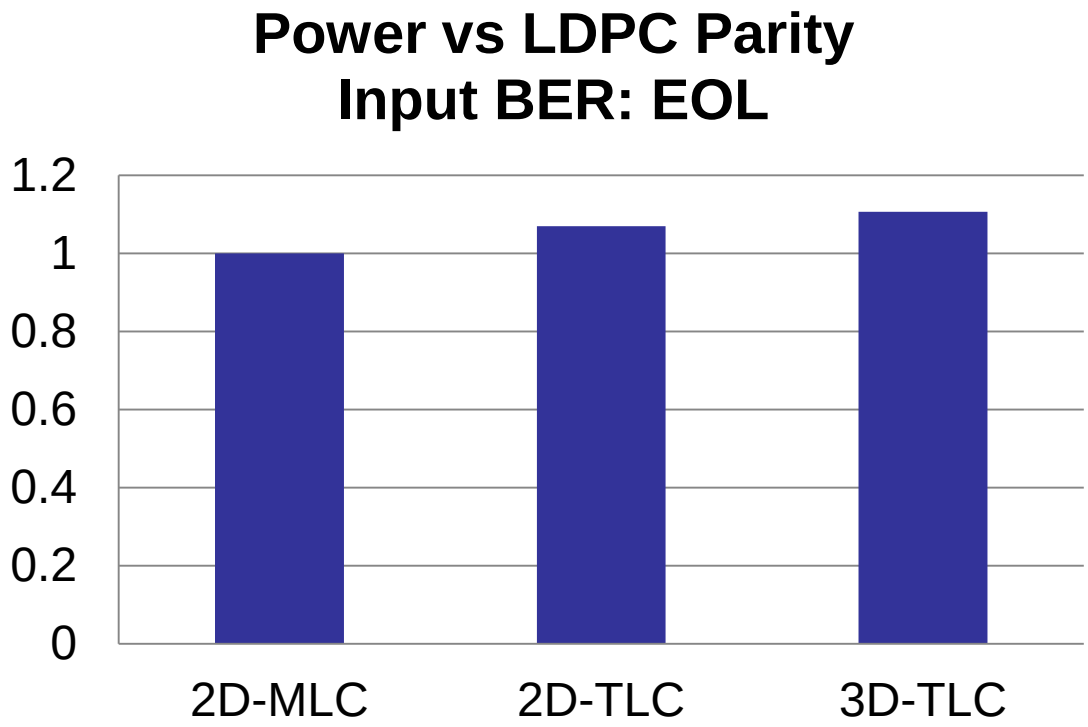
Power Measure Platforms

- EDA Environment
  - NetList + PrimePower
- Real Silicon (With the entire SoC Chip)
  - Power = I * V
- Cross-Check
  - Silicon ⇔ ASIC Simulation

LDPC HD-DEC:



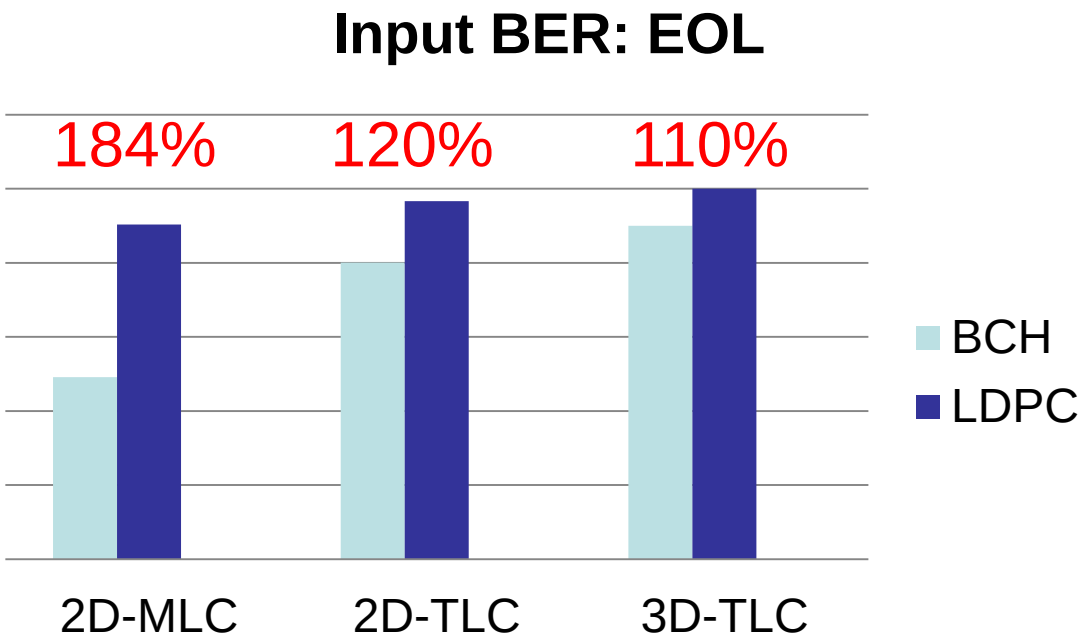
LDPC HD-DEC:


Power vs LDPC Parity
Input BER: EOL
1.2
1
0.8
0.6
0.4
0.2
0
2D-MLC
2D-TLC
3D-TLC

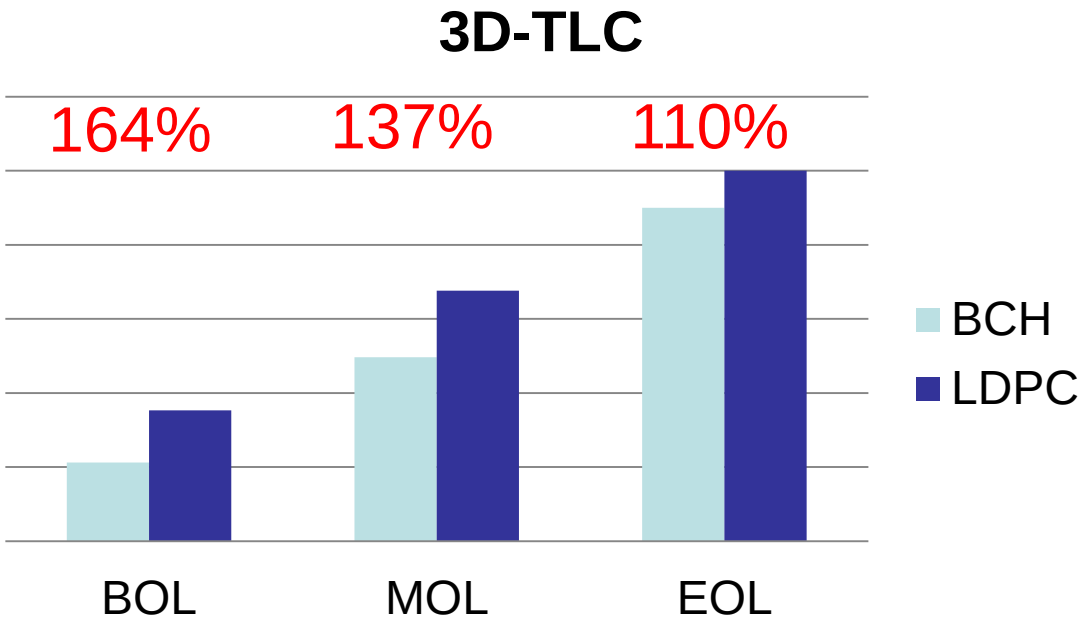
ECC Comparison Setting

- Same Setting for LDPC and BCH
  - ECC Feature
    - Code Length
    - Parity: Configurable to support 2D/3D NANDs
    - Max ECC Correction Capability
  - Implementation:
    - ASIC Process
    - Throughput: Freq * (Bits/Cycle)

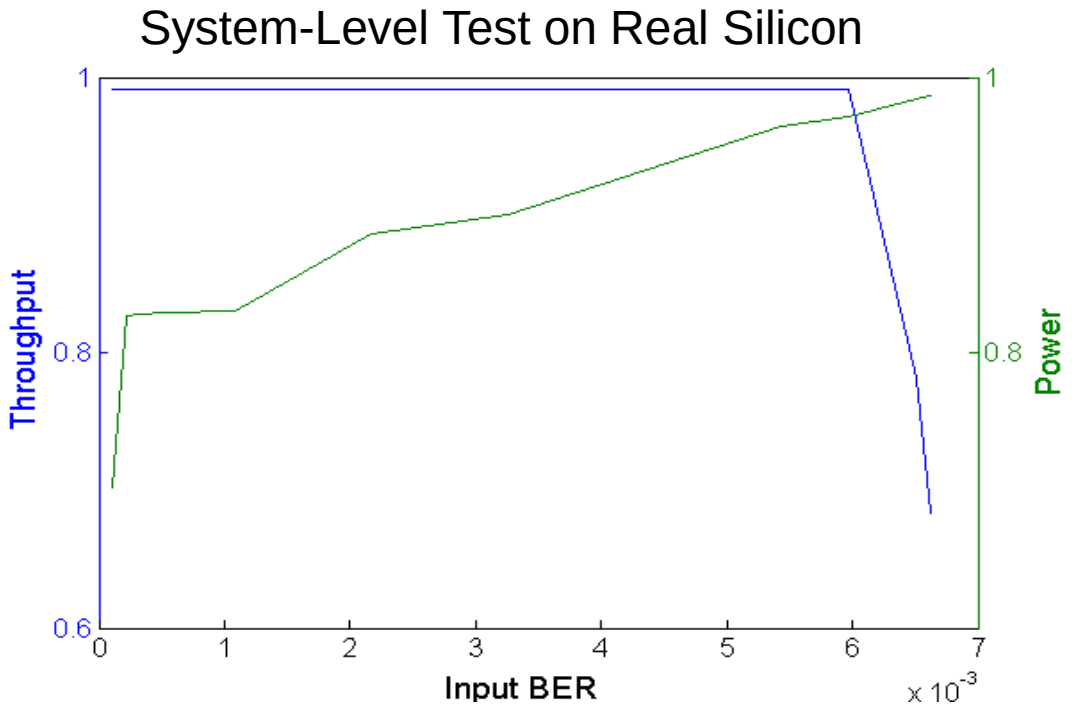
LDPC HD-DEC vs BCH DEC



LDPC HD-DEC vs BCH DEC



Real Silicon Measurement: Power and Throughput vs InputBER



LDPC SD-DEC

- SD-DEC Power
  - Grow with Iteration# / Input BER
  - Grow with Parity
- Compare with HD-DEC,
  - When decoding, power is higher
  - SD-DEC frequency <1%

    => Average power consumption is low

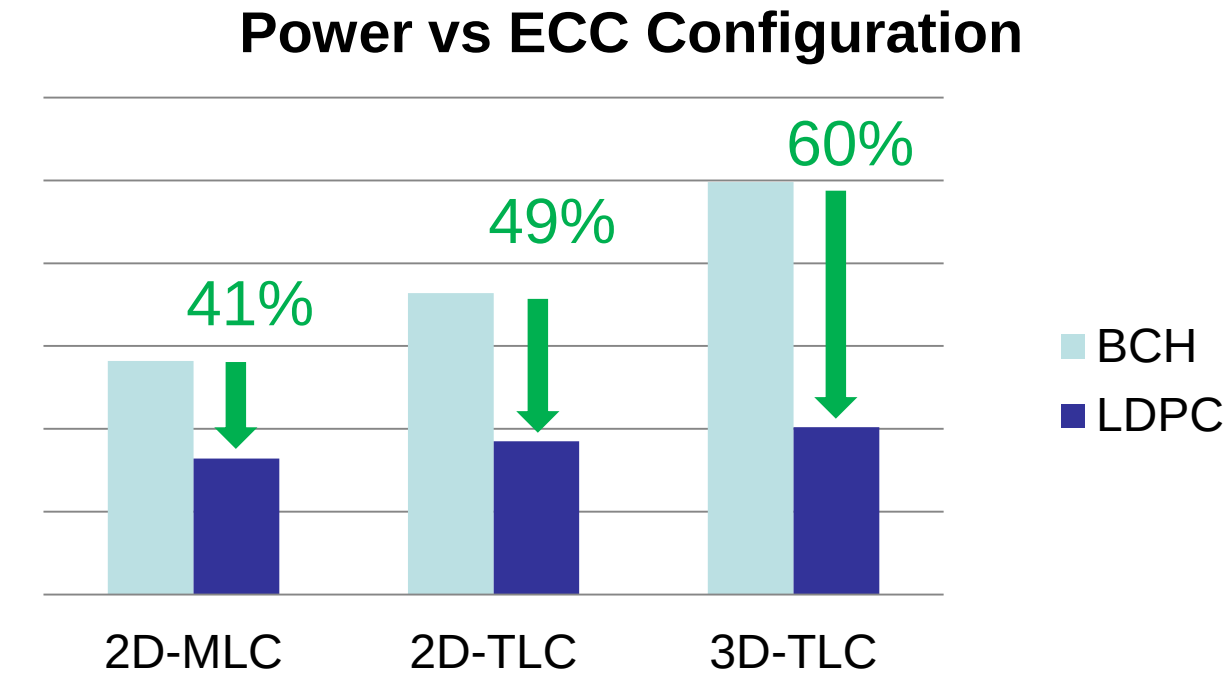
LDPC SD-DEC: Peak Power

ECC Wrapper	Power	Busy / Idle
HD-DEC	1	100% Busy
SD-DEC	165%	100% Busy

ENC Wrapper: LDPC vs BCH

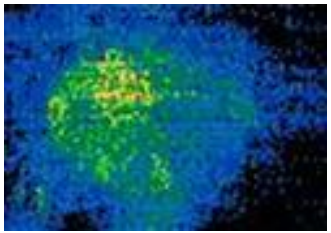
ECC Wrapper	Area	Throughput with Parity
BCH-Wrapper	1	1.6 GB/s
LDPC-Wrapper	192%	1.6 GB/s

ENC Power: BCH vs LDPC

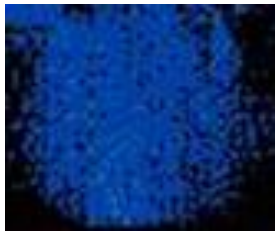


Backend: P&R

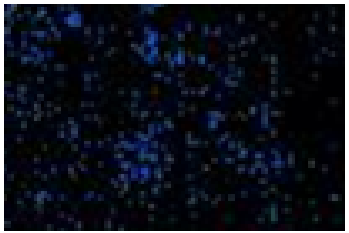
- Routing Congestion



DEC



ENC



MCU

Summary

- LDPC HD-DEC:
  - Grow with Input BER.
  - When applied to 3D-TLC, about the same power as BCH.
- LDPC SD-DEC:
  - Peak power is high, but average is not a concern.
- LDPC ENC:
  - Though LDPC requires more area, its power consumption is much lower.
- VIA LDPC+ Solution employs power efficient architecture for high performance SSDs.

We Are @ Booth #728

VIA Technologies @ Flash Memory Summit	
Time	Presentation
Forum E-22 Wed, Aug. 9 3:20 ~ 5:45pm	Power Efficient LDPC Technology for High Performance SSDs
Forum M-22 Wed, Aug. 9 3:20 ~ 5:45pm	A Novel On-The-Fly NAND Flash Read Channel Parameter Estimation and Optimization