3D NAND Status and Roadmap 2017

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What We Know

- TLC is primary focus for all 3D NAND. MLC is a derivative if needed
- Building the highest possible capacity part is not always optimal.
  - 256G is “Sweet Spot” today, 512+ is useful for high capacity SSDs
- Micron has 256Gb 64L product at 59mm2. CUA is die size advantage
- Toshiba has 512Gb at ~132mm2
- Hynix has 72L (“64L Class”) 512Gb
- Samsung has 512Gb at ~129mm2
- Controller companies/end customers have be qualifying these or similar parts or 6+ months.
  - These are available today for use in SSDs, Memory cards.
- As Samsung and Micron have converted majority of bits to 3D, their costs have declined significantly. 3D NAND is lowering costs

What is Announced/Claimed

- 64L is a done deal. It will ship in high volume at low cost
- Toshiba/WDC announced 96L/QLC
  - Sampling in Fall, shipping in 2018. Not seen in the wild
- Micron is planning Gen 3, will ship in 2018
- Samsung/Hynix planning 96+ layers
- None of these are close to qualification and subject to change as they are evaluated
  - Claiming any of these announcements as a first or leadership is debatable
- Key Takeaway: There is no “brick wall”, we have plans for 3-5 years

Future Model and Estimates

- At full production, 3D wafer cost is significantly more expensive than 2D NAND for both Greenfield and Conversion
  - Fab output/ft^2 drops and new equipment needed.
  - There are still multiple critical lithography layers and advanced tools
  - Some layers are pitch doubled.
- String Stacking adds to cost. Doesn't double the cost of the array but could add 10% to cost. All NAND vendors will need some type of string stacking eventually
- BUT Improvement in bits/mm2 is dramatic and overcomes the wafer cost increase
- Yields are lower for 3D NAND initially. Multiple vendors have achieved mature yields. Adding layers doesn't automatically limit yields (redundancy)
- Yields will approach HVM Goals after 6-12 months in production for all companies
- For new technologies, wafer cost and die cost start very high and reduce over lifetime with efficiency and high yields
- All of these inputs go in to our very detailed cost model for all companies

Flash Memory Summit

From FMS 2013: ROI on NAND Scaling

N Generation announced for samples

N +1 Generation announced for samples 6Q Later

N +1 Cost is cheaper than N

N generation cost

N+1 historical data

Unit cost (normalized)

Quarter after N Generation Samples

Unit cost is very high to start

- **High wafer cost**
- **Low output**
- **Low yield**

3D NAND is NO different

Process/Product Technologies

- REPEAT: Geometry terms like 40nm or 20nm are not useful. Architecture is too complex for analysis like this.
  - All companies have channel holes at 60nm+ and contacts at 20nm
  - Vertical gate spaces and features can be <20nm
- Micron/Intel floating gate is significantly different from charge trap
  - Opinions vary on which will scale better
  - CUA gives die size advantage at equivalent number of layers
- Density (Not Capacity) and Die Size are the key cost metrics and both are available after sampling. Some numbers are published.
- QLC is coming. Acceptance depends on performance and actual cost savings (25% lower in theory).
  - Yields, test cost, overprovisioning, etc combine to determine true cost.

Cost summary

- Planar yields gave them a cost advantage up to 32L/ Mid 2016.
  - Ramp decisions were based on each companies Planar vs 3D Costs
- 48L+TLC+HVM yields gave 3D a cost advantage even with mediocre yields
- 64L Gives all companies a large cost advantage.
  - This drives aggressive capital spending and conversion
- 96L+ and QLC allow significant cost reduction for next 5 years

August 2017 Cost Summary ($/GB)

Announces or Reported Technologies

2017/2018/2019 NAND Costs

(2017 Average Cost)

2017 Planar TLC

128L not mature until 2020

2017 HDD

32L TLC (B) | 48L TLC (D) | 48L TLC (A) | 48L TLC (C) | 64L TLC (D) | 64L TLC (A) | 64L TLC (B) | 96L TLC | 96L QLC | 128L TLC | 128L QLC

Cost 2017 | Cost 2018 | Cost 2019

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Impact of Cost on 3D Ramp

- 3D NAND will be ~50% of all bits for 2017 overall. This will be confirmed in earnings announcements

- 3D Industry conversion prediction
  - 50% of Industry Bits in 2017
  - <75% of Industry Bits in 2018
  - Market/capital spending decisions 2019+
    - Can we afford to convert
    - Is it cost effective for <128Gbit
    - Is NAND Price stagnating market growth
    - Phones market is the tipping point

What about price???

- In June 2016, NAND (and DRAM) shortages started to appear and have continued since
- Prices increased. Market reports showed increased of 50-100%.
  - NAND vendors actual reported increases of 15-30%
- During shortage, Price is not related to cost. Costs went down, prices increased.
- When the shortage is eliminated, prices will fall quickly based on costs and acceptable margins
- 64L conversion and ramp SHOULD address the shortage in 2018

Summary

- 3D NAND at 64L provides significant bit cost reduction compared to Planar.
- 64L is working at all companies and will ramp aggressively in 2017
  - This will provide relief to shortages by early 2018.
- Yields will struggle initially, then reach maturity over time. Not new
- 96L+ and QLC provide significant bit cost reduction over the next 5 years.
  - 25% cost reduction per year