



Flash Memory Summit

Scalable Platform for Keeping SSD Test Costs Under Control

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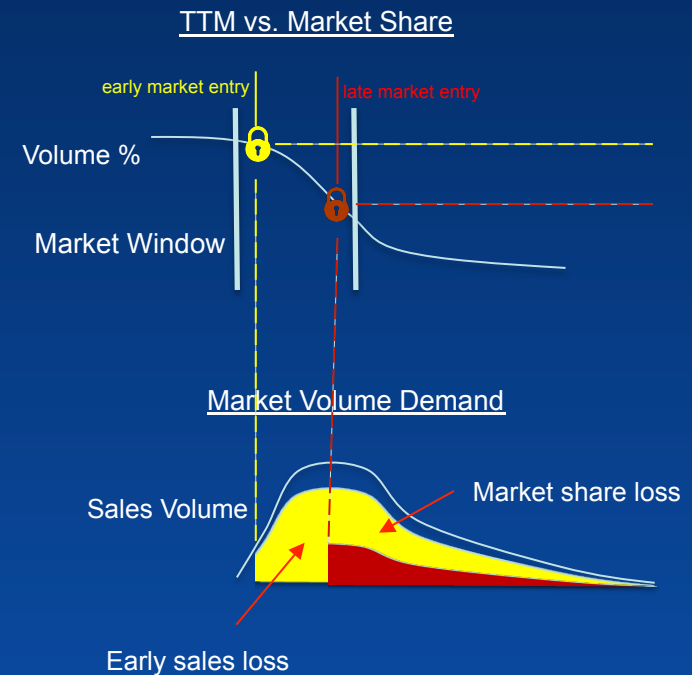
Outline

- Time to market and test
- SSD Test Platform
 - Main characteristics
- SSD Test Platform Automation
- Traffic Capture and Debug Tools
- Conclusions



Time-To-Market and Market Share

- Hitting market window greatly increases product revenue
- Both early market volume and increased market share are gained
- TTM is critical to determining product success

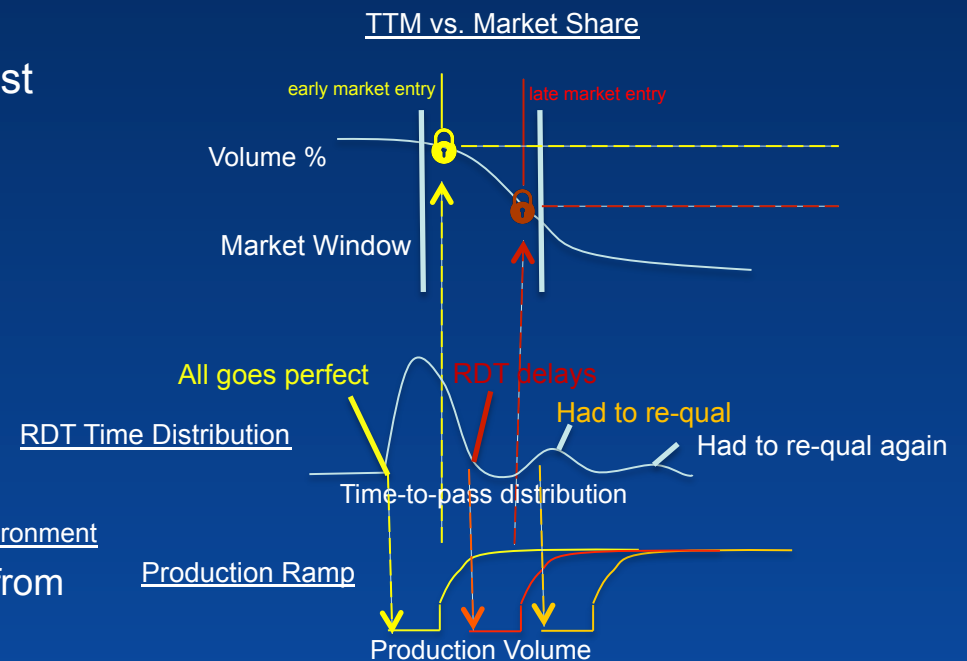




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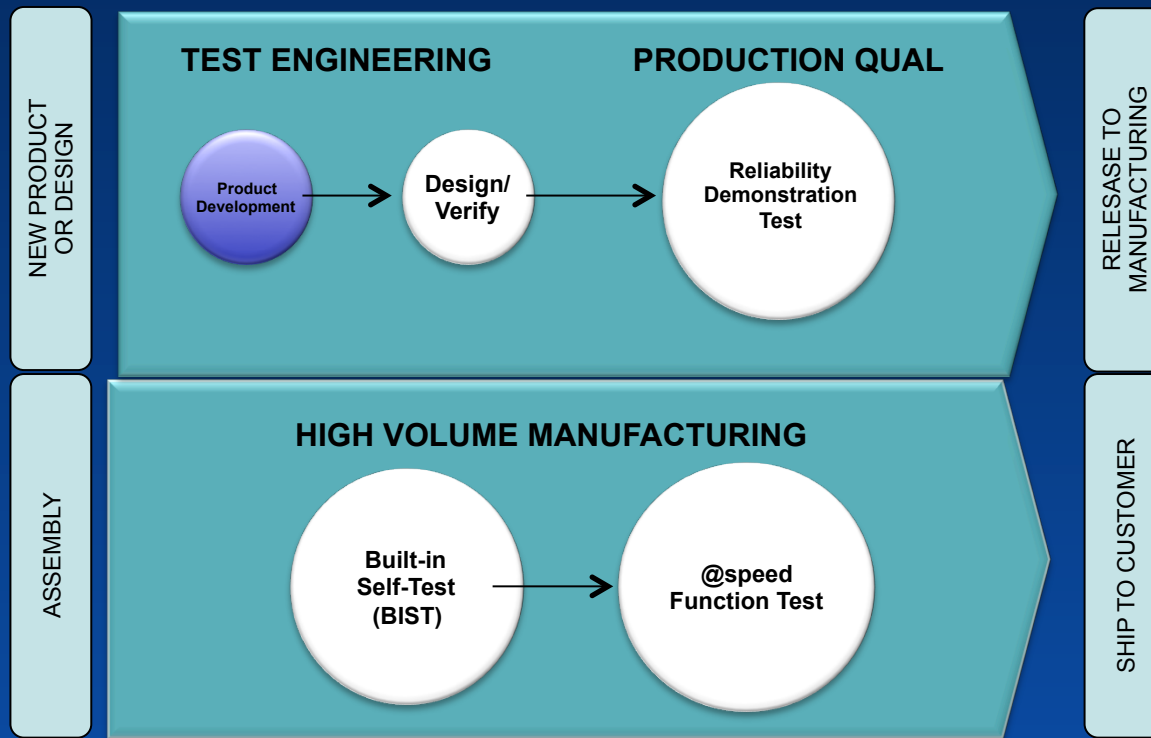
How Does Test Affect TTM?

- RDT is needed to qualify the SSD product
- Followed by time to release to production test
- Risks to hit market window:
 - Product and Test development delays
 - Qual failures
- Risk Mitigation
 - Catch device problems early
 - Thorough set of Engineering Tools
 - Support from tester provider
 - Catch test development problems early
 - Run all production, RDT at engineering, in the same environment
 - Minimize introduction of new test conditions from engineering through production
 - Reuse tests and interfaces



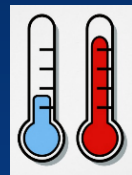


SSD Lifecycle Test Stages





SSDs Wide Variety of Test Requirements



-10 to 85 degC
(125 degC)

Different Temperatures

Different Protocols



HHHL



2.5"/U.2



M.2

Different Form Factors

SSDs

Manual/
Automated



Operator/Robot

Different Test Methods



Functional

Enterprise/
Consumer



Different Speeds



1.5 Gbps to 12 Gbps



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How to address all these test needs?

- All-included Test Cell
 - Advantage: Can do everything
 - Disadvantage: Expensive

- Application Specific Test Cell
 - Advantage: Inexpensive
 - Disadvantage: Can only do one thing

- Is it possible to have the best of both worlds?

- Test Platform – SLT Test Platform
 - Allows for component “mix-and-match” to develop optimal tester at the right cost.






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Application Specific Optimal Test Systems

FPGA Based Test Electronics


- Two FPGAs include HVV acceleration & PCIe Protocol IP
- 8 DUTs per board
- 48 lanes per board
- 48 DUTs with 1600 lanes each 8 lanes
- 48 DUTs with 1600 lanes each 8 lanes
- 48 DUTs with 1600 lanes each 8 lanes
- New protocols and drivers can be downloaded to the FPGAs
- CDM Processor facilitates file system commands, SPI drivers and compatibility with existing PCIe programs
- 128 Sideband Signal pins
- 2x 48 W boards (2 DUT)
- Controls 1-2 DPS boards
- Support for 4 independent modules per DUT



Hot – Double Density Site Module

BIST – BI Site Module

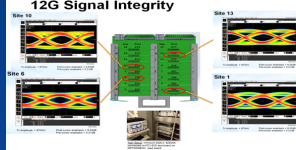
Powerful, Easy-to-Use Software



HDDPS – High Density DPS

DRDPS – Dual Range DPS

12G Signal Integrity




Thermal Control Closed Loop

Thermal Open Loop

Independent Power Supplies

- Per DUT Programmable Supplies
- Individual control of power per module
- Remote sensing provided per DUT module
- Stable output 0.01% to 1% 500W max
- Current 10A to 20A per supply
- Current measurement 0A to 0.2% 500W max
- Voltage measurement 0V to 10V 0.001% max
- Remote sensing: 0.01% accuracy in 500W mode
- Additional Features: Simultaneous DV, Capable, Measurement averaging, Measurement Impedance, Trigger, Drive rate control, DUT discharge, Programmable over current threshold and time
- Modular/Scalable
- 48 independent power supplies per DPS board
- 200W per DUT power overhead (0 supplies), 500W total per DPS board (48 supplies)
- 1-2 supplies per DUT (2 for availability up to 4 for 48 test availability)



Test Cell Automation

Test Floor Automation

High Performance System
SM + DPS + TCL + Stylus

HP HVM System
Hot + HDDPS + TOL + Stylus

HP A HVM System
Hot + HDDPS + TOL + Stylus + Automation

BI/BIST HVM System
BIST + HDDPS + TOL + Stylus

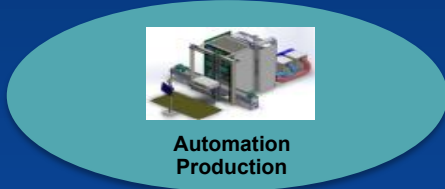
BI/BIST A HVM System
BIST + HDDPS + TOL + Stylus + Automation





SSD Test Platform

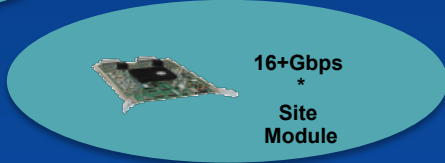
- Today
 - Application Specific Test Systems at “optimal” cost.
 - Chose components tailored to address current test needs.
- Tomorrow
 - Only need to buy specific components to cater for new DUT technologies, for instance, “next generation protocol board”.
 - Reuse the rest of the system.



Automation
Production



Self-Test
Site Module/ DPS*



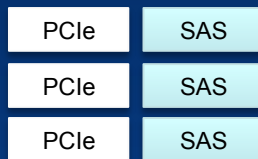
16+Gbps
*
Site
Module



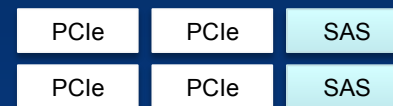


Different Protocols: PCIe, SAS, SATA

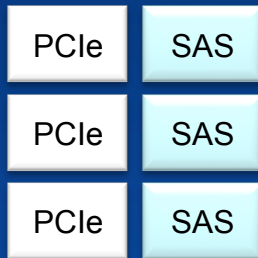
Market Demand A



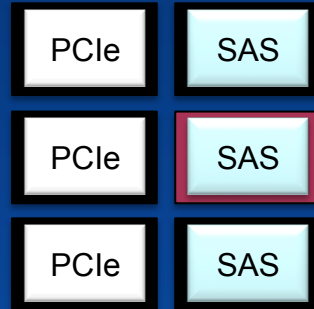
Market Demand B



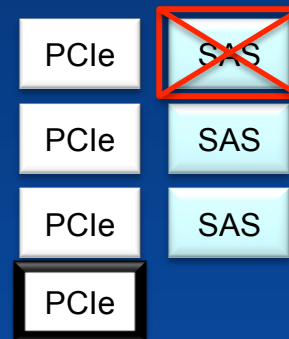
Std Tester



Test Platform



Std Tester



1x New Tester
1x Idle Tester

Test Platform

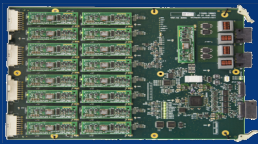


No new testers
FW download in
minutes



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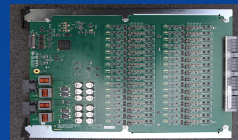
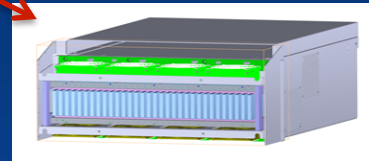
Full Protocol Test



Different Test Methods



BIST+
Smart
Power
Test

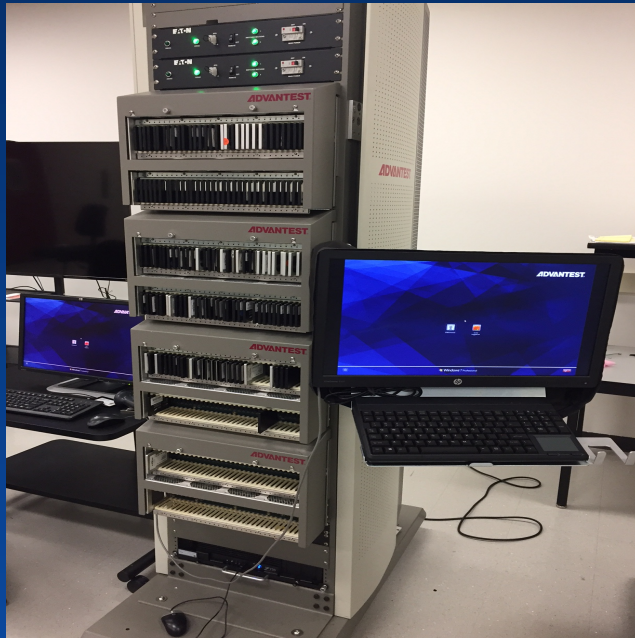


BIST Test



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Different Form Factors



U.2



M.2

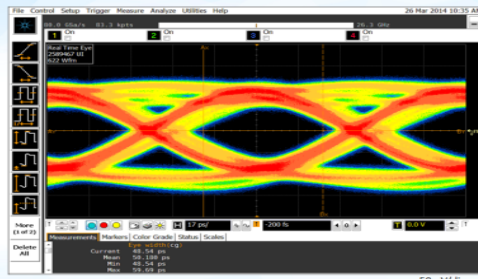




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Different Speeds: 12G Signal Integrity

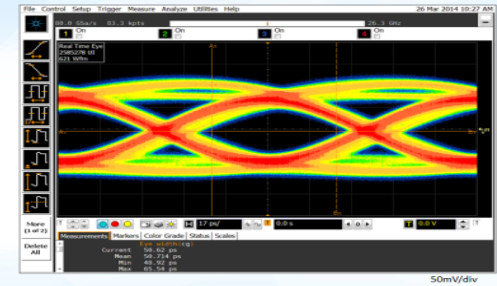
Site 10



Tx Amplitude = 973mV
Post-cursor emphasis = 8.52dB
Pre-cursor emphasis = 2.21dB

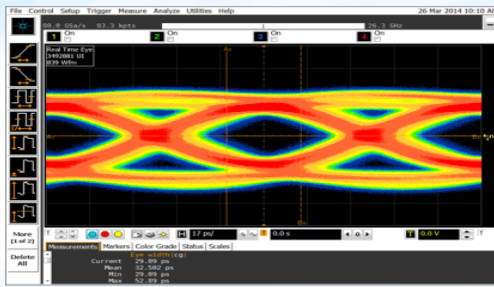


Site 13

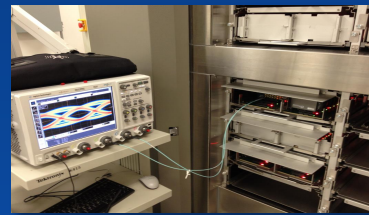


Tx Amplitude = 973mV
Post-cursor emphasis = 8.52dB
Pre-cursor emphasis = 2.21dB

Site 6

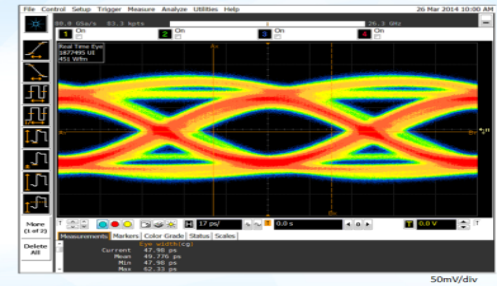


Tx Amplitude = 973mV
Post-cursor emphasis = 8.52dB
Pre-cursor emphasis = 2.21dB



Test Setup: Infiniium DSA-X 92504A connected to PCI-SIG test board on MPT3000ENV load board.

Site 1



Tx Amplitude = 973mV
Post-cursor emphasis = 8.52dB
Pre-cursor emphasis = 2.21dB

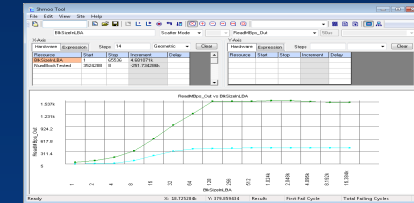


Powerful, Easy-to-Use Software

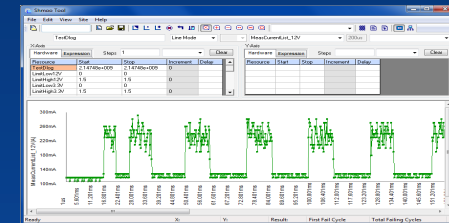
Flash Memory Summit Stylus Main, Datalog & Test Flow Control Tools

Graph Characterization (BW vs LBA Size)

The screenshot displays a complex software interface for test flow control. On the left, there are several panels: 'Program Flow Tool' showing a flowchart with nodes like 'ProgramOutDevice', 'ProgramInDevice', and 'Verify'; 'Datalog Tool' showing a log of test results with columns for time, test name, and status; and 'Program Flow Control' showing a list of test steps. A central '10 BEST' award logo is overlaid on the interface.



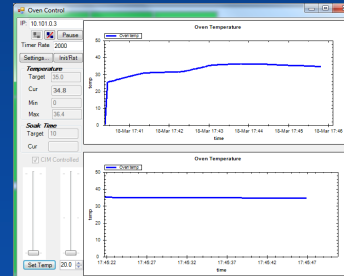
Power Profile Tool



Production Operator Interface

The screenshot shows the 'Production Operator Interface' with the 'ADVANTEST' logo. It includes a 'Ready Operator' section with a list of items, a central control panel with a red bar, and a 'Status' section with a table of data.

Oven Control

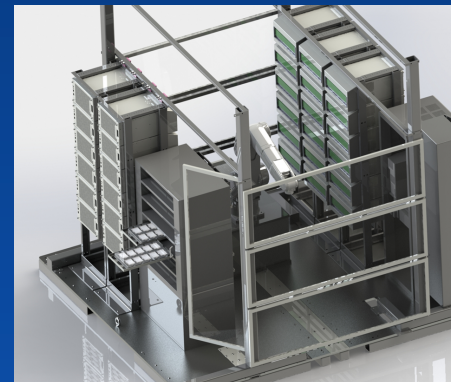
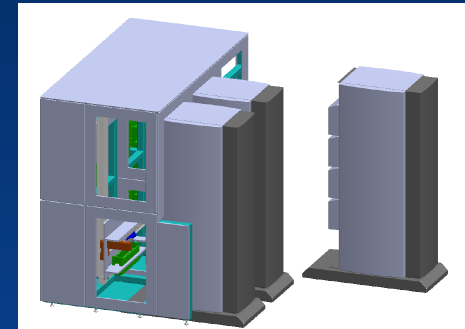
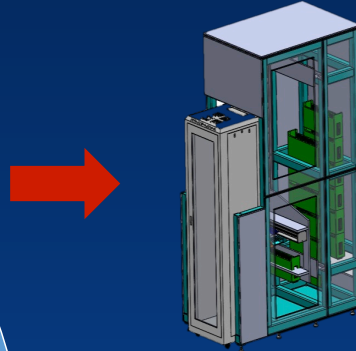
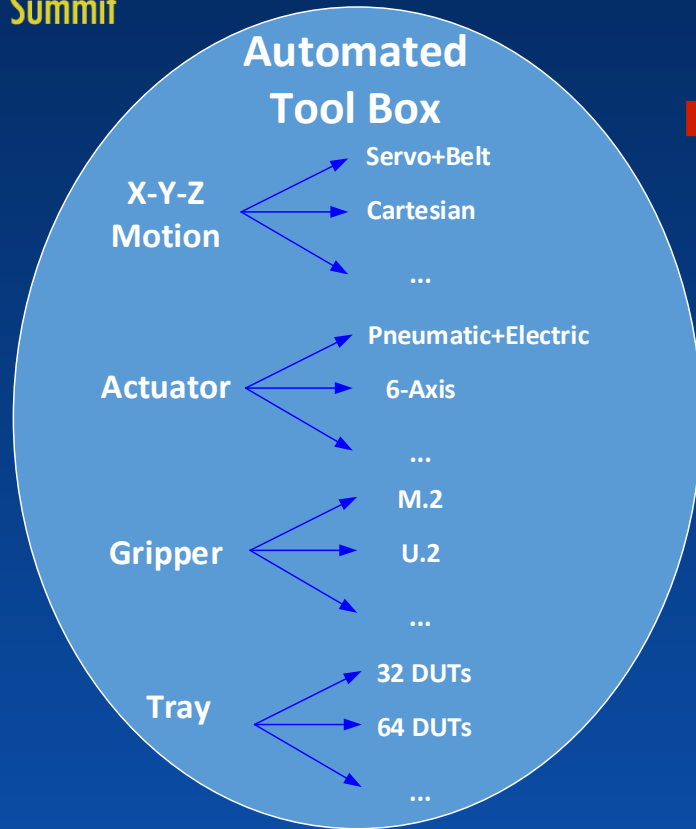


Calibration & Diagnostics

The screenshot shows the 'Calibration & Diagnostics' interface. It includes a 'Calibration Modules' section with a list of modules, a 'Diagnostics' section with a color-coded bar, and a 'Status' section with a table of data.

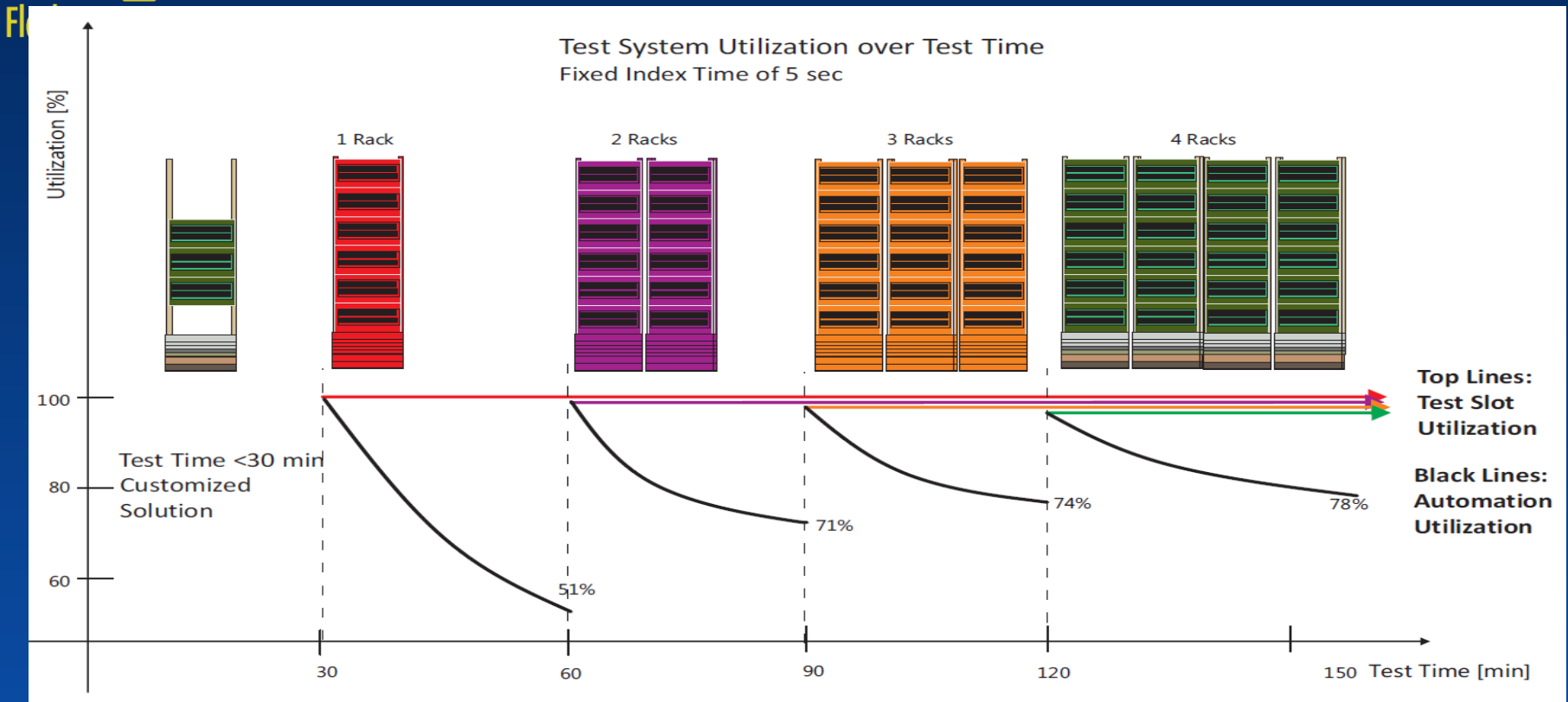


Automation Platform Components





SSD Automated System Scalability





Fault Detection Vs Fault Location

- ATE normally focuses on fault detection.
- SSD Test requires fault location capabilities.

Log File Processing

- Automatically create a batch file to bring up logs in viewers to lines of interest

```

@echo off
start notepad++ multiInat -session -eo %0 -%0 -M7293 *0306_09_09_v2_0000
start notepad++ multiInat -session -eo %0 -%0 -M2551 *smc_wm031_2017_01
start notepad++ multiInat -session -eo %0 -%0 -M25548 *smc_wm031_2017_01
start notepad++ multiInat -session -eo %0 -%0 -M8784 *ltp_wm031_2017_01_1
  
```

LTSSM Capture

LTSSM Capture

- Vary fields based upon state
 - No need to show low power state-machines in L0 or Recovery,Equalization
 - Add field to indicate capture format
- Link EQ negotiation



ltssm00 Rcv_Equ	ds=1 w=1 pre=4 cursor=[0,0,0] use=0 E=24 IE=00	TAEI=0	RREI=0
ltssm00 Rcv_Equ	ds=0 w=0 pre=4 cursor=[00,40,00] use=0	TAEI=0	RREI=0
ltssm00 Rcv_Equ	ds=0 w=1 pre=4 cursor=[0,0,0] use=0 E=40 IE=12	TAEI=0	RREI=0
ltssm00 Rcv_Equ	ds=1 w=0 pre=4 cursor=[00,40,00] use=0	TAEI=0	RREI=0
ltssm00 Rcv_Equ	ds=1 w=2 pre=4 cursor=[00,39,01] use=0	TAEI=0	RREI=0
ltssm00 Rcv_Equ	ds=0 w=0 pre=4 cursor=[00,39,02] use=0	TAEI=0	RREI=0
ltssm00 Rcv_Equ	ds=1 w=2 pre=4 cursor=[00,38,02] use=0	TAEI=0	RREI=0
ltssm00 Rcv_Equ	ds=1 w=2 pre=4 cursor=[00,37,02] use=0	TAEI=0	RREI=0
ltssm00 Rcv_Equ	ds=1 w=2 pre=4 cursor=[00,40,00] use=0	TAEI=0	RREI=0
ltssm00 Rcv_Equ	ds=0 w=0 pre=4 cursor=[00,40,00] use=0	TAEI=0	RREI=0
ltssm00 Rcv_Equ	ds=1 w=3 pre=4 cursor=[00,24,00] use=0	TAEI=0	RREI=0





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Conclusions

- Time to market is critical for product success.
 - Test development time and qual risk reduction are keys to TTM.
- An SSD Test Platform optimally addresses:
 - Shortening time to market.
 - Adapt to ever decreasing SSD product lifecycles.
 - Keep test cost under control even as device performance, density, and variety all increase.



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Thank you!