Using Simulations to Generate Relevant PCB Constraints for Flash Systems

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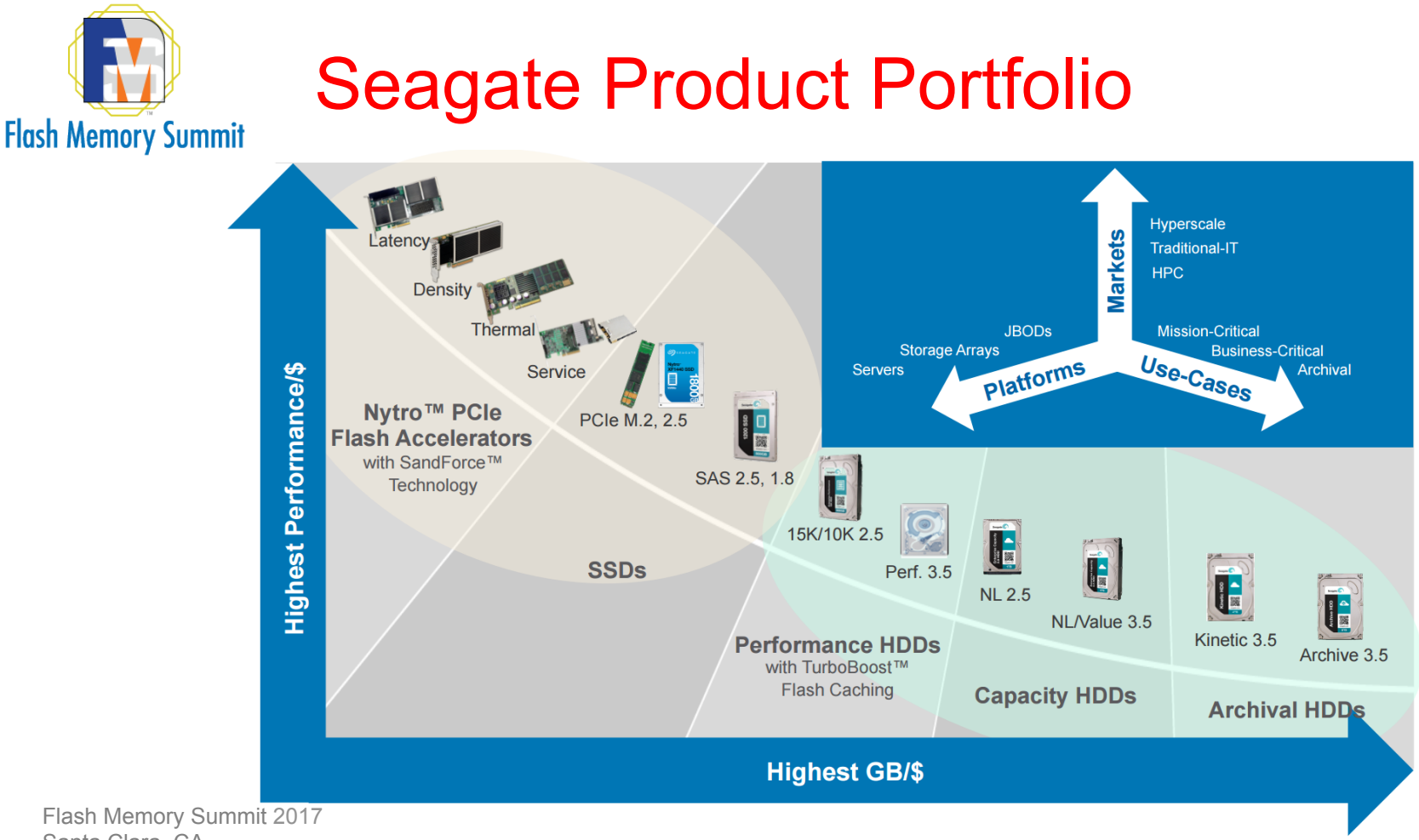
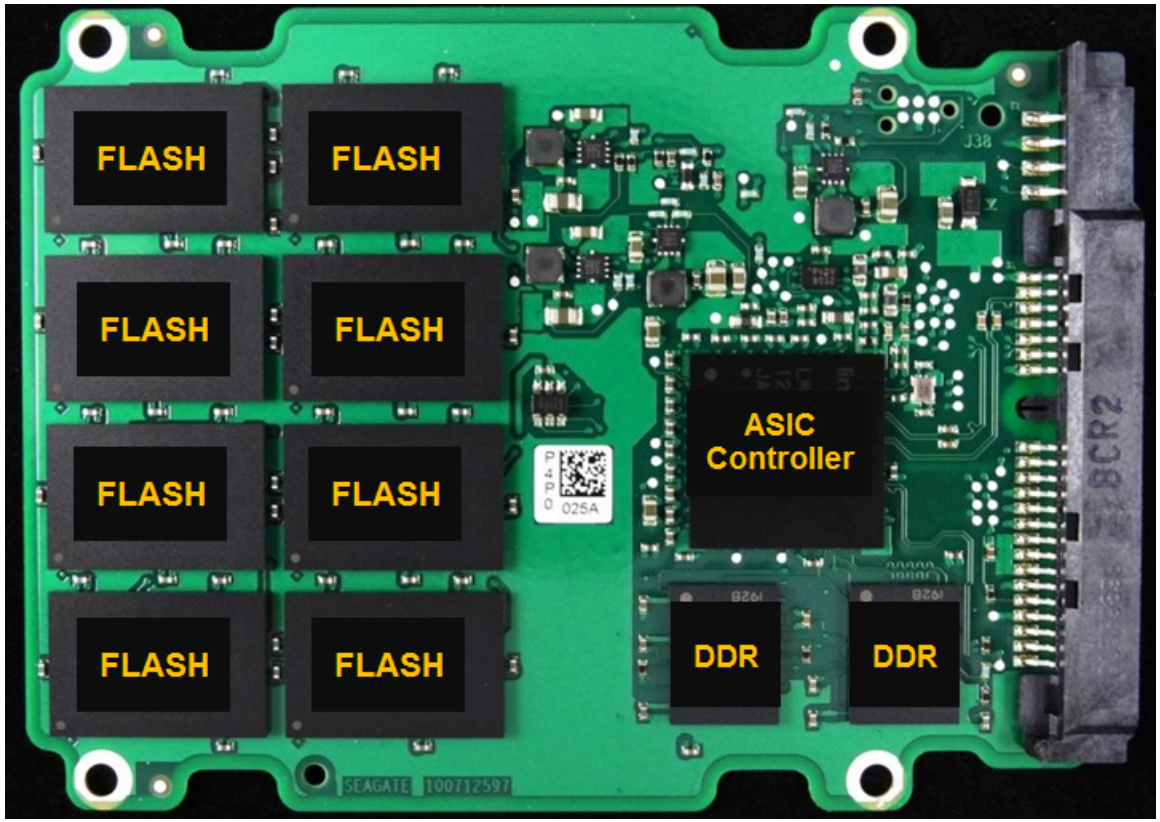
Agenda

- Seagate Background
- Problem Statement
- Solution
- Pre-layout and Checklist
  - Sweep Manager
- Post-layout and Checklist
- Summary



Seagate Product Portfolio

Flash SSD Drive

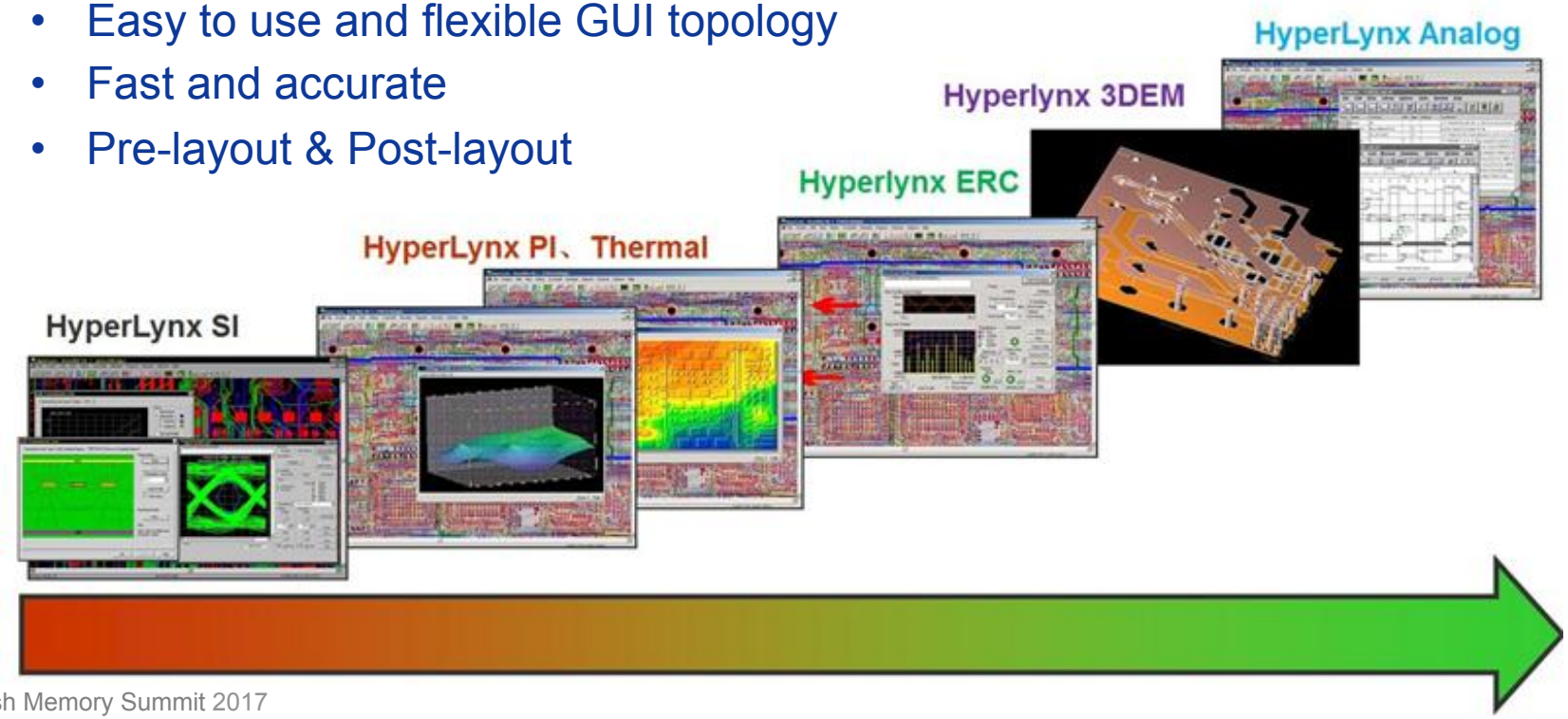


Problem Statements

- Demand for higher capacity, more flash devices(16+ loads) per package
- Demand for higher speed, ONFI 4.0 @ 800MTS
- Challenging System Signal Integrity
- System failure without robust Signal Integrity

Solution

- Easy to use and flexible GUI topology
- Fast and accurate
- Pre-layout & Post-layout



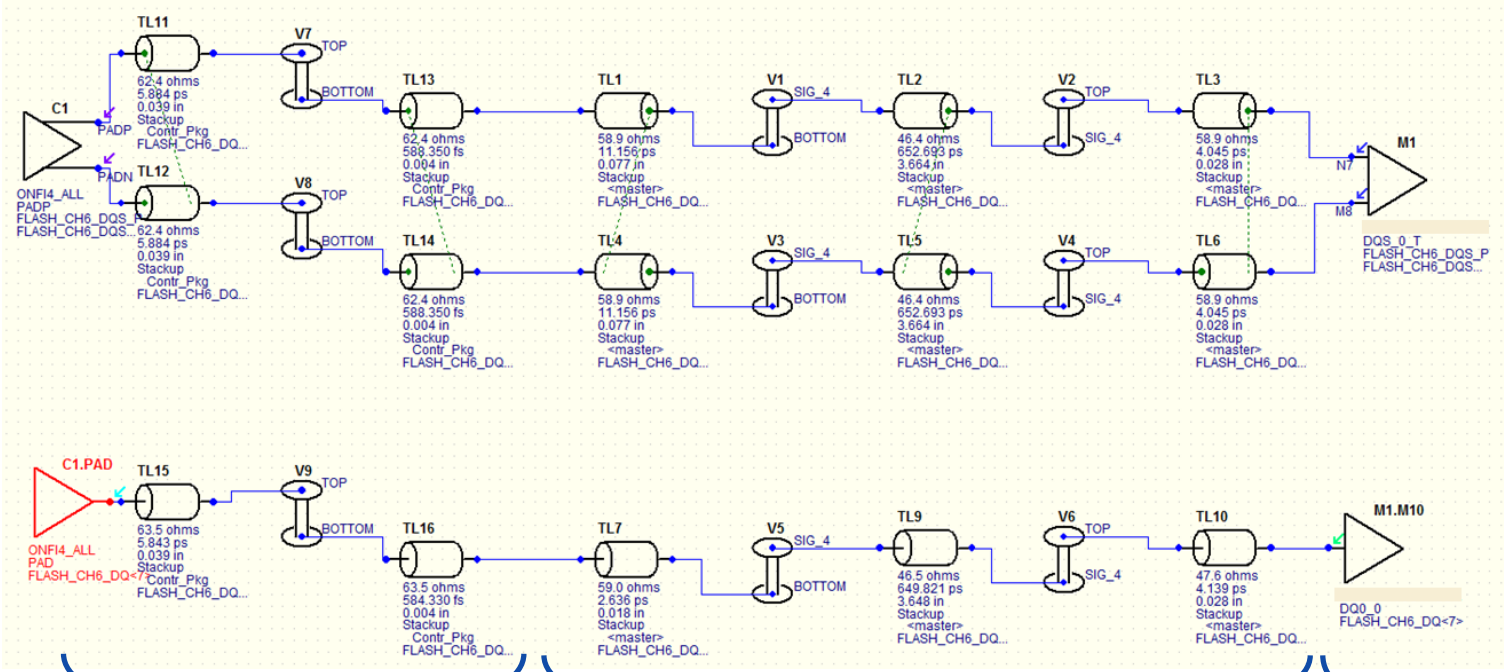
Pre-layout Simulation Checklist

What you will need:

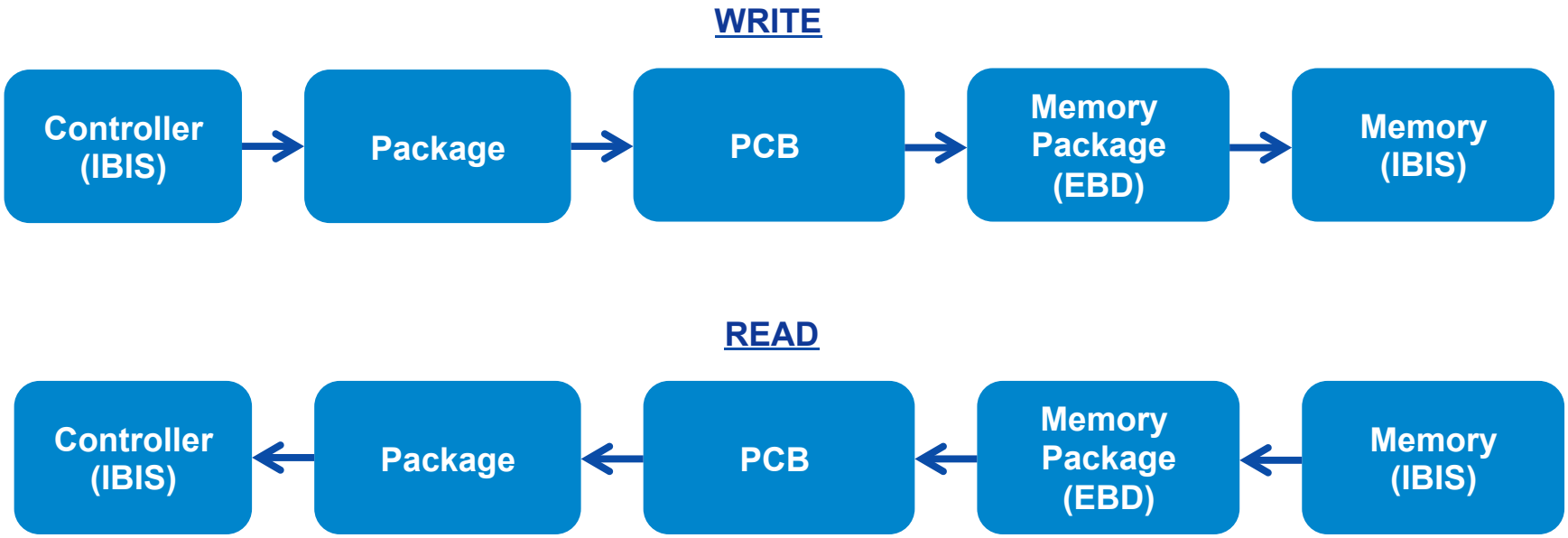
- ✓ Controller IBIS file (includes drive strength and terminations)
- ✓ Package stackup, via and trace length
- ✓ PCB stackup, via and trace length
- ✓ Memory EBD(Electrical Board Description) and IBIS files (includes drive strength and terminations)

Flash Memory Summit

Pre-layout



System SI Flow



Sweep Manager

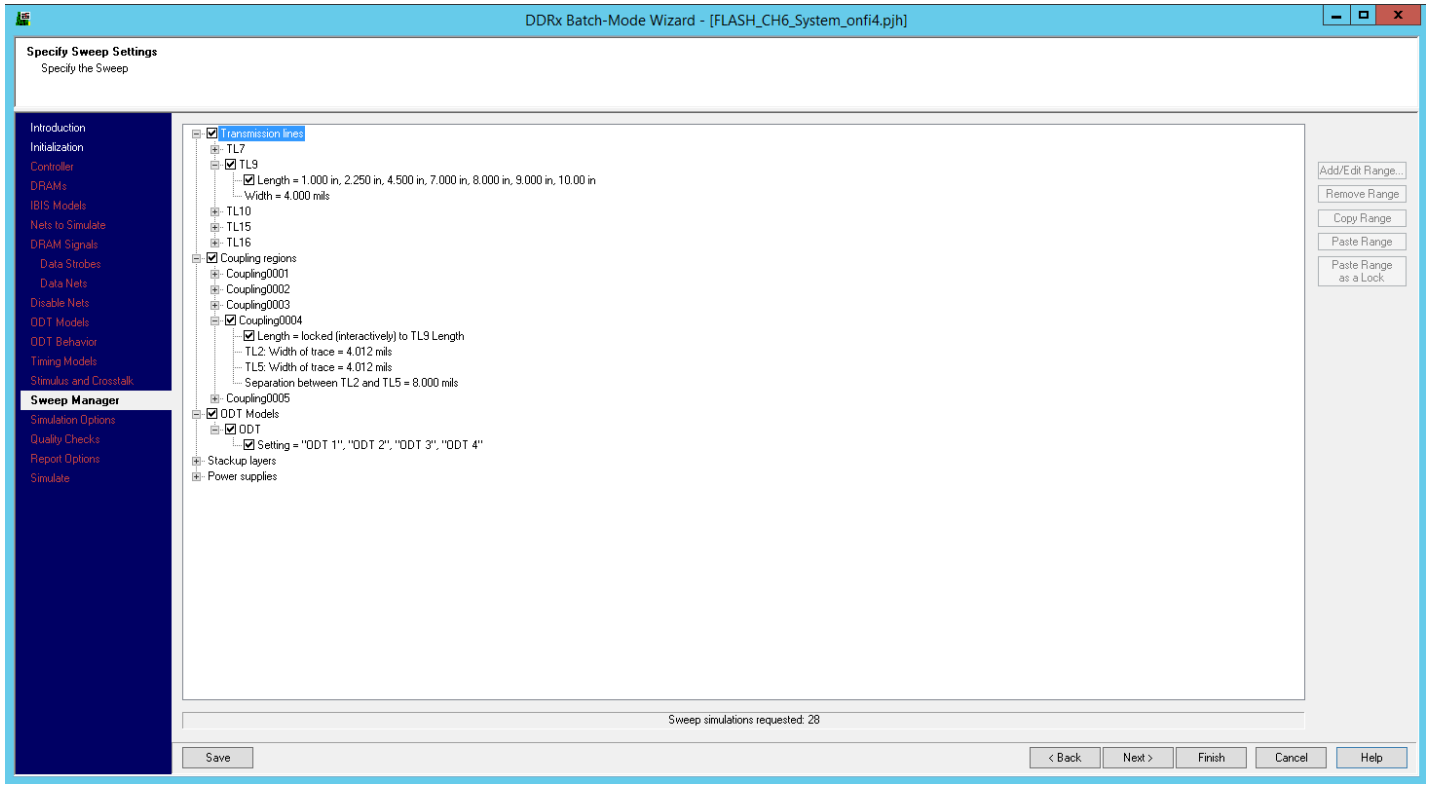
We can vary the following parameters:

- Package trace length
- PCB trace length
- Drive strength
- ODT settings

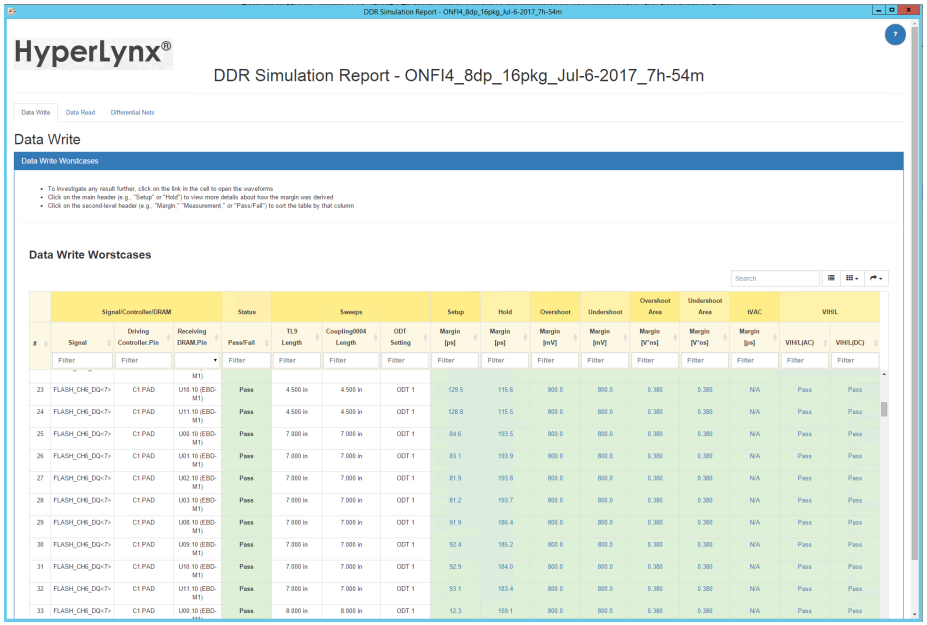
Results:

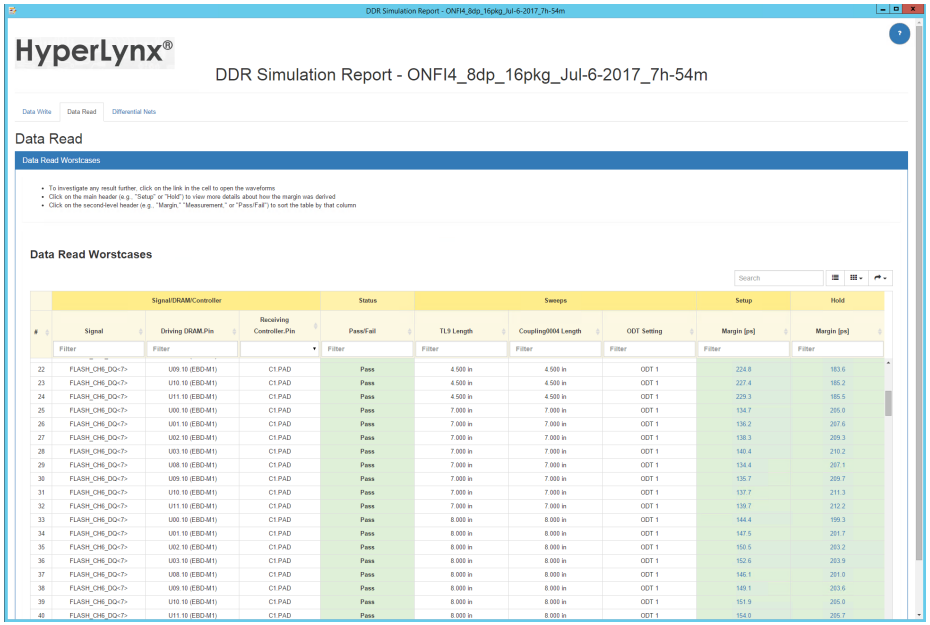
- Validate timing pass ONFI standard

Sweep Manager



Pre-layout Results





READ/WRITE passed up to 8 inches of PCB length(8 devices Load)

Post-layout Controller Package and PCB Checklist

Check Package Design for:

- Impedance, Insertion Loss
- Crosstalk in dB for DQ nets
- Trace Length skew between DQ and Strobe

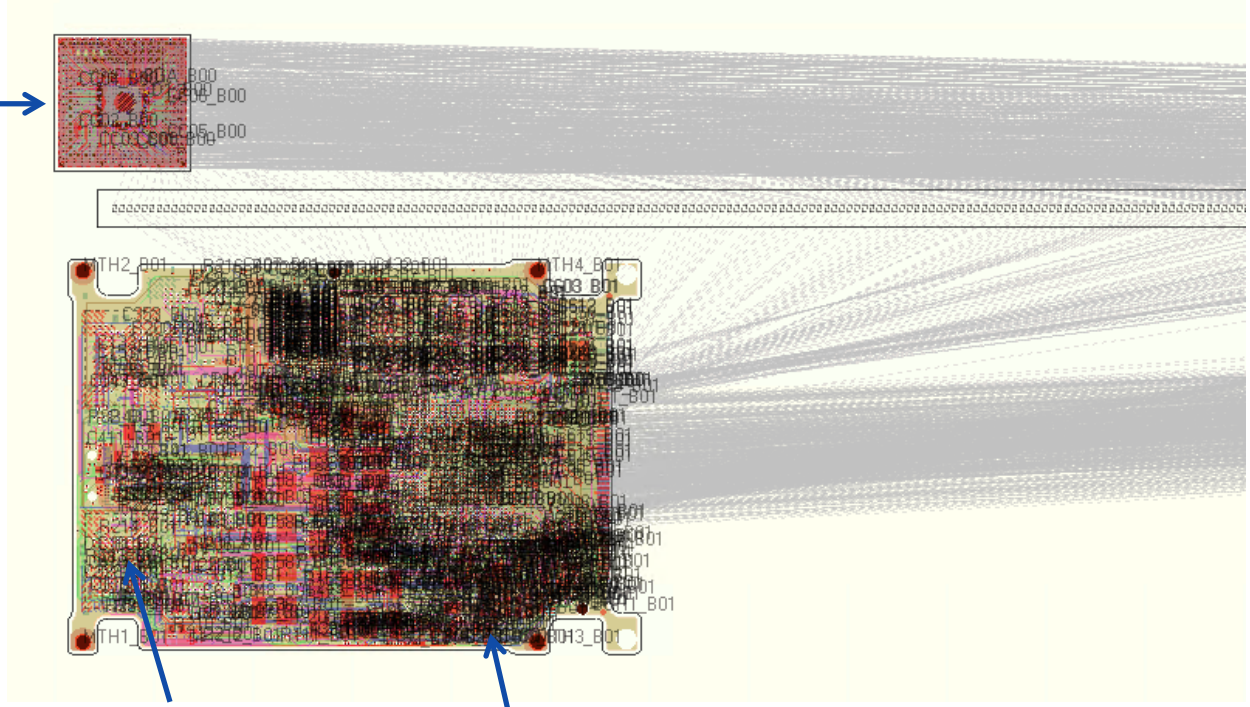
Check PCB Design for:

- Impedance, Insertion Loss
- Crosstalk in dB for DQ nets
- Trace Length skew between DQ and Strobe

Check IBIS files for:

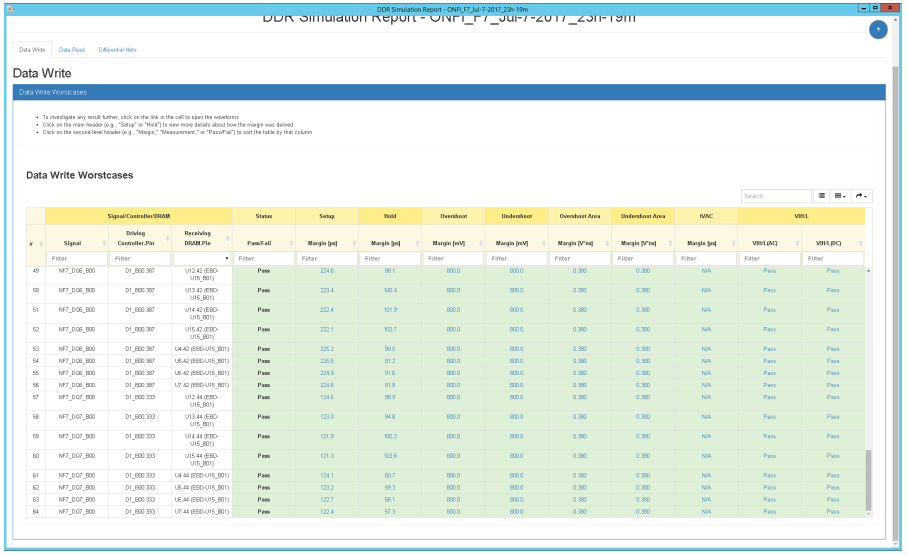
- Monotonic

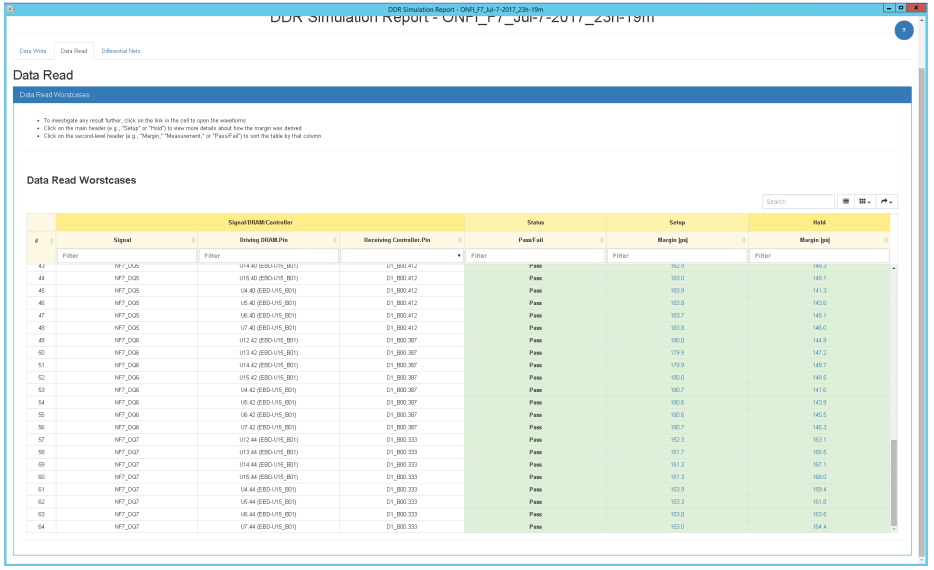
Post Layout (Die - Package - PCB)



Flash Memory Summit

Post-layout Result





READ/WRITE passed 4 inches of PCB length, confirming pre-layout simulations

Summary

- Use Pre-layout to determine electrical constraints
  - Sweep parameters to find optimal solutions that pass ONFI spec
- Layout the Package/PCB based on optimal solutions
- Use Post-layout to verify Pre-layout results

THANK YOU