



Using Simulations to Generate Relevant PCB Constraints for Flash Systems

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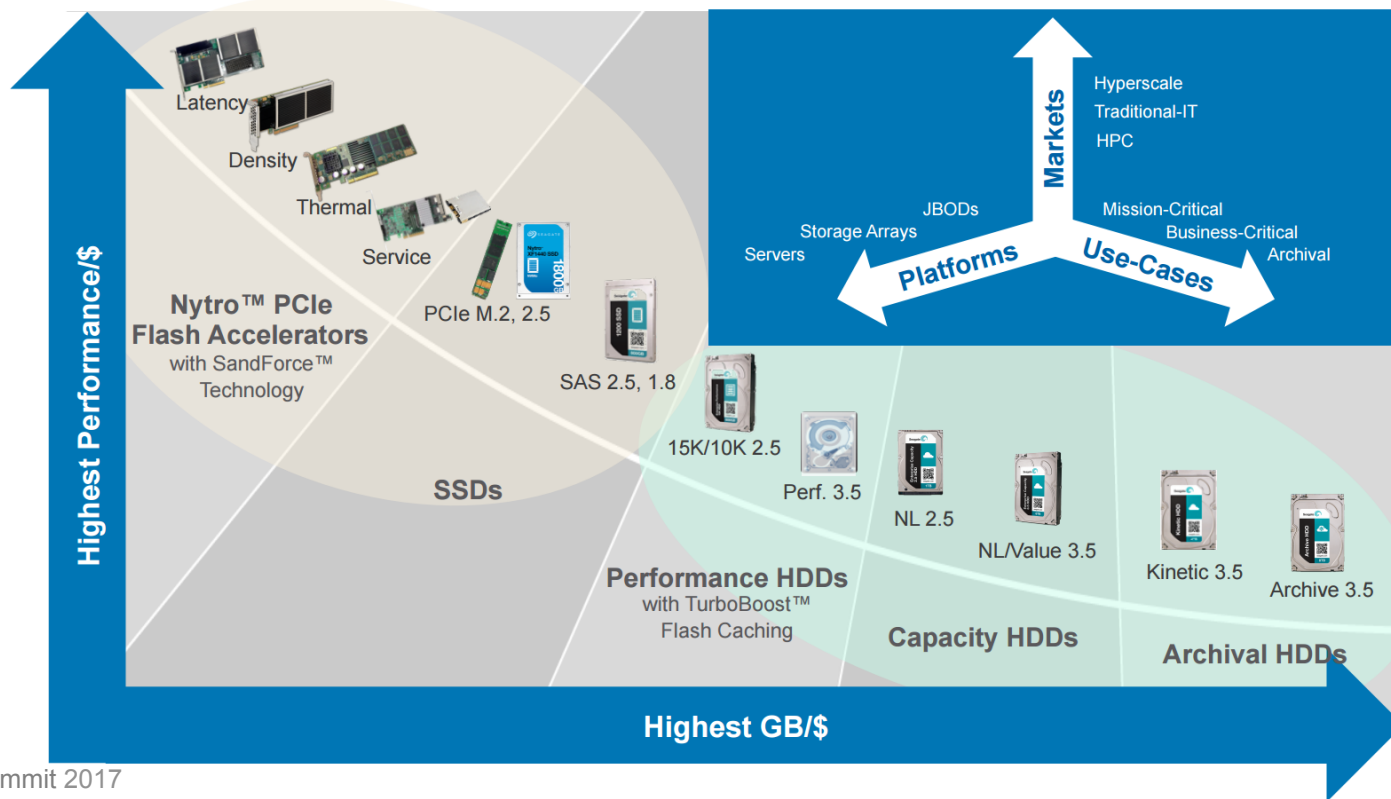
Agenda

- Seagate Background
- Problem Statement
- Solution
- Pre-layout and Checklist
 - Sweep Manager
- Post-layout and Checklist
- Summary



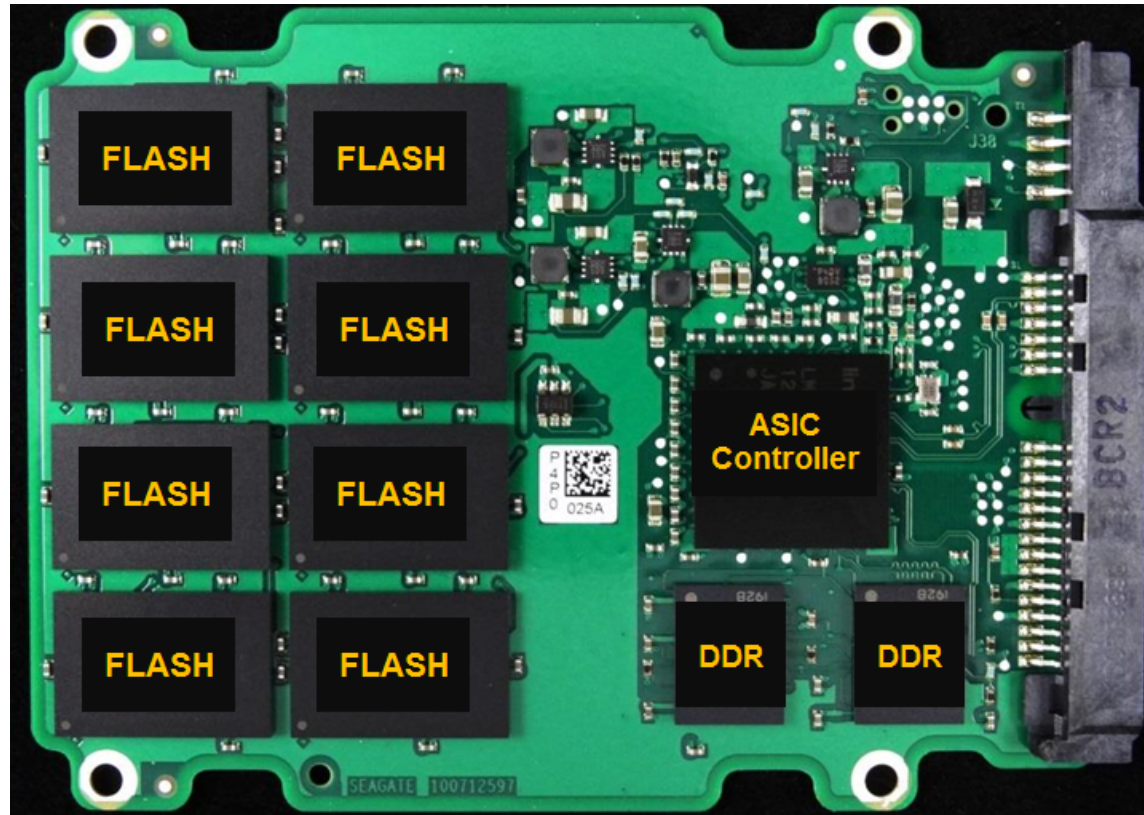
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Seagate Product Portfolio



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Flash SSD Drive





Problem Statements

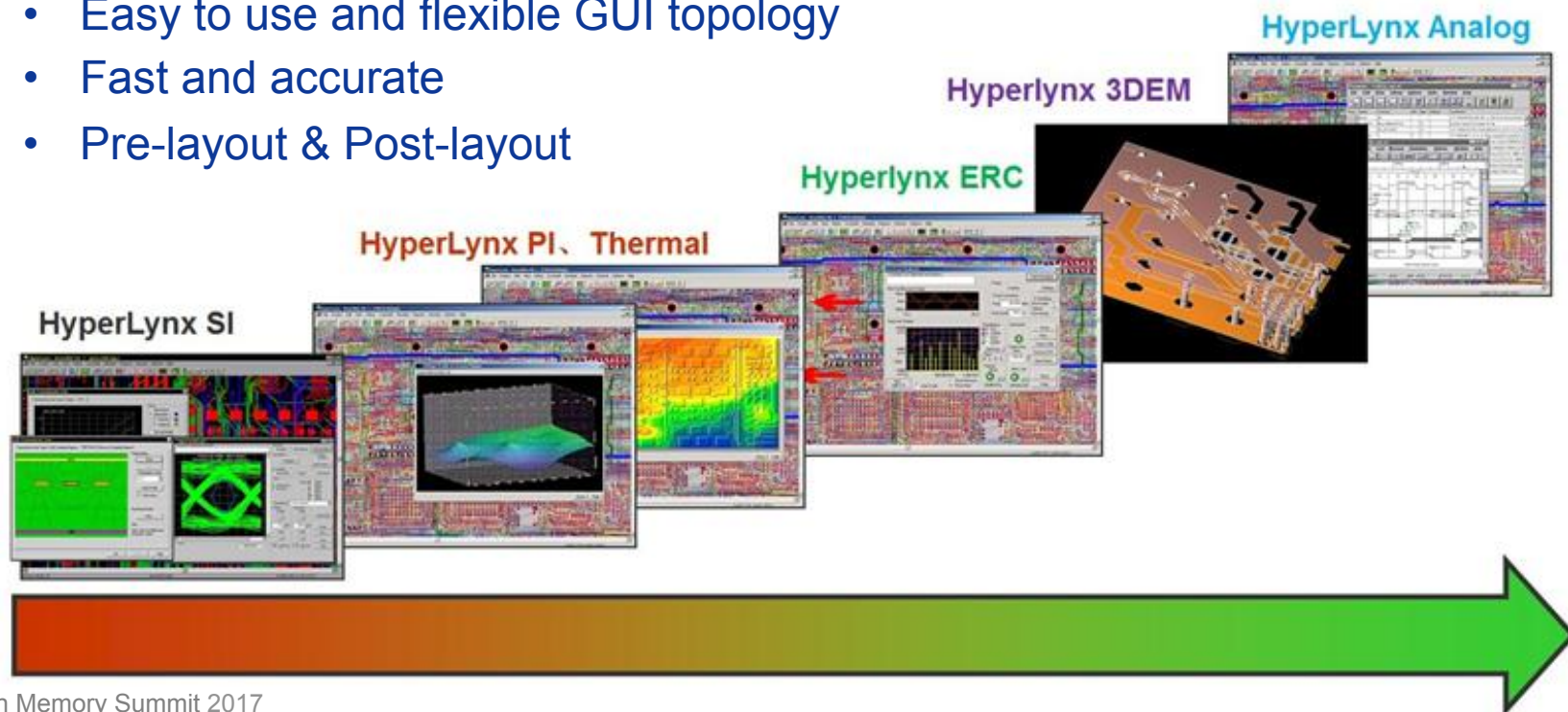
- Demand for higher capacity, more flash devices(16+ loads) per package
- Demand for higher speed, ONFI 4.0 @ 800MTS
- Challenging System Signal Integrity
- System failure without robust Signal Integrity



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Solution

- Easy to use and flexible GUI topology
- Fast and accurate
- Pre-layout & Post-layout





Pre-layout Simulation Checklist

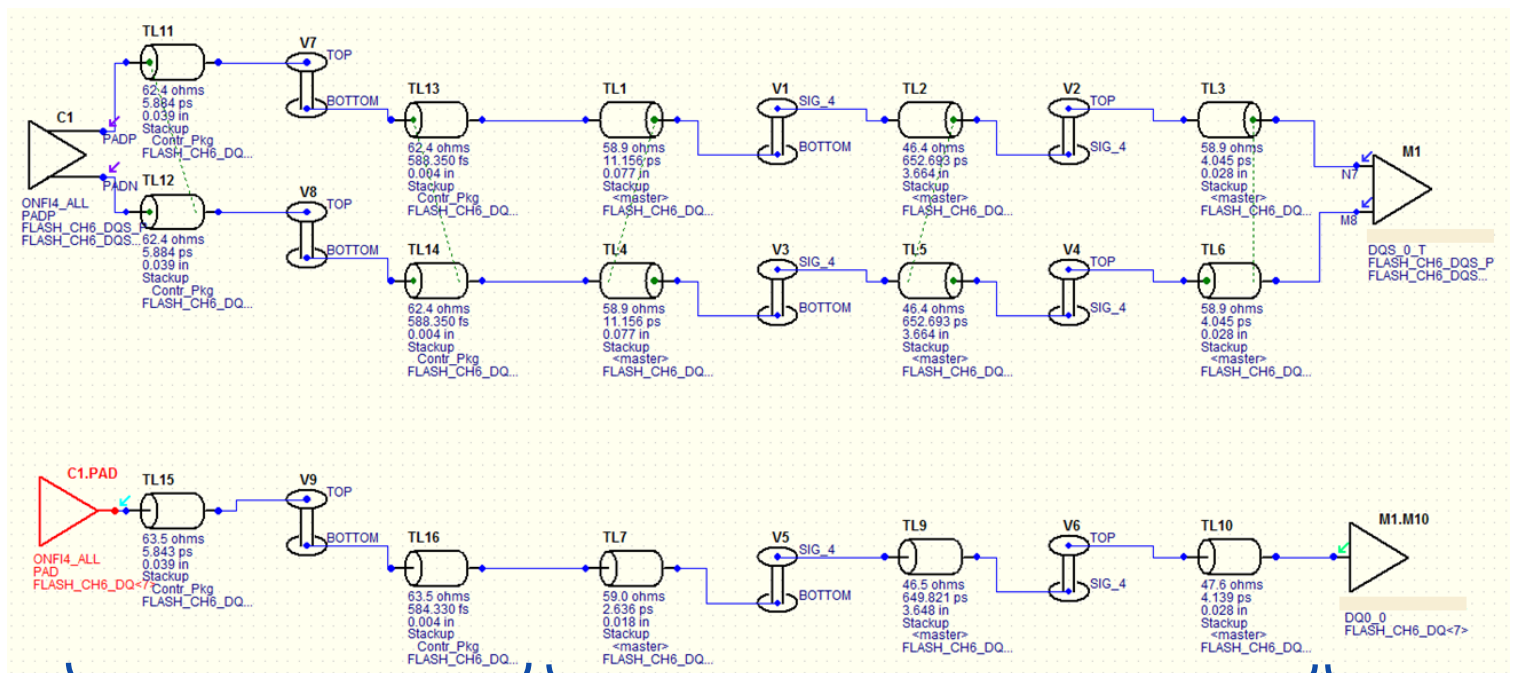
What you will need:

- ✓ Controller IBIS file (includes drive strength and terminations)
- ✓ Package stackup, via and trace length
- ✓ PCB stackup, via and trace length
- ✓ Memory EBD(Electrical Board Description) and IBIS files (includes drive strength and terminations)



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Pre-layout



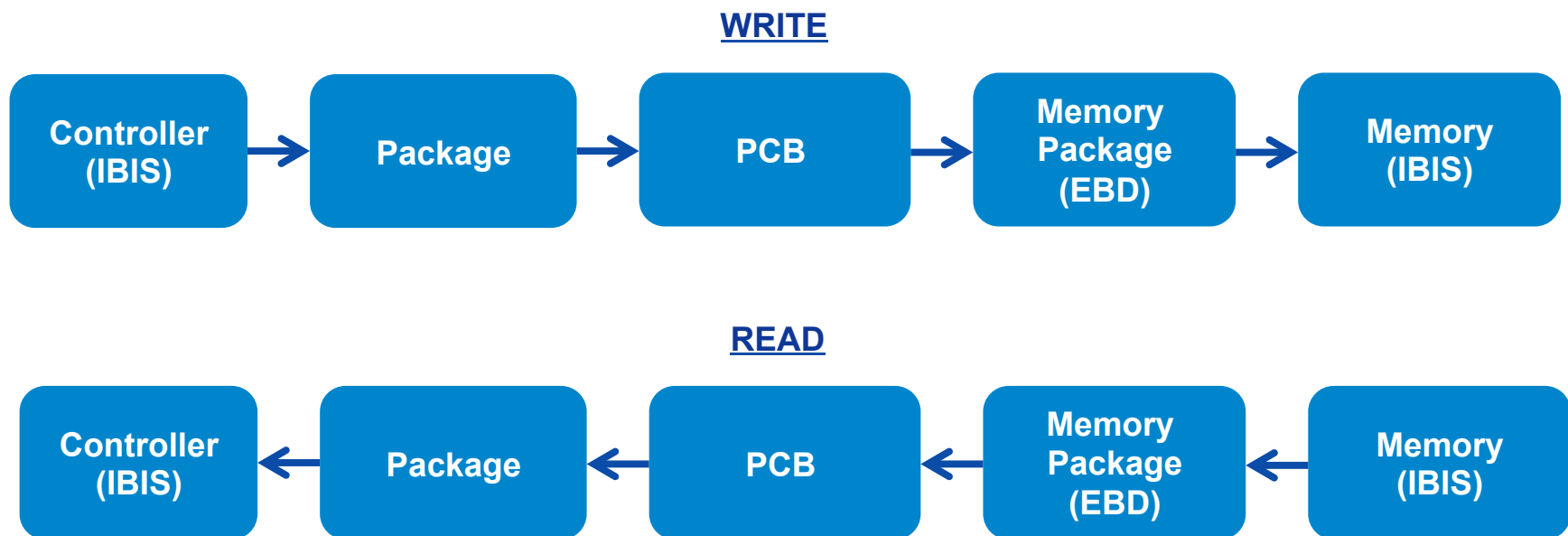
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**Controller
PACKAGE**

PCB

**Memory
PACKAGE**

System SI Flow





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Sweep Manager

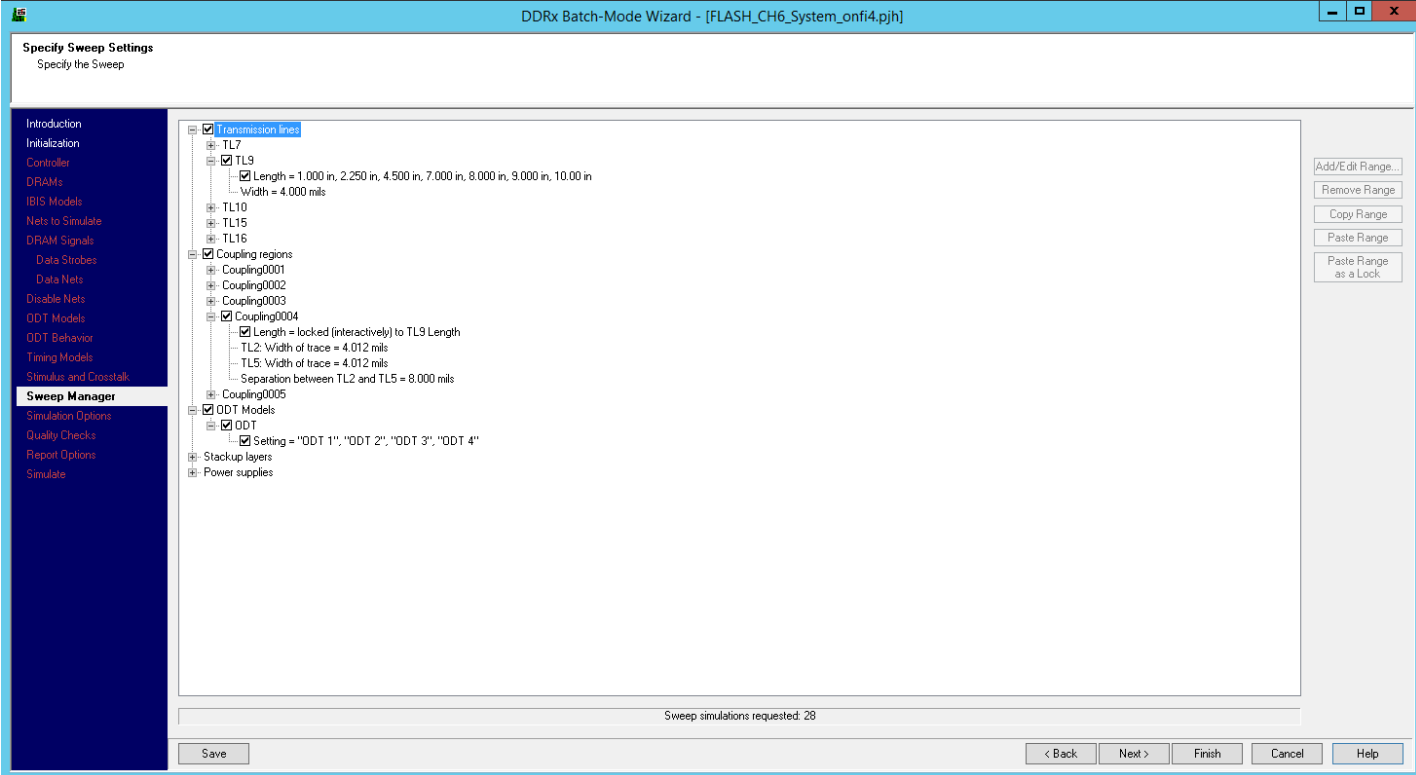
We can vary the following parameters:

- Package trace length
- PCB trace length
- Drive strength
- ODT settings

Results:

- Validate timing pass ONFI standard

Sweep Manager



DDRx Batch-Mode Wizard - [FLASH_CH6_System_onf4.pjh]

Specify Sweep Settings
Specify the Sweep

- Transmission lines
 - TL7
 - TL9
 - Length = 1,000 in, 2,250 in, 4,500 in, 7,000 in, 8,000 in, 9,000 in, 10,00 in
 - Width = 4,000 mils
 - TL10
 - TL15
 - TL16
- Coupling regions
 - Coupling0001
 - Coupling0002
 - Coupling0003
 - Coupling0004
 - Length = locked (interactively) to TL9 Length
 - TL2: Width of trace = 4,012 mils
 - TL5: Width of trace = 4,012 mils
 - Separation between TL2 and TL5 = 8,000 mils
 - Coupling0005
- ODT Models
 - ODT
 - Setting = "ODT 1", "ODT 2", "ODT 3", "ODT 4"
- Stackup layers
- Power supplies

Sweep simulations requested: 28

Save < Back Next > Finish Cancel Help



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Pre-layout Results

HyperLynx®
DDR Simulation Report - ONFI4_8dp_16pkg_Jul-6-2017_7h-54m

Data Write

Data Write Worstcases

- To investigate any result further, click on the link in the cell to open the waveform.
- Click on the main header (e.g., "Setup" or "Hold") to view more details about how the margin was derived.
- Click on the second-level header (e.g., "Margin," "Measurement," or "Pass/Fail") to sort the table by that column.

Data Write Worstcases

#	Signal/DRAM/Controller			Status	Sweeps			Setup		Hold	Overshoot		Undershoot		Overshoot Area		Undershoot Area		WAC	VIRL	
	Signal	Driving Controller Pin	Receiving DRAM Pin		Pass/Fail	TL9 Length	Coupling/004 Length	ODT Setting	Margin [ps]		Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]	Margin [ps]		VIRL(A)	VIRL(D)
23	FLASH_CH0_DQ-7*	C1 PAD	U10 10 (E8D-M)	Pass	4.500 in	4.500 in	ODT 1	129.5	115.6	800.0	800.0	0.380	0.380	N/A	Pass	Pass					
24	FLASH_CH0_DQ-7*	C1 PAD	U11 10 (E8D-M)	Pass	4.500 in	4.500 in	ODT 1	128.8	115.5	800.0	800.0	0.380	0.380	N/A	Pass	Pass					
25	FLASH_CH0_DQ-7*	C1 PAD	U08 10 (E8D-M)	Pass	7.000 in	7.000 in	ODT 1	84.6	193.5	800.0	800.0	0.380	0.380	N/A	Pass	Pass					
26	FLASH_CH0_DQ-7*	C1 PAD	U01 10 (E8D-M)	Pass	7.000 in	7.000 in	ODT 1	83.1	193.9	800.0	800.0	0.380	0.380	N/A	Pass	Pass					
27	FLASH_CH0_DQ-7*	C1 PAD	U02 10 (E8D-M)	Pass	7.000 in	7.000 in	ODT 1	81.9	193.0	800.0	800.0	0.380	0.380	N/A	Pass	Pass					
28	FLASH_CH0_DQ-7*	C1 PAD	U03 10 (E8D-M)	Pass	7.000 in	7.000 in	ODT 1	81.2	193.7	800.0	800.0	0.380	0.380	N/A	Pass	Pass					
29	FLASH_CH0_DQ-7*	C1 PAD	U06 10 (E8D-M)	Pass	7.000 in	7.000 in	ODT 1	81.9	195.4	800.0	800.0	0.380	0.380	N/A	Pass	Pass					
30	FLASH_CH0_DQ-7*	C1 PAD	U09 10 (E8D-M)	Pass	7.000 in	7.000 in	ODT 1	82.4	195.2	800.0	800.0	0.380	0.380	N/A	Pass	Pass					
31	FLASH_CH0_DQ-7*	C1 PAD	U10 10 (E8D-M)	Pass	7.000 in	7.000 in	ODT 1	82.9	194.0	800.0	800.0	0.380	0.380	N/A	Pass	Pass					
32	FLASH_CH0_DQ-7*	C1 PAD	U11 10 (E8D-M)	Pass	7.000 in	7.000 in	ODT 1	83.1	193.4	800.0	800.0	0.380	0.380	N/A	Pass	Pass					
33	FLASH_CH0_DQ-7*	C1 PAD	U00 10 (E8D-M)	Pass	8.000 in	8.000 in	ODT 1	12.3	193.1	800.0	800.0	0.380	0.380	N/A	Pass	Pass					

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DDR Simulation Report - ONFI4_8dp_16pkg_Jul-6-2017_7h-54m

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Data Read Worstcases

#	Signal/DRAM/Controller			Status	Sweeps			Setup		Hold
	Signal	Driving DRAM Pin	Receiving Controller Pin		Pass/Fail	TL9 Length	Coupling/004 Length	ODT Setting	Margin [ps]	
22	FLASH_CH0_DQ-7*	U09 10 (E8D-M)	C1 PAD	Pass	4.500 in	4.500 in	ODT 1	224.8	183.6	
23	FLASH_CH0_DQ-7*	U10 10 (E8D-M)	C1 PAD	Pass	4.500 in	4.500 in	ODT 1	227.4	186.2	
24	FLASH_CH0_DQ-7*	U11 10 (E8D-M)	C1 PAD	Pass	4.500 in	4.500 in	ODT 1	225.3	186.6	
25	FLASH_CH0_DQ-7*	U08 10 (E8D-M)	C1 PAD	Pass	7.000 in	7.000 in	ODT 1	134.7	255.0	
26	FLASH_CH0_DQ-7*	U01 10 (E8D-M)	C1 PAD	Pass	7.000 in	7.000 in	ODT 1	136.2	257.6	
27	FLASH_CH0_DQ-7*	U02 10 (E8D-M)	C1 PAD	Pass	7.000 in	7.000 in	ODT 1	138.3	259.3	
28	FLASH_CH0_DQ-7*	U03 10 (E8D-M)	C1 PAD	Pass	7.000 in	7.000 in	ODT 1	140.4	210.2	
29	FLASH_CH0_DQ-7*	U06 10 (E8D-M)	C1 PAD	Pass	7.000 in	7.000 in	ODT 1	134.4	207.1	
30	FLASH_CH0_DQ-7*	U09 10 (E8D-M)	C1 PAD	Pass	7.000 in	7.000 in	ODT 1	135.7	209.7	
31	FLASH_CH0_DQ-7*	U10 10 (E8D-M)	C1 PAD	Pass	7.000 in	7.000 in	ODT 1	137.7	211.3	
32	FLASH_CH0_DQ-7*	U11 10 (E8D-M)	C1 PAD	Pass	7.000 in	7.000 in	ODT 1	139.7	212.2	
33	FLASH_CH0_DQ-7*	U00 10 (E8D-M)	C1 PAD	Pass	8.000 in	8.000 in	ODT 1	144.4	199.3	
34	FLASH_CH0_DQ-7*	U01 10 (E8D-M)	C1 PAD	Pass	8.000 in	8.000 in	ODT 1	147.5	201.7	
35	FLASH_CH0_DQ-7*	U02 10 (E8D-M)	C1 PAD	Pass	8.000 in	8.000 in	ODT 1	150.5	203.2	
36	FLASH_CH0_DQ-7*	U03 10 (E8D-M)	C1 PAD	Pass	8.000 in	8.000 in	ODT 1	152.6	203.9	
37	FLASH_CH0_DQ-7*	U06 10 (E8D-M)	C1 PAD	Pass	8.000 in	8.000 in	ODT 1	146.1	201.0	
38	FLASH_CH0_DQ-7*	U09 10 (E8D-M)	C1 PAD	Pass	8.000 in	8.000 in	ODT 1	148.1	203.6	
39	FLASH_CH0_DQ-7*	U10 10 (E8D-M)	C1 PAD	Pass	8.000 in	8.000 in	ODT 1	151.9	205.0	
40	FLASH_CH0_DQ-7*	U11 10 (E8D-M)	C1 PAD	Pass	8.000 in	8.000 in	ODT 1	154.0	205.7	

READ/WRITE passed up to 8 inches of PCB length(8 devices Load)

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Post-layout Controller Package and PCB Checklist

Check Package Design for:

- Impedance, Insertion Loss
- Crosstalk in dB for DQ nets
- Trace Length skew between DQ and Strobe

Check PCB Design for:

- Impedance, Insertion Loss
- Crosstalk in dB for DQ nets
- Trace Length skew between DQ and Strobe

Check IBIS files for:

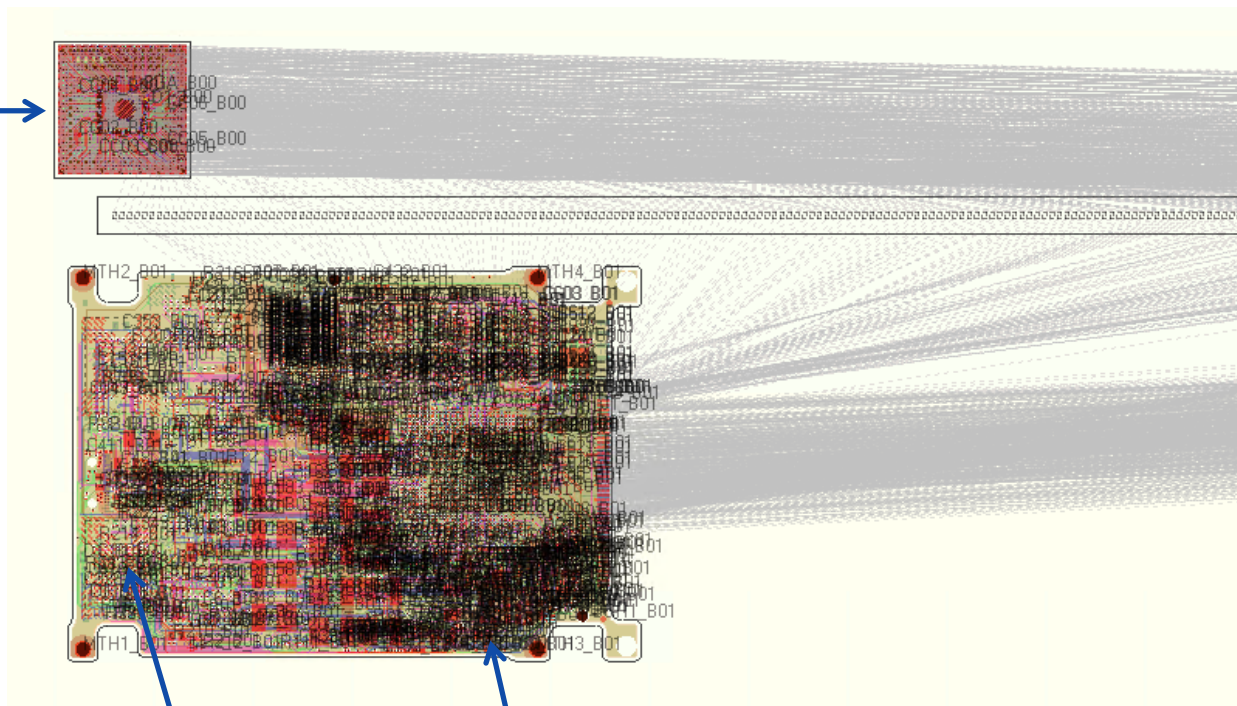
- Monotonic



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Post Layout (Die - Package - PCB)

Controller Package →



Memory Package

PCB(Trace length is around 4 inches)

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Post-layout Result

DDR Simulation Report - ONFI_F7_Jul-7-2017_23h-19m

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Data Write Worstcases

#	Signal/Controller/DRAM			Status	Setup	Hold	Overclock	Underclock	Overclock Area		Underclock Area		MVC	VBL	
	Signal	Controller.Pis	Receiving DRAM.Pis						Margin [ns]	Margin [ns]	Margin [ns]	Margin [ns]		VBL(DI)	VBL(DQ)
45	NFT_106_800	D1_800_367	U15 A1 (E8D-U16_800)	Pass	224.6	95.1	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
50	NFT_106_800	D1_800_367	U15 A2 (E8D-U16_800)	Pass	221.4	101.4	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
51	NFT_106_800	D1_800_367	U15 A3 (E8D-U16_800)	Pass	222.4	101.9	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
52	NFT_106_800	D1_800_367	U15 A4 (E8D-U16_800)	Pass	223.1	102.7	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
53	NFT_106_800	D1_800_367	U16 A0 (E8D-U16_800)	Pass	225.2	105.6	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
54	NFT_106_800	D1_800_367	U16 A1 (E8D-U16_800)	Pass	225.5	111.2	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
55	NFT_106_800	D1_800_367	U16 A2 (E8D-U16_800)	Pass	224.9	111.6	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
56	NFT_106_800	D1_800_367	U16 A3 (E8D-U16_800)	Pass	224.6	111.8	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
57	NFT_107_800	D1_800_333	U16 A0 (E8D-U16_800)	Pass	124.6	80.9	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
58	NFT_107_800	D1_800_333	U16 A1 (E8D-U16_800)	Pass	123.0	84.8	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
59	NFT_107_800	D1_800_333	U16 A2 (E8D-U16_800)	Pass	121.9	100.2	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
60	NFT_107_800	D1_800_333	U16 A3 (E8D-U16_800)	Pass	121.9	103.6	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
61	NFT_107_800	D1_800_333	U16 A4 (E8D-U16_800)	Pass	124.1	107.7	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
62	NFT_107_800	D1_800_333	U16 A0 (E8D-U16_800)	Pass	122.2	59.3	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
63	NFT_107_800	D1_800_333	U16 A1 (E8D-U16_800)	Pass	122.7	59.1	800.0	800.0	0.300	0.300	N/A	Pass	Pass		
64	NFT_107_800	D1_800_333	U16 A2 (E8D-U16_800)	Pass	122.4	57.3	800.0	800.0	0.300	0.300	N/A	Pass	Pass		

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Data Read Worstcases

#	Signal/DRAM Controller			Status	Setup	Hold
	Signal	Driving DRAM.Pis	Receiving Controller.Pis			
44	Filter	Filter	U14 A0 (E8D-U16_800)	Pass	Filter	Filter
44	NFT_106	U15 A0 (E8D-U16_800)	D1_800_412	Pass	93.9	148.3
45	NFT_106	U15 A1 (E8D-U16_800)	D1_800_412	Pass	93.9	141.3
46	NFT_106	U15 A2 (E8D-U16_800)	D1_800_412	Pass	93.9	143.6
47	NFT_106	U15 A3 (E8D-U16_800)	D1_800_412	Pass	93.7	145.1
48	NFT_106	U16 A0 (E8D-U16_800)	D1_800_412	Pass	93.8	146.0
49	NFT_106	U16 A1 (E8D-U16_800)	D1_800_367	Pass	90.0	144.9
50	NFT_106	U16 A2 (E8D-U16_800)	D1_800_367	Pass	179.9	147.2
51	NFT_106	U16 A3 (E8D-U16_800)	D1_800_367	Pass	179.9	148.7
52	NFT_106	U16 A4 (E8D-U16_800)	D1_800_367	Pass	90.0	149.5
53	NFT_106	U16 A0 (E8D-U16_800)	D1_800_367	Pass	90.7	141.6
54	NFT_106	U16 A1 (E8D-U16_800)	D1_800_367	Pass	90.6	143.9
55	NFT_106	U16 A2 (E8D-U16_800)	D1_800_367	Pass	90.0	146.5
56	NFT_106	U16 A3 (E8D-U16_800)	D1_800_367	Pass	90.7	148.3
57	NFT_107	U15 A4 (E8D-U16_800)	D1_800_333	Pass	92.3	163.1
58	NFT_107	U15 A0 (E8D-U16_800)	D1_800_333	Pass	151.7	165.5
59	NFT_107	U15 A1 (E8D-U16_800)	D1_800_333	Pass	151.3	167.1
60	NFT_107	U15 A2 (E8D-U16_800)	D1_800_333	Pass	151.3	168.0
61	NFT_107	U15 A3 (E8D-U16_800)	D1_800_333	Pass	153.9	169.4
62	NFT_107	U16 A4 (E8D-U16_800)	D1_800_333	Pass	153.3	161.6
63	NFT_107	U16 A0 (E8D-U16_800)	D1_800_333	Pass	153.0	163.5
64	NFT_107	U16 A1 (E8D-U16_800)	D1_800_333	Pass	153.0	164.4

READ/WRITE passed 4 inches of PCB length, confirming pre-layout simulations

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Summary

- Use Pre-layout to determine electrical constraints
 - Sweep parameters to find optimal solutions that pass ONFI spec
- Layout the Package/PCB based on optimal solutions
- Use Post-layout to verify Pre-layout results



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THANK YOU