



Flash Memory Summit

# ReRAM Technology, Versatility, and Readiness

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*VP of Engineering & Cofounder*

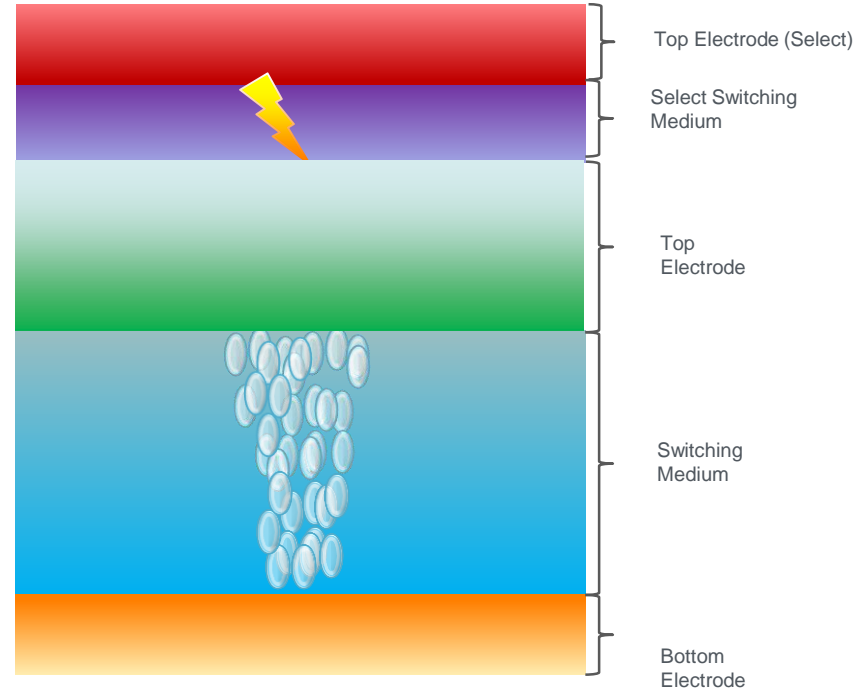
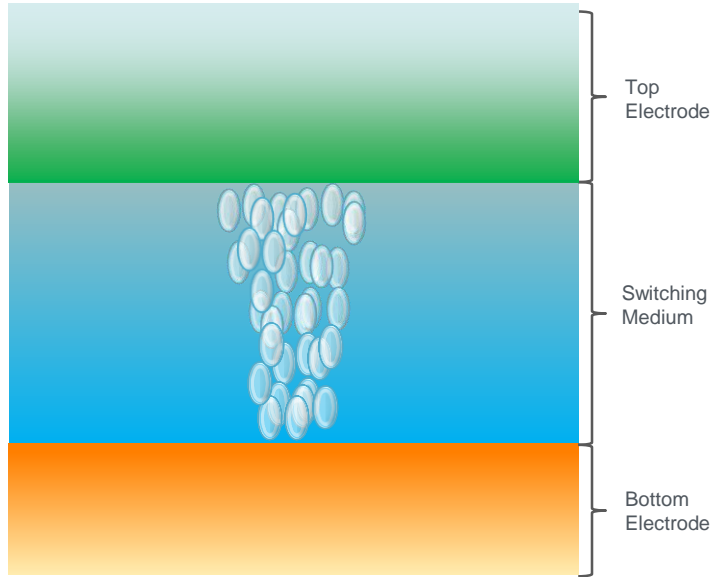


- Introduction to ReRAM
- ReRAM Technology Attributes
  - Scalability
  - Ease of integration with CMOS
  - Architectural Flexibility
  - Energy reduction
- 40nm ReRAM Product results
  - Performance
  - Endurance
  - Retention
- Status & Conclusion



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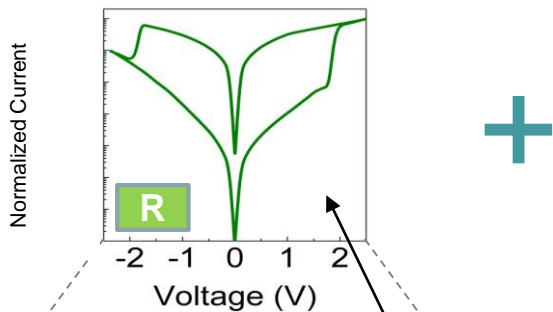
# Filamentary ReRAM technologies leads to a simple yet powerful non-volatile technology





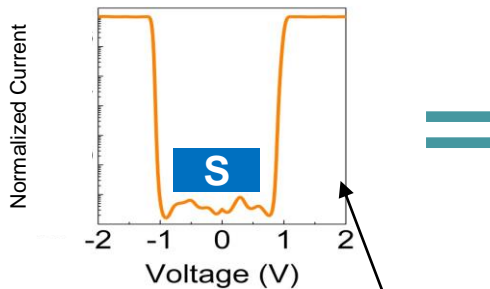
# Wide range of applications with ReRAM

## Crossbar **Re**RAM Cell



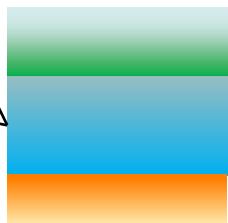
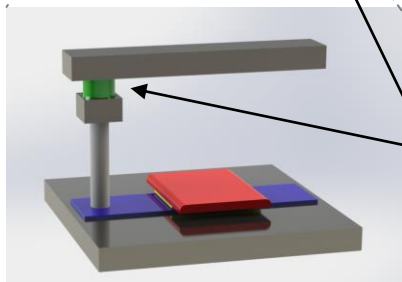
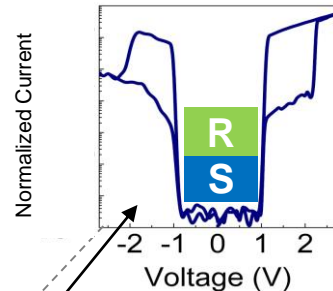
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## Crossbar **S**elector

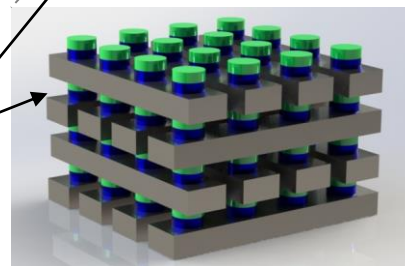


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## Crossbar **S**R Cell



Suited for low latency, high speed  
embedded memory



Suited for high density high performance  
NAND or SCM memory

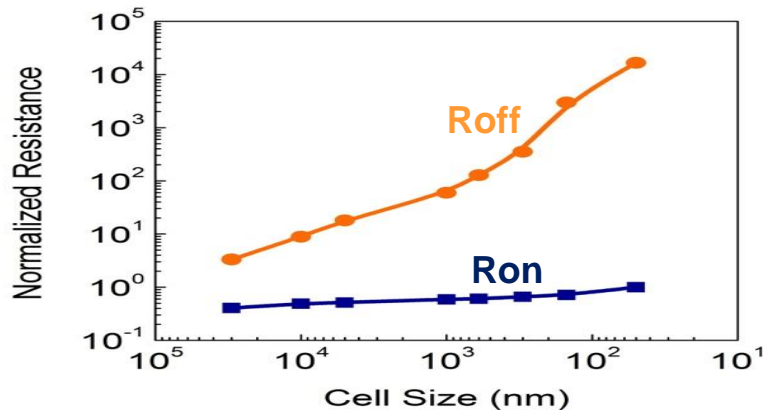


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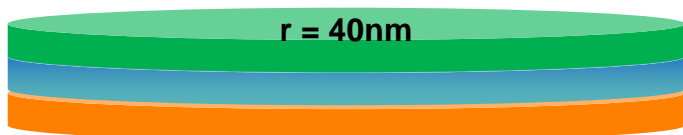
# ReRAM Technology Attributes



# ReRAM performance improves with scaling

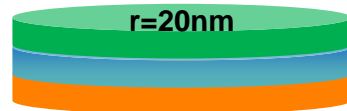


- Scaling ReRAM device
  - $R_{off} \propto \frac{1}{Cell\ Area}$
  - **R<sub>on</sub> Stays nearly constant**
- R<sub>off</sub>/R<sub>on</sub> ratio improves
- Sensing window improves
- Improves BER



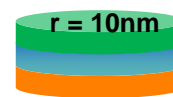
$I_{off}=1\mu A, R_{off}=1M\Omega, R_{on}=10K\Omega$

**R<sub>off</sub>/R<sub>on</sub>=100**



$I_{off}=0.25\mu A, R_{off}=4M\Omega, R_{on}=10K\Omega,$

**R<sub>off</sub>/R<sub>on</sub>=400**

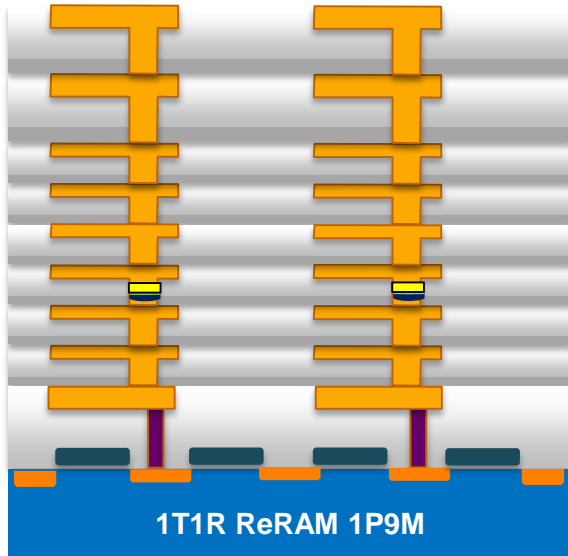


$I_{off}=62nA, R_{off}=16M\Omega, R_{on}=10K\Omega,$

**R<sub>off</sub>/R<sub>on</sub>=1600**



# Ease of integration with CMOS



- Back-end process – No impact to CMOS transistors
- ReRAM located between metal layers
- Adds only 1 to 2 masks & 8 processing steps
- 32% lower cost
- Smaller die size



# ReRAM enabling scalability, performance, monolithic integration

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Conventional Flash	ReRAM	Architectural Advantages
4 terminal device D/G/S/Substrate	2 terminal device	Smaller device Simpler to operate
Common substrate	Has no common terminal	Allows Byte alterability Byte Write
Front-end Impacts CMOS transistors	Back-end	Area efficiency No impact on CMOS transistors
Requires additional HV transistors	No HV transistors needed	Much easier to design and integrate with CMOS and uses 1 or 2 masks
Scaling Limitations or Degradations	No Scaling limitations or Degradations	Well Suited for advanced nodes Monolithic integration with CMOS





# Major system energy reduction with ReRam

Energy consumption ratio NAND/ReRAM based on SSD & NVDIMM-P						
Write Amplification	SSD			NVDIMM-P		
	512B Write			64B Write		
	NAND based SSD (nJ)	ReRAM(nJ)	ReRAM Energy Reduction	NAND based NVDIMM-P(nJ)	ReRAM(nJ)	ReRAM Energy Reduction
1	53056	21504	2X	53056	2688	20X
2	70947	21504	3X	70947	2688	26X
3	88838	21504	4X	88838	2688	33X
4	106729	21504	5X	106729	2688	40X

- ReRAM based SSD provides 2X to 5X energy reduction
- ReRAM based NVDIMM provides 20X to 40X energy reduction





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# ReRAM Product Array Results

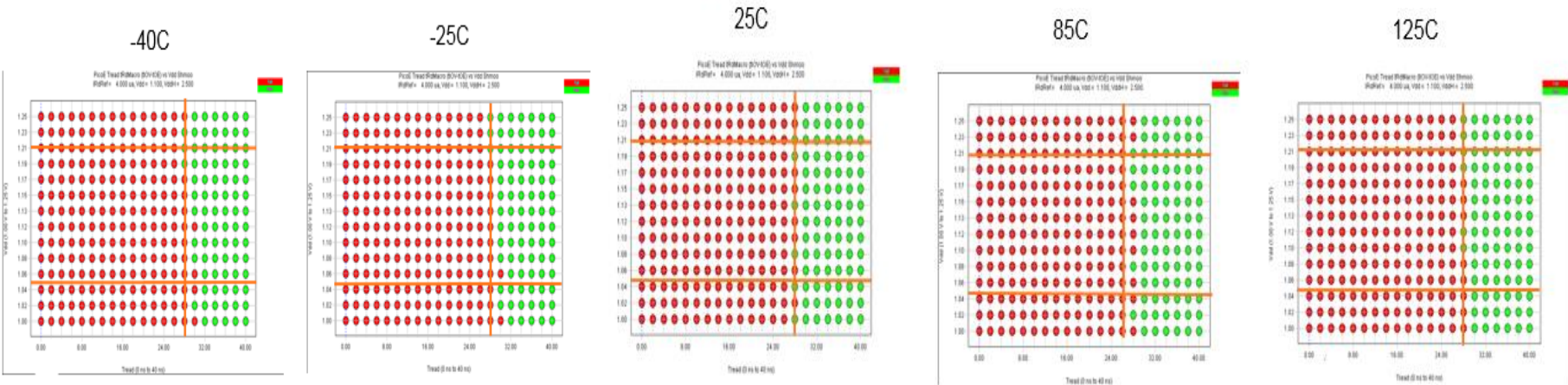
Performance

Endurance

Retention



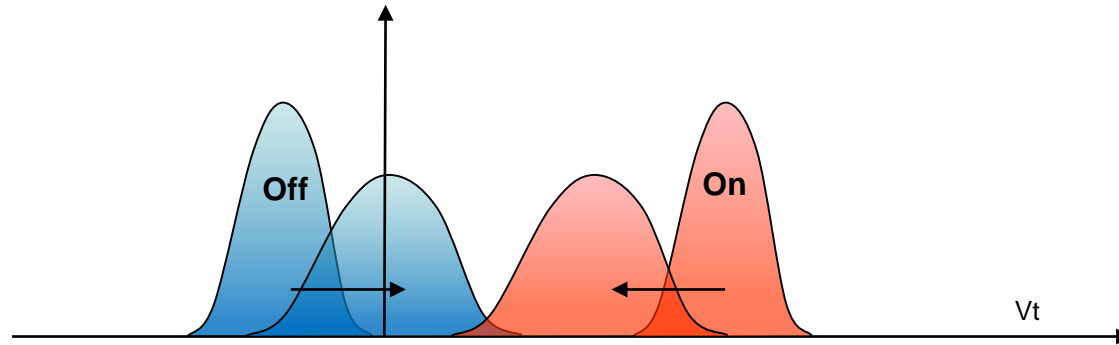
# Stable performance across VCC and wide temp range



- Superior Speed stability across temperature and VCC is established



## Problems with aging Flash technology



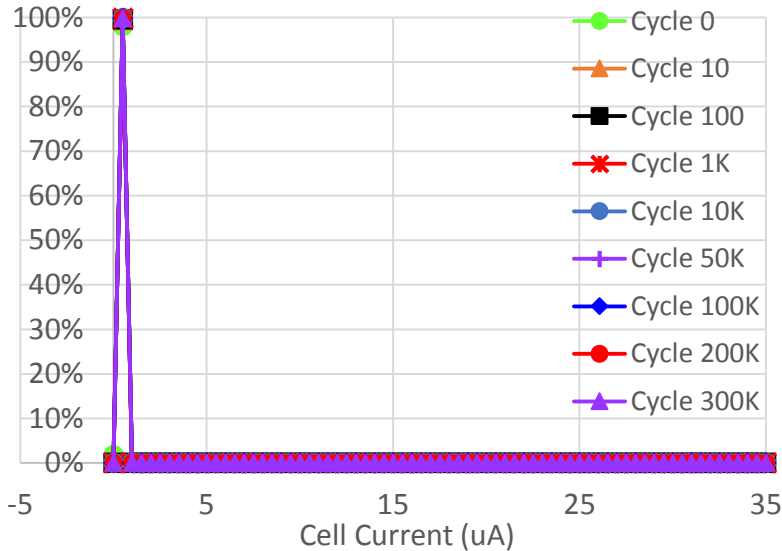
- Flash distributions widens
- Flash distribution gap closes increasing BER



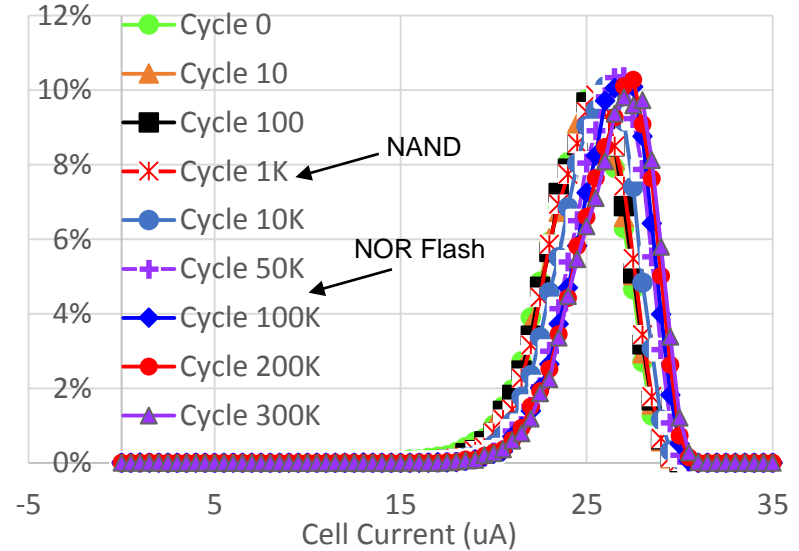
# 300K endurance cycles with no degradation

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32Kb Endurance Cycling



32Kb Endurance Cycling

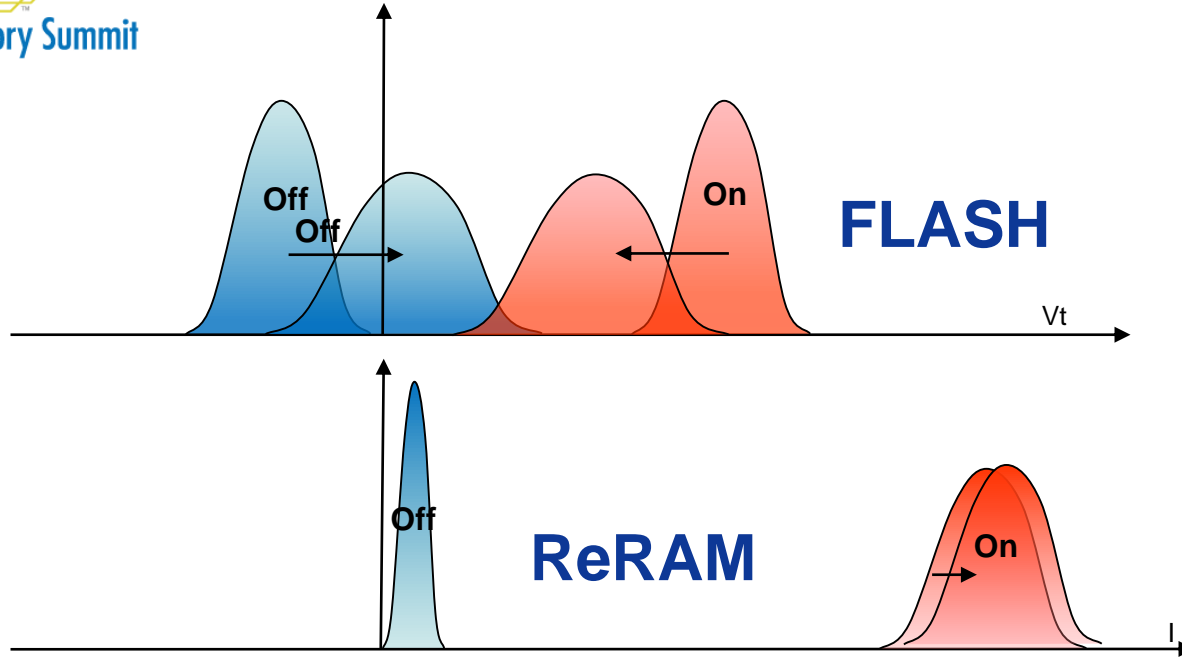


- ReRAM “On” and “Off” Distribution width stayed the same !!!
- ReRAM “On” and “Off” Distribution gap increased !!!



# ReRAM vs. Flash

## Distribution over endurance & retention

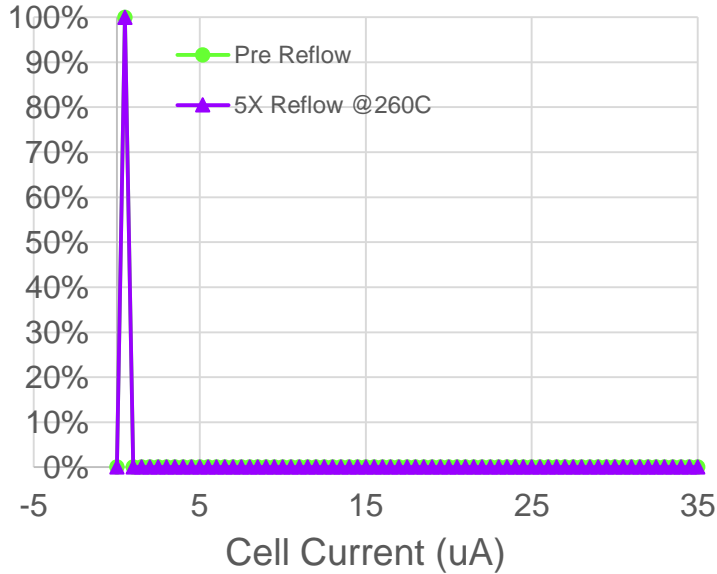


**ReRAM Distribution gap & width does not close or widen!!**

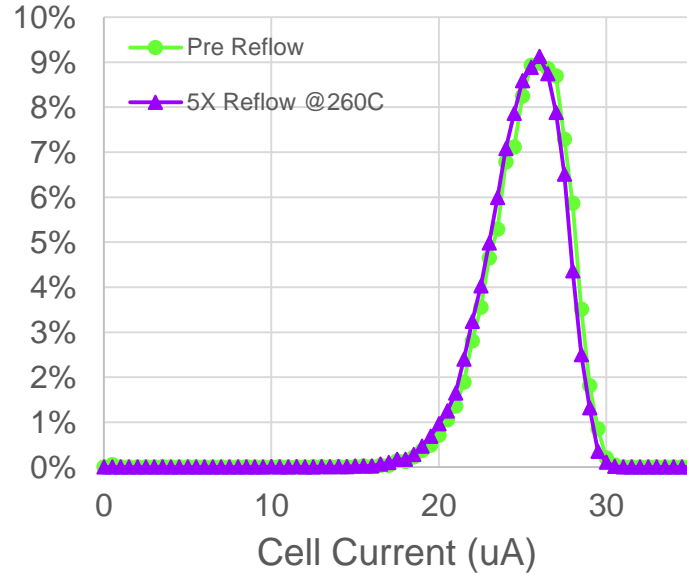


# ReRAM distribution is unchanged after 5X solder reflow retention test

Reflow Retention



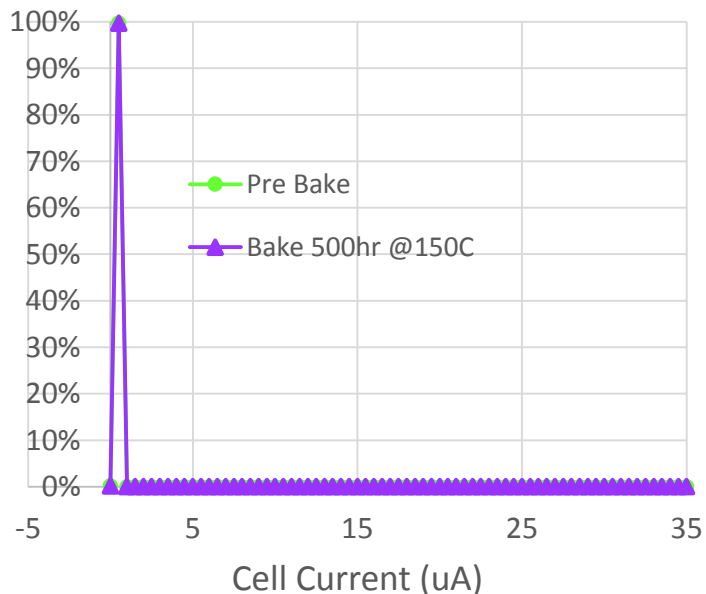
Reflow Retention



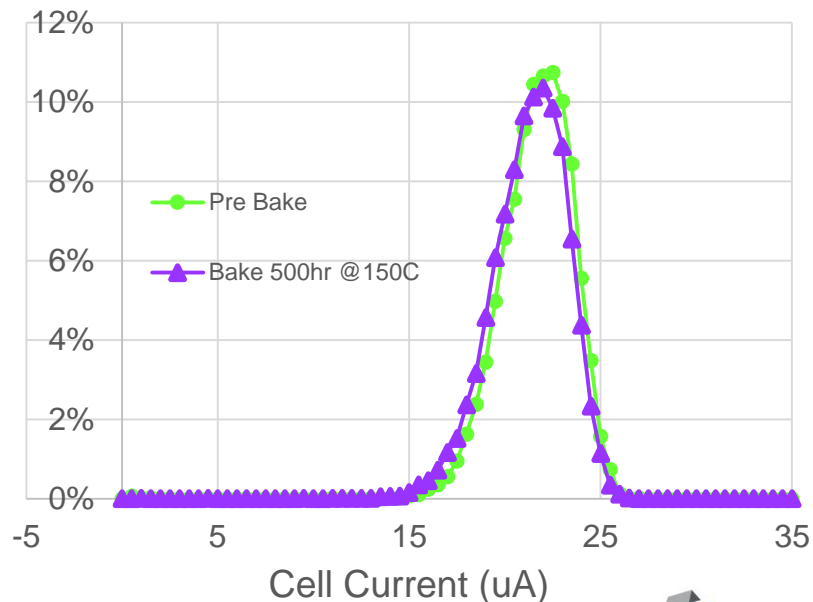


# ReRAM retention post 10K cycles is solid – No changes

32Kb Data Retention (Post 10K Cycle)



32Kb Data Retention (Post 10K Cycle)

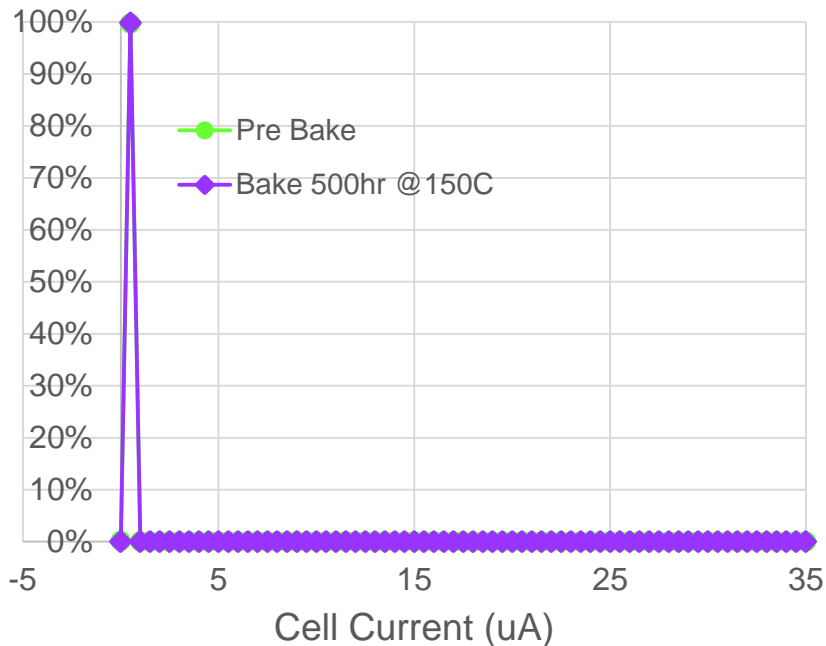




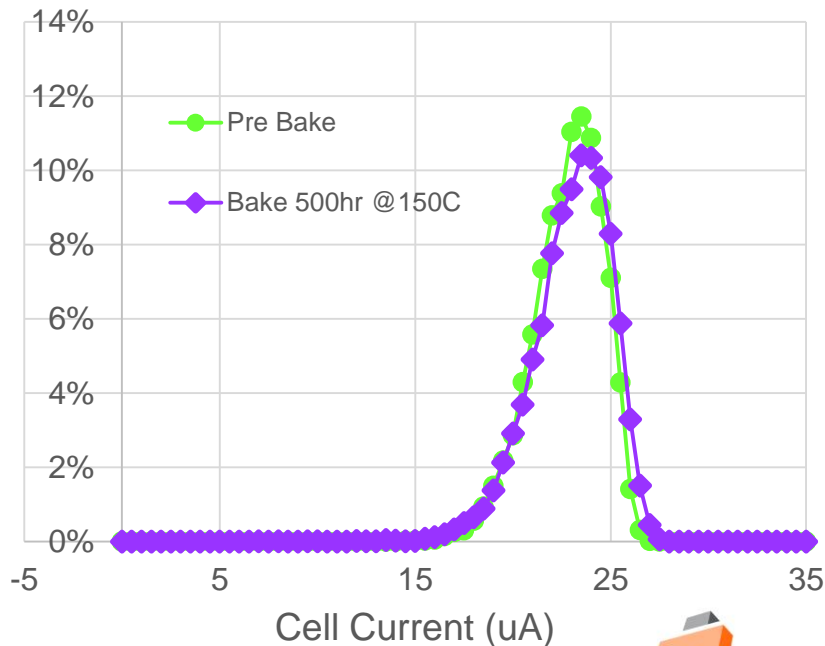


# ReRAM retention post 300K cycles is solid – No changes

32Kb Data Retention (Post 300K Cycle)



32Kb Data Retention (Post 300K Cycle)





# ReRAM is here and ready for the future

- ✓ Impressive reliability with robust retention post 10K & 300K endurance cycles
- ✓ ReRAM distributions remain stable post 5X Solder reflow
- ✓ Consistent ReRAM array performance across temperature (-40, 125C) and VCC range
- ✓ Starting production with SMIC for ReRAM customer designs
- ✓ 2X node ReRAM integration in progress
- ✓ Already started 1X node ReRAM design with customer