



Flash Memory Summit



Evaluation of error recovery flow of SSD media based on real NAND data simulation

Young Pil Kim, Antoine Khoueir, and
Erich F. Haratsch



Flash Memory Summit

Outline

- Motivation
- Simulation system
- LDPC performance investigation
- Recovery flow evaluation



Probabilistic behavior of LDPC

- Raw error count in a sector?

→ **Cannot tell Pass/Fail in LDPC**



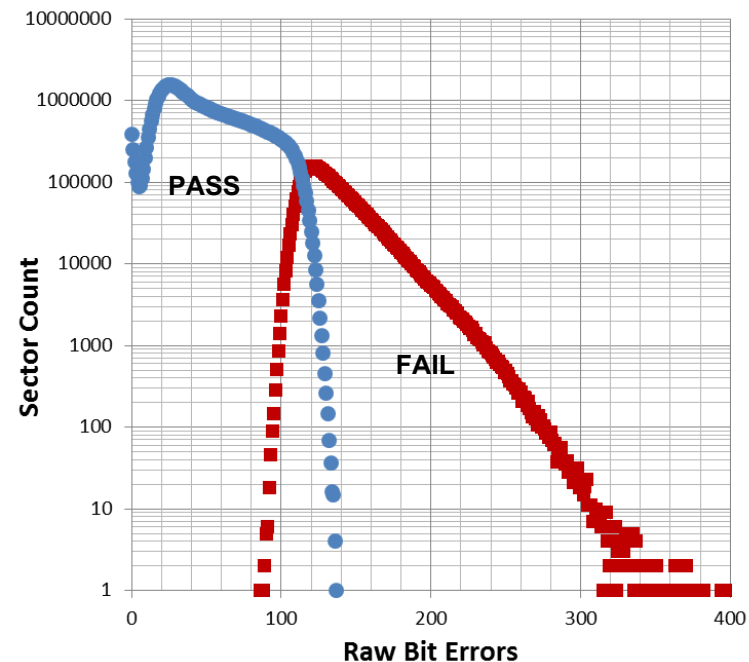
128 errors: Fail



136 errors: Pass

↪ Error bit location: both look similar

→ **Need LDPC simulation !**





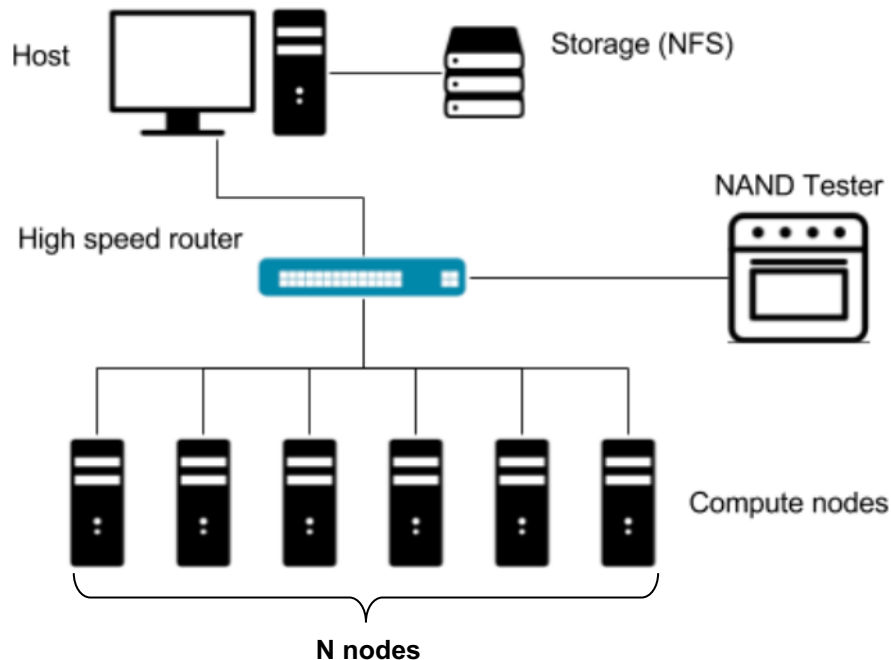
1 bit error per 1E17 bits

- Enterprise SSDs need to achieve UBER of 1E-17 or better
- More than 1E17 bits need to be simulated
- \Rightarrow Need to handle large amount of data



LDPC Simulation System

- Linux based Beowulf clusters
- Intel Xeon multicore + DDR4
- Multi-HDDs with RAID0 for fast access
- High speed Ethernet connection
- Python/C++ with Message Passing Interface (MPICH)



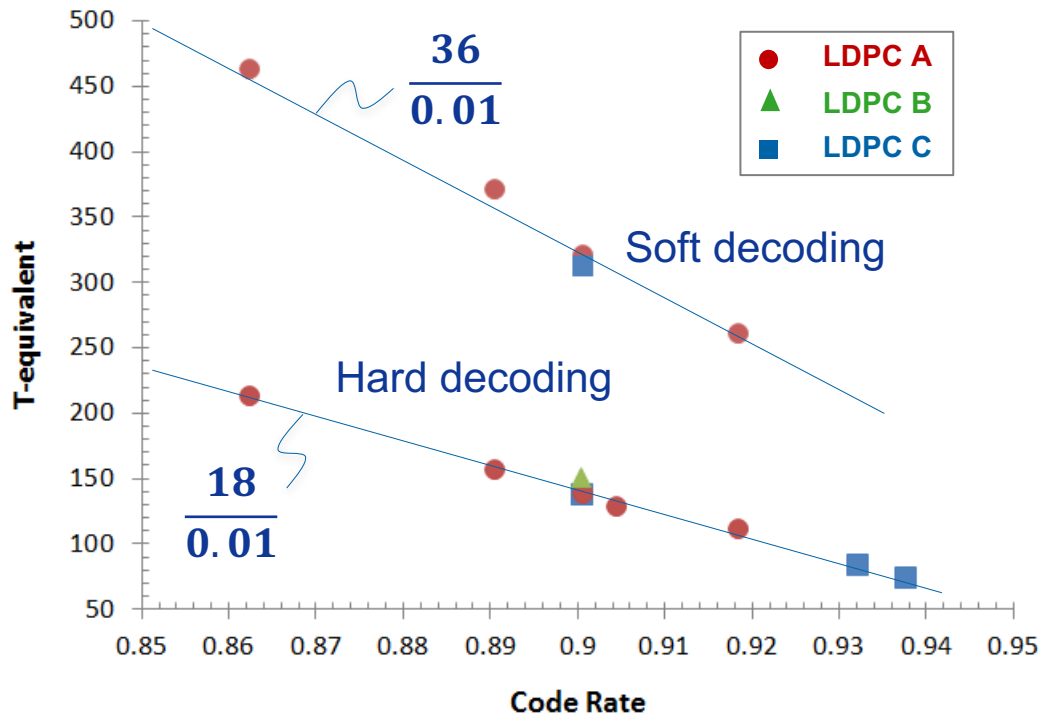


Selection of LDPC decoders

- Equivalent threshold (T_{EQ}): a threshold of an equivalent BCH decoder which gives the same code failure rate as the LDPC decoder under investigation for a given data set
- Statistically meaningful figure of LDPC decoding performance based on simulating decoding algorithms with NAND data
- LDPC decoder algorithms and architectures can be selected based on the T_{EQ} analysis



Correction capability of LDPC decoding

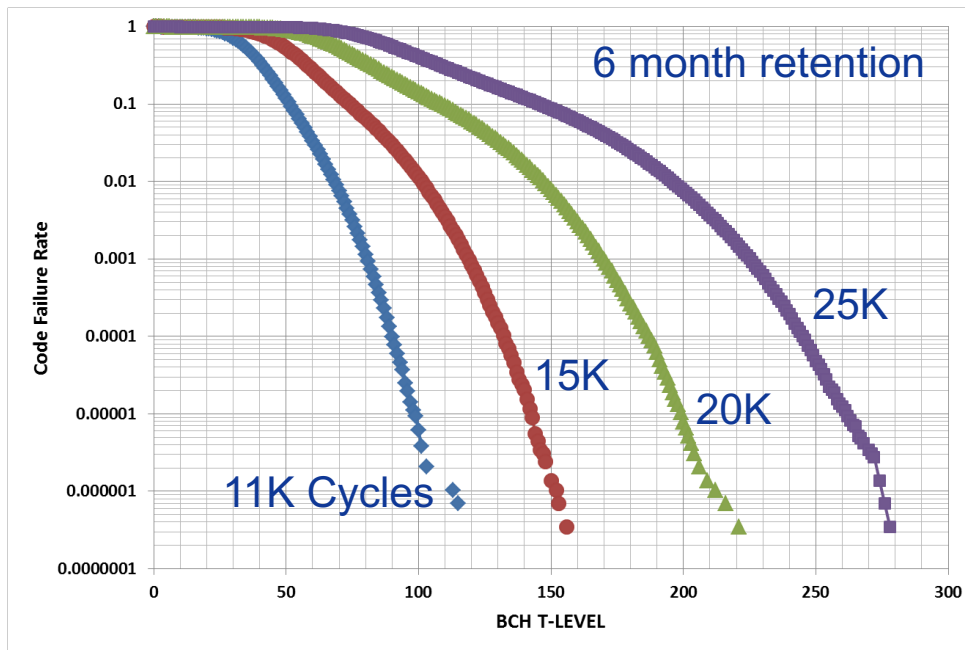


- ~18 bits of gain per 10% of code rate change for hard LDPC
- ~36 bits of gain per 10% of code rate change for soft LDPC



NAND flash samples

NAND type	cycle	retention
1y nm MLC	11k, 15K, 20K, 25K	6 months @40C



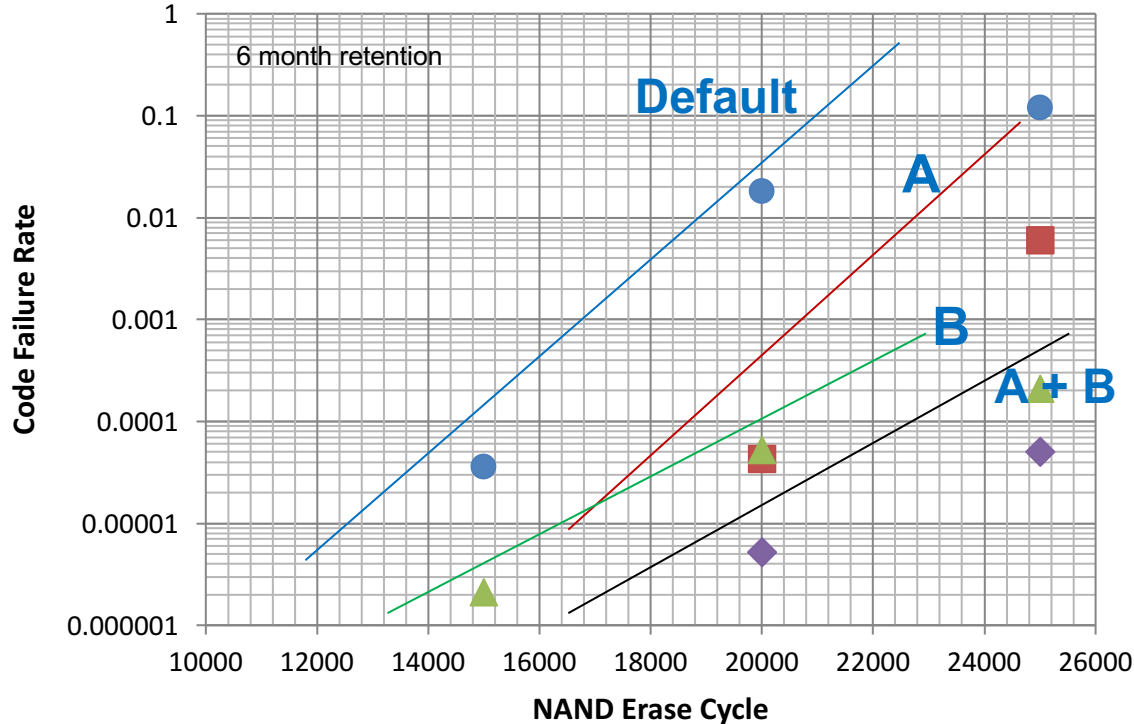


Two error recovery plans compared

- Plan A: Sequential read retry
 - Multiple decoding operations until decoding succeeds
- Plan B: Calibrated read
 - Single decoding operation after multiple read operations
- Combination of A and B also investigated
- Hard LDPC decoding is shown



CFR vs Cycle for the error recovery plans



- Trend curves tell maximum reachable cycle numbers for a given CFR requirement
- Significant improvement in CFR for the presented recovery plans
- More improvement possible with soft LDPC



Conclusion

- An LDPC simulation using high performance computing (HPC) cluster system with message passing interface (MPI) was introduced for the real NAND data based analysis
- A case study for SSD NAND media with two error recovery plans was discussed showing the maximum achievable number of program/erase cycles



Flash Memory Summit

Thank You! Questions?



Visit Seagate Booth #505

Learn about Seagate's portfolio of SSDs,
flash solutions and system level products for
every segment.