High-Throughput Low-Power Finite Alphabet Iterative Decoders

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High-throughput Design Challenges

- Migration to 3D TLC flash (and later QLC flash) → LDPC codes are becoming essential for endurance.
- LDPC decoders by nature are power-consuming compared to BCH.
- Throughput requirements are only increasing.
- Achieved at the cost of significantly higher area and power.

Previous Results

- Introduced Finite Alphabet Iterative Decoders (FAIDs)
- Address the error floor problem while providing savings in hardware resources.
- Hard-decoding and 2-bit soft decoding (1 hard bit and 1 soft bit)
- **Goal for this talk**: Propose FAID-based architectures suitable for very high throughputs with better scaling for area and power.

FAID: Decoding Approach

- Finite alphabet iterative decoding (FAID): messages belong to a finite alphabet represented as 0, ± 1, ± 2, etc.
- Check node update: same as a typical min-sum decoder (sign operation of messages along with minimum of magnitudes).
- The main differentiator is in the variable node update (VNU).
- VNU is a simple map designed to operate with 3-bit messages

FAID: Key Features

- VNU is a (d_v-1)-dimensional map (d_v is the column-weight) defined for each value received from the channel (set Y).
- Hard-decoding: Y={-1,+1}, 2-bit soft: Y={-2,-1,+1,+2}

Example VNU map for d_v = 3

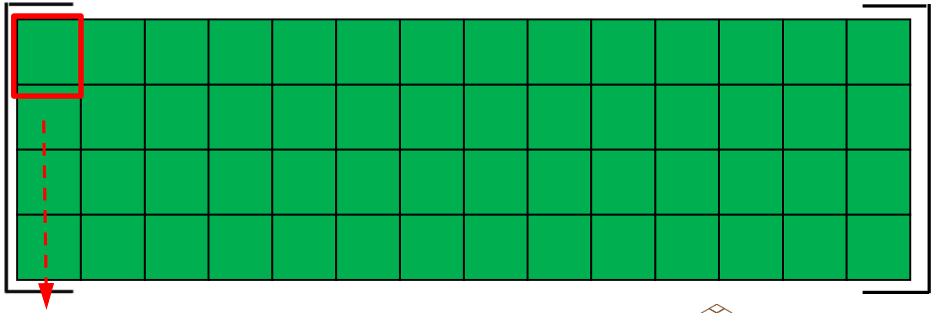
m_1/m_2	-3	-2	-1	0	1	2	3
-3	-3	-3	-3	-3	-3	-3	-1
-2	-3	-3	-3	-3	-2	-1	1
-1	-3	-3	-2	-2	-1	-1	1
0	-3	-3	-2	-1	0	0	1
1	-3	-2	-1	0	0	1	2
2	-3	-1	-1	0	1	1	3
3	-1	1	1	1	2	3	3

- Limited precision in the messages
- Optimized for both waterfall and error floor performance

Vertically Layered Architecture

- Quasi-cyclic LDPC codes – parity-check matrix defined by blocks of circulants (denoted by ■)

- Vertically Layered architecture: sequential updating of messages across columns

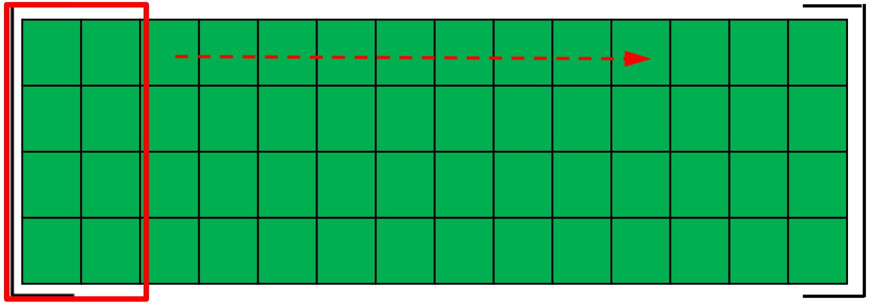


- Previous architecture - Single circulant per clock cycle processing

- Flexibility in rate and length

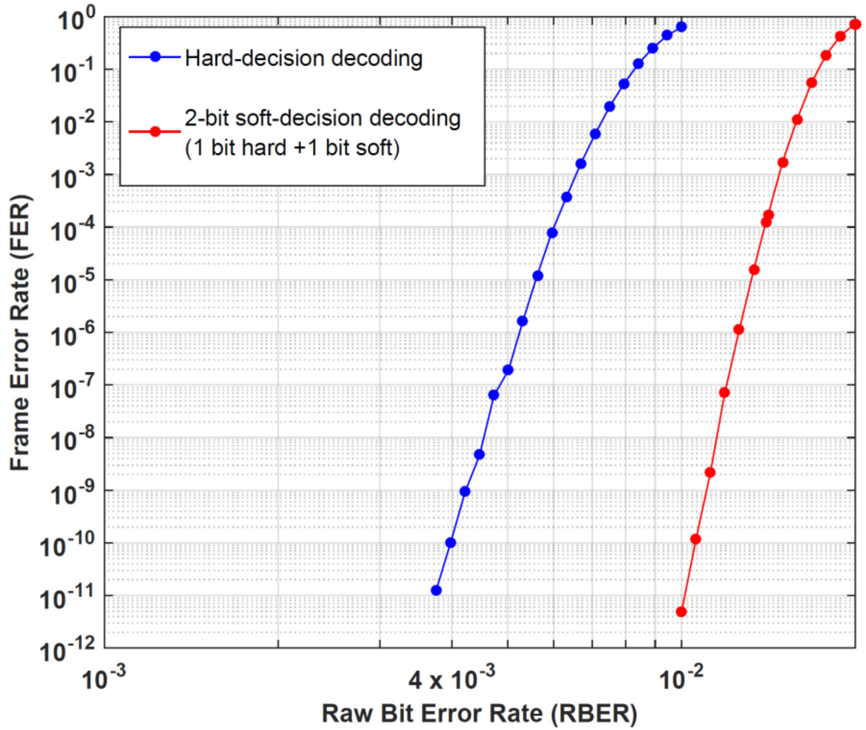
High-throughput Architecture

- Multi-column processing – Processing multiple columns per clock cycle
- More favorable throughput scaling with area and power



- Account for reduced layering
- Memory used at variable nodes is small
- Flexibility in rate and length

FER vs RBER: 1KB, R=0.883



- No occurrence of error floor at FER of 1e-11.
- Multi-column processing has identical FER performance as single circulant processing.

Results generated using multiple Xilinx Virtex-7 FPGA boards

ASIC Design results

- 28nm (using only HVT memory and SVT standard cell)
- 60% utilization with no routing congestion issues

Single circulant processing	
Total Cell Size	0.46 mm^2
Total Die Size	0.72 mm^2

High-throughput Multi-column processing	
Total Cell Size	1.73 mm^2
Total Die Size	2.9 mm^2

Increase in area by about 4 times

ASIC Design results

- 28nm (HVT memory and SVT standard cell)
- Timing closed at slow and fast corner
- Clock frequency of 556 MHz (at constant power of 1.55W).

Average Throughput at RBER=1e-2 (4.9 iterations)	4.1 GB/s
Average Throughput at RBER=5e-3	5.95 GB/s
Average Throughput at RBER=1e-3	8.33 GB/s

ASIC Design results

- Power vs RBER measured at constant throughput of 4.1GB/s at clock frequency of 556MHz (28nm)
- Power measured at typical operating conditions
- Power measurement includes SAIF-based analysis with toggle rates generated at the corresponding RBER

Average Power at RBER=1e-2	1.55 W
Average Power at RBER=5e-3	1.06 W
Average Power at RBER=1e-3	760 mW

Throughput Scaling vs Area/Power

- 7.5x increase in throughput for only 4x increase in area and 5x increase in power
- Scaling improves with higher rates (additional 10-20% savings in power and area)
- Scaling holds for larger codeword lengths depending on the structure of the parity-check matrix.

Conclusions

- Multi-column processing vertically-layered FAID can enable very high throughputs.
- The nature of FAID allows low-error-floor error-rate performance with limited precision in the soft-decoding.
- Can provide significant savings in area and power to achieve those throughputs.