UFS 3.0 - Controller Design Considerations

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Before I Start….

1. What’s the benefit of adopting UFS?
2. What’s the UFS application/market?

What’s the UFS3.0 requirements that controller company need to consider?

Mobile Storage Evolution

eMMC
- Latest widely adopted standard before UFS 2.x
- Limited to 400MB/s (duplex) since 2013

UFS 1.x
- Not adopted

UFS 2.x
- Offers desktop-grade performance of ~1200MB/s over full-duplex links
- Good adoption in flagship devices (2017)

UFS 3.0
- Doubles UFS 2.x performance, offering ~2400MB/s
- **Requirements are tough for mobile form factors**

UFS 3.0 Controller Requirements

1. **High Throughput**
2. **Low Active Power**
3. **Low Latencies**
4. **Cost Management**
   a) Reduced DIE Size
   b) Support to latest 3D NAND technologies

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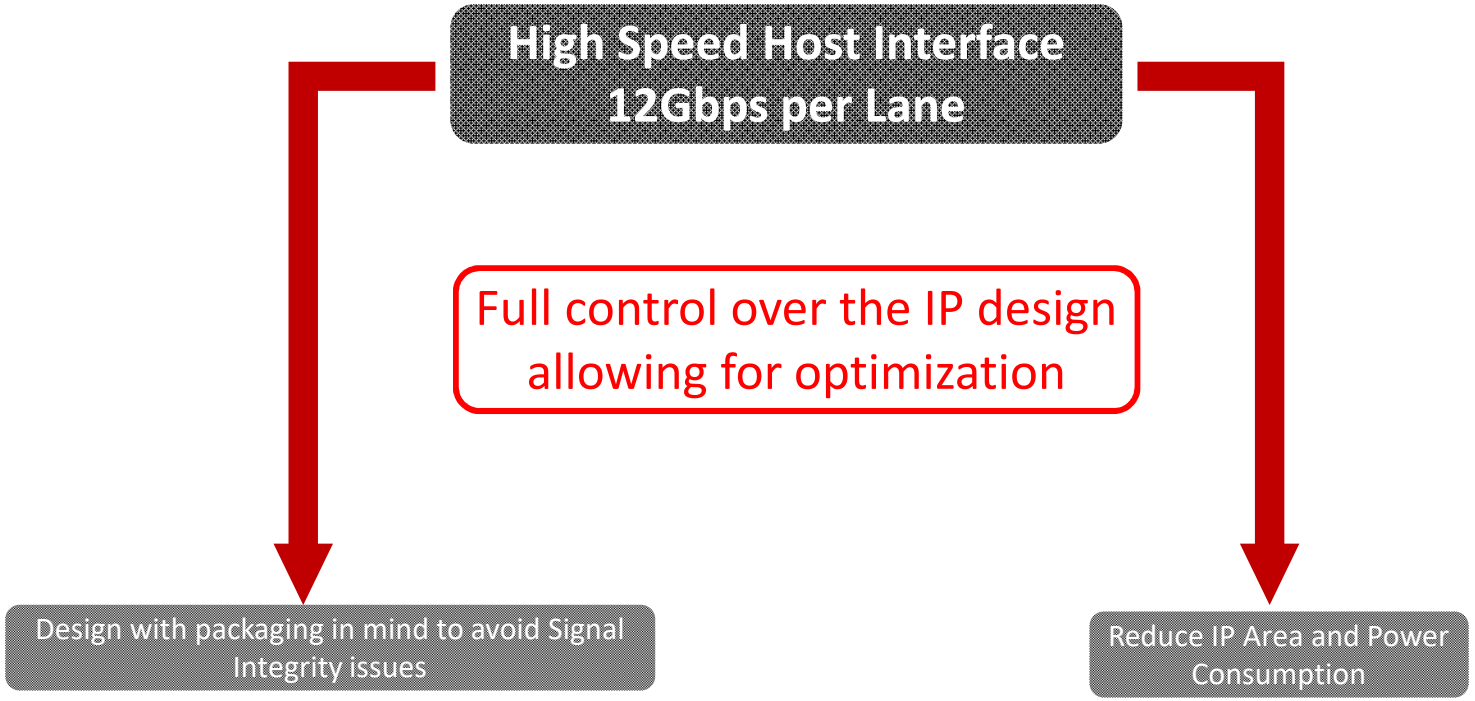
UFS 3.0 Controller Challenges



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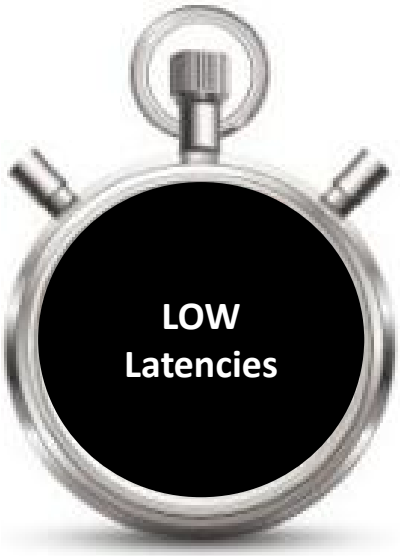
UFS 3.0 Controller Challenges

High Speed
Flash Interface

High Speed
Error Correction Engine



Hardware Acceleration to
reduce FW & CPU Overhead

QoS (Quality of Service)

Having in-house IPs can shape the design around these requirements

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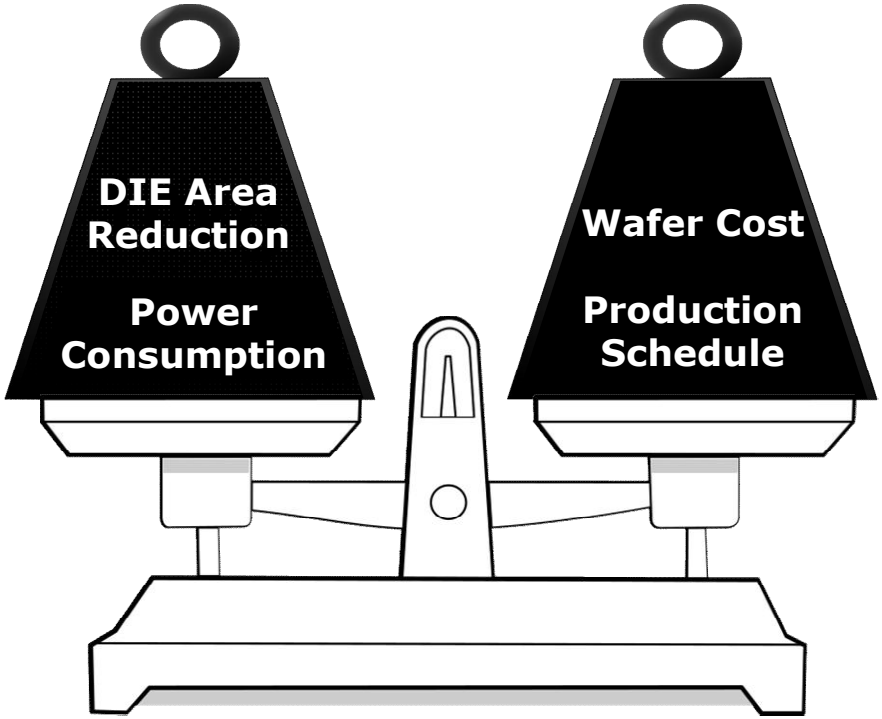
Newer Process: All About the Right Balance



Choosing the Ideal Process

EXAMPLE – Phison's Error Correction Engine IP Study			
	Phison Gen1	**Phison Gen2**	**Next Gen**
Application	**UFS 2.1 - HS G3 x1-L**	**UFS 2.1 - HS G3 x2-L**	**UFS3.0 - HS G4 x2-L**
ECC Throughput (Higher than I/F)	800MB/s (800 x1)	1333MB/s (800 x1.66)	2666MB/s (800 x3.33)
Area (aprox.)	x1	x0.32	**x0.44**
Power Consumption	x1	x0.46	**x0.67**
DIE Area Cost	x1	x0.53	**x0.75**

A newer process will bring more advantages. However mask investment, wafer cost, production schedule, IP availability (if not in-house) will have to be considered

Summary

- In device controller design, the balance between performance, power and cost is critical. A total control of the design will offer more flexibility to optimize the solution

In-house IPs can optimize the cost and requirements

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Performance	PS8313* 3D TLC	PS8313* 3D TLC
Host Interface Mode	HS-Gear 3B **x1 Lane** **(eUFS / UFS Card)**	HS-Gear 3B **x2 Lanes** **(eUFS only)**
NAND Flash Configuration	2ch, 4CE @667MT/s	2ch, 4CE @667MT/s
Seq Read	530 MB/s	920 MB/s
Seq Write	400 MB/s	550 MB/s
Random Read	67,000 IOPS	67,000 IOPS
Random Write	60,000 IOPS	62,000 IOPS

*Test with Phison Tester (No host/OS overhead)

Thank you