

Embedded 28-nm Charge-Trap NVM Technology

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- Embedded NVM applications
- Charge-trap NVM at Cypress
- Scaling
- Key Flash macro specs
- 28-nm Flash memory reliability
- Conclusions

Embedded NVM Applications

- Focus on NVM monolithically integrated in a System-on-Chip (SoC)

Consumer

- Cost
- Endurance
- Ambient -25C to 85C
- 50-ns access
- 100k endurance



Industrial

- Low power
- Cost
- Ambient -40C to 105C
- 25-ns access
- 10k endurance



Automotive

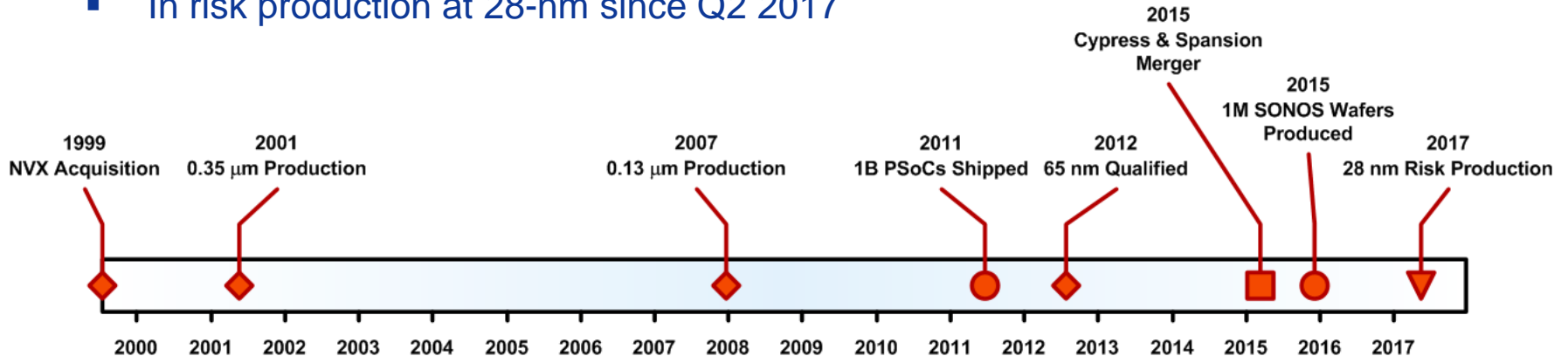
- Performance
- Reliability
- Ambient -40C to 125C
- Code: 20-ns access
- Code: 1k endurance
- Data: 100k endurance



- IoT device shipments will grow from 0.6 billion units in 2017 to 2.3 billion units in 2023¹
 - eNVM is a key enabler of embedded processing and connectivity
 - eNVM costs are holding up adoption (process and test)
 - Low power read and write operations – active power
 - Secure program/data storage
 - No compromise on reliability; fast access time

Charge-Trap NVM: Cypress History

- Acquired NVX and its Silicon Oxide Nitride Oxide Silicon (SONOS) IP in 1999
- Put SONOS into production at 0.35- μm node in 2001 and 0.13- μm node in 2007
- Shipped >2 billion PSoC units with SONOS eFlash
- Produced >1 million wafers with foundry partners HH-Grace, UMC, and HLMC
- In risk production at 28-nm since Q2 2017



Embedded Charge-Trap NVMs



Feature

Node

Cell Architecture

Memory Device

Program/Erase Method

Ambient Operating Temperature

Speed/Random Access Time

Write Endurance

Data Retention

Extra Masks beyond Std CMOS

Applications

eCT

40-nm

1.5T, 1 bit/cell

ONO

HEI/HHI

-40C to 125C

8 ns

125k cycles

20 years

8

Embedded NOR Flash for automotive MCUs

SONOS

40, 28-nm

2T, 1 bit/cell

ONO

FN/FN

-40C to 105C

25 ns

100k cycles

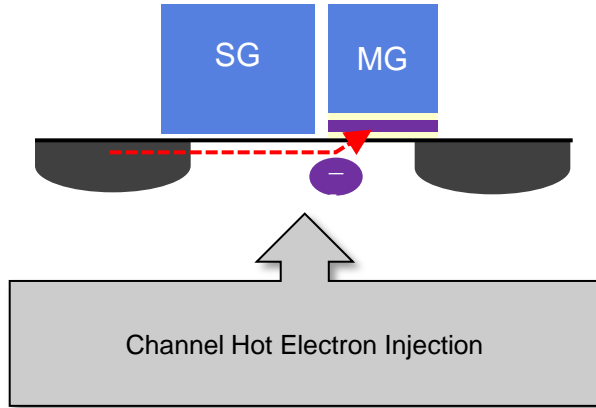
10 years

5

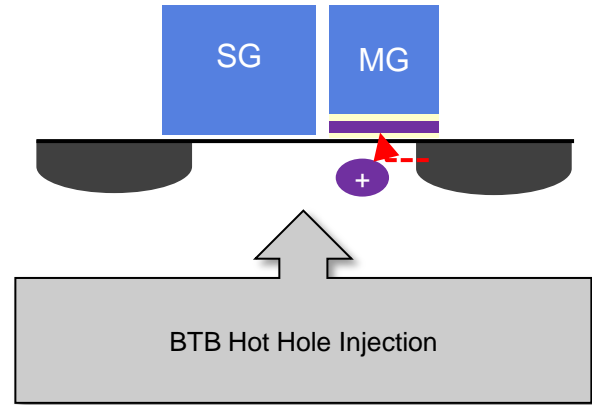
Embedded NOR Flash for consumer and industrial MCUs

eCT Program & Erase Operations

Program



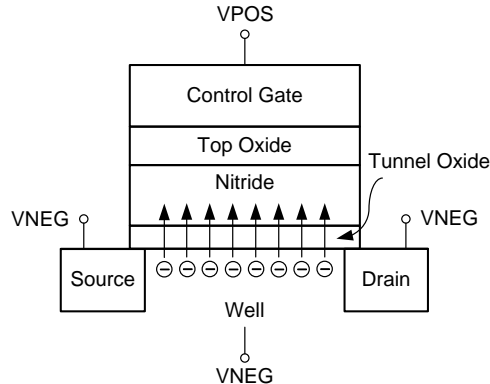
Erase



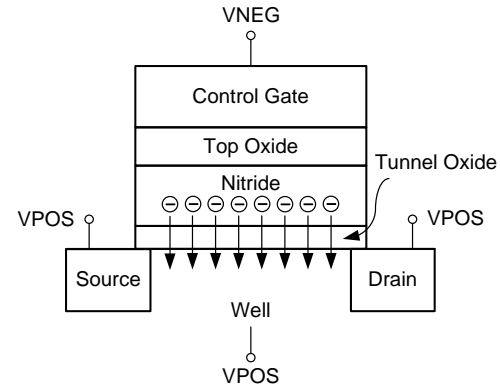
SONOS Program & Erase Operations

- Silicon Oxide Nitride Oxide Silicon (SONOS)
 - A SONOS transistor is a planar, scalable MOS transistor with an ONO stack as the gate dielectric
 - The basis of the NVM function is storage of captured charges in discrete traps in the nitride (N) layer
 - Program and erase operations use uniform channel FN tunneling
 - Requires only five extra masks beyond the standard CMOS process

Program

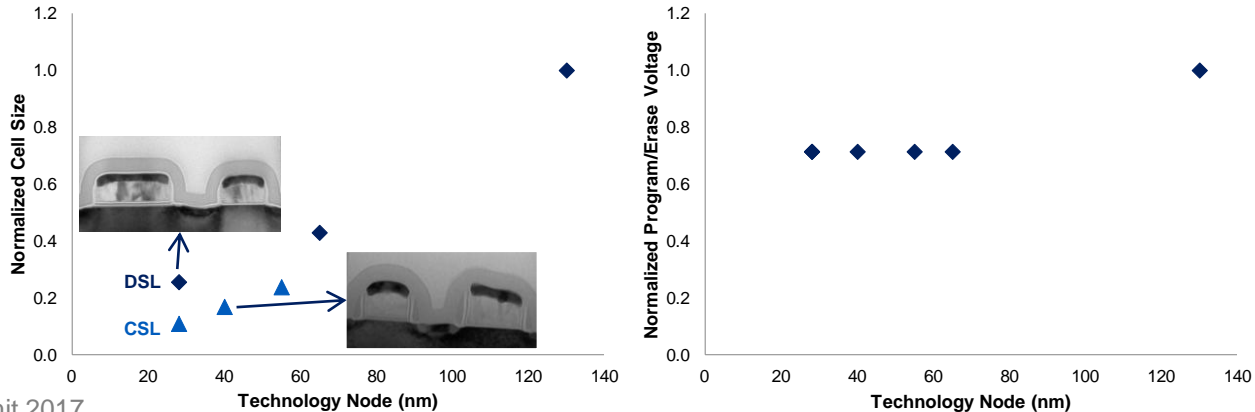


Erase



SONOS Scaling

- Cell area scales down
 - Program/erase voltages are held constant since 65-nm
 - Transition from dedicated (DSL) to common (CSL) source line array enables significant reduction in cell area at the same node
- Trade-off exists between the access time and cell area

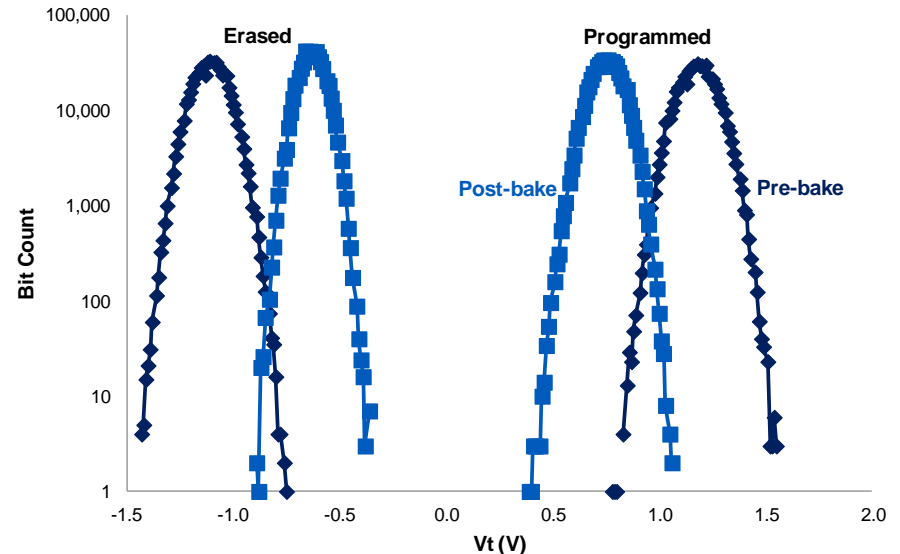
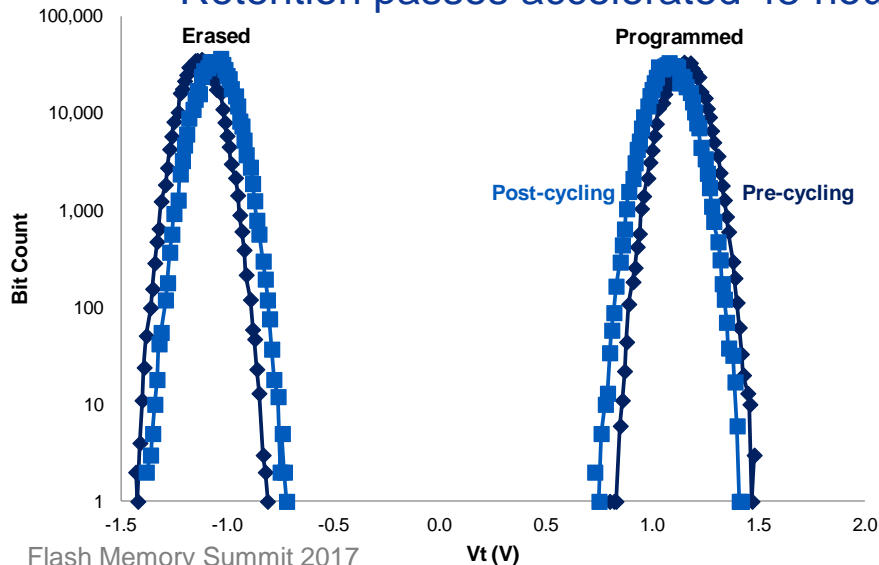


Key Flash Macro Specs

	<u>28-nm SONOS</u>	<u>40-nm SONOS</u>
Density	1Mb	1Mb-16Mb
Input data width	32-bit	32-bit
Output data width	64-bit	32-, 64- or 128-bit
Dual Power Supply	0.89 V-1.10V & 2.25 V-2.75 V	0.81 V-1.21 V & 1.62 V-3.63 V
Operating Temperature	-55C to 125C	-40C to 125C
Read access time	25 ns (1.05±0.05 V)	25 ns (1.10±0.11 V)
Read Current	75 μ A/MHz per 64-bit	61 μ A/MHz per 32-bit
Write Endurance	> 10k cycles	> 100k cycles
Data Retention	> 10 years at 110C	> 10 years at 100C

28-nm Flash Memory Reliability

- Write endurance easily passes 10,000 program/erase cycles at 125C
 - Vt window >1.4 V after cycling with single-pulse program/erase of constant amplitude and duration
- Retention passes accelerated 48-hour bake at 250C with > 0.7 V window left



Conclusions

- Charge-trap Flash technology has several advantages
 - Low cost: only five extra masks beyond the standard CMOS process
 - Low power: 0.9 V power supply, low-current FN/FN program/erase
 - Performance: 25-ns read access time in the standard power supply range
 - Resistant to de-processing; security features
- Cell is scalable even at constant program/erase voltages
- Cell and macro can be tuned to application
 - Consumer, e.g., smart cards: cost (CSL cell), 50 ns read, < 4 ms write time
 - Industrial: 25-ns read access with design techniques (smaller sectors, etc.)
 - Automotive: 8-ns eCT or robust DSL cell

Acknowledgments

- Cypress technology R&D team in San Jose, CA and Taiwan
- Cypress embedded NVM design team in Colorado Springs, CO and San Jose, CA