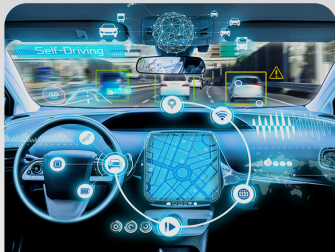# Solving functional safety challenges in Automotive with NOR Flash Memory

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Automotive Megatrends

Totally Connected Car	Levels 1 – 5	Intuitive & Responsive	Electrified Transportation
Connectivity	*Autonomous*	*HMI*	*Electrification*

Autonomous Driving – Evolution

Key Benefits
- **Higher Safety Levels**
- **Reduced Emissions**
- **Increased productivity**
- **Improved Mobility**

No Driver Needed (TBD)

2025 Urban Traffic Management

2021 Highway Traffic Management

2019 Traffic Jam Management

2018 Safe Distance & Lane Assist

2017 Driver Assist

2010 Emergency Brake Assist

2006 Parking Assistance

FULLY AUTONOMOUS

HIGHLY AUTONOMOUS

SEMI-AUTONOMOUS

CYPRESS
EMBEDDED IN TOMORROW

Challenges Facing Next-Gen Automotive Systems

Need safe, secure, and reliable external NOR Flash memories for code and data storage
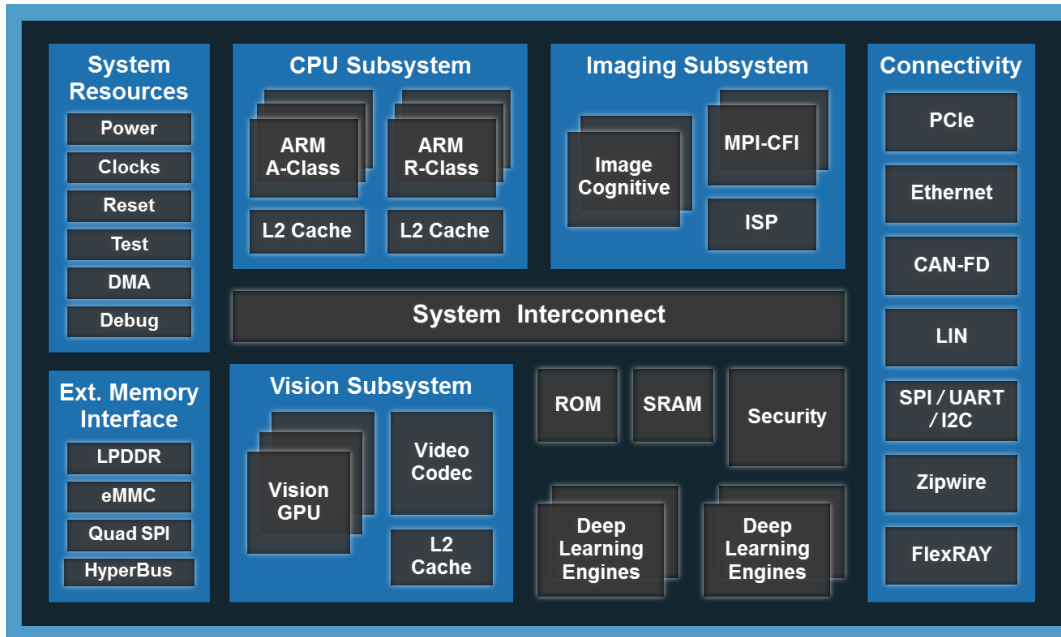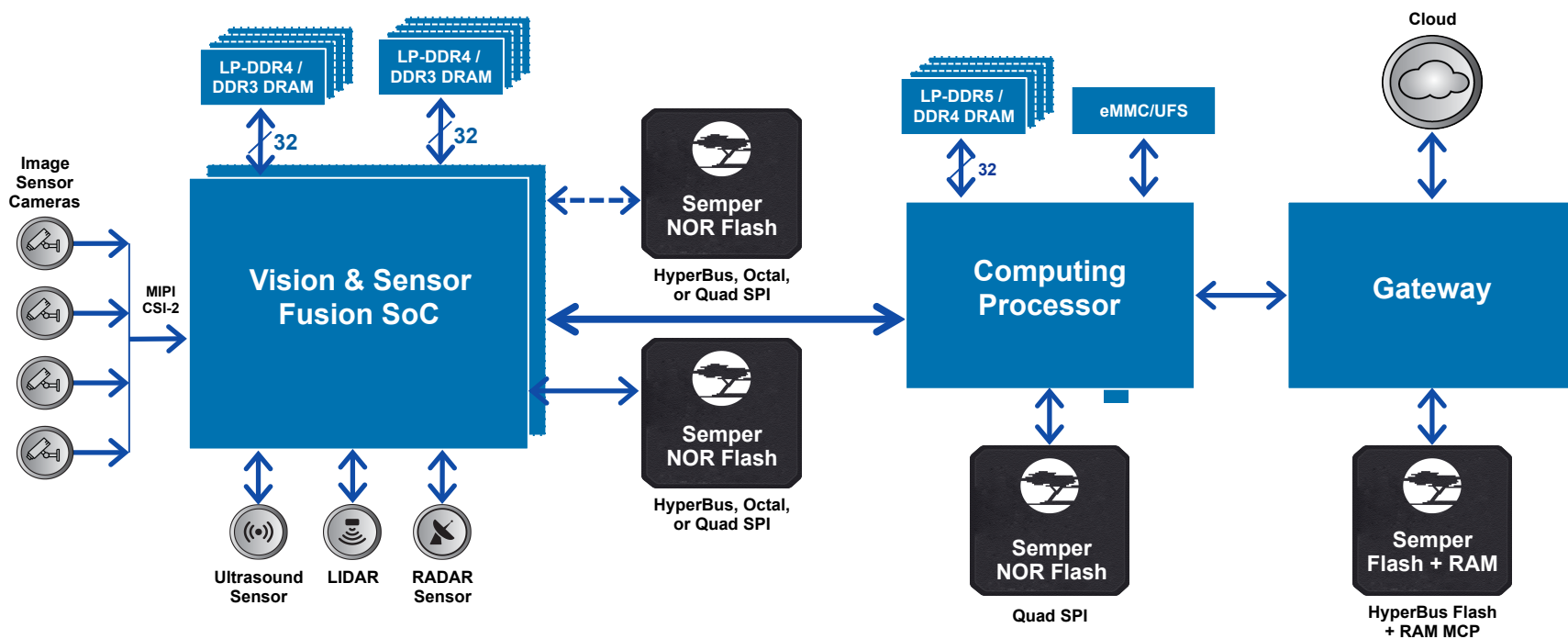

!(Embedded Flash)

- Heterogenous Architectures
- Real-Time Sensor Processing
- Safety and Reliability
- Security
- Software Complexity
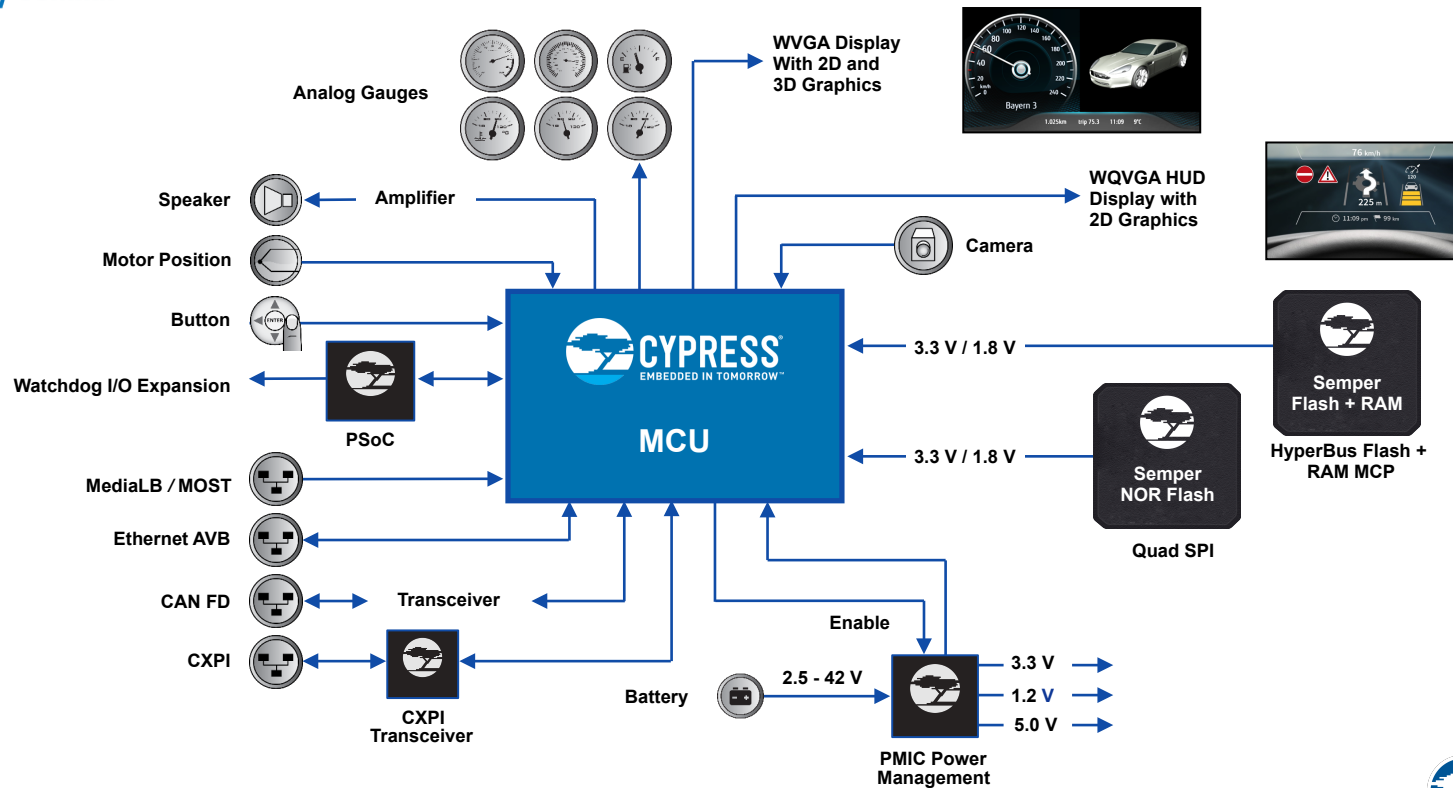- High-Speed Connectivity

ADAS System Solution

Instrument Cluster System Solution

Analog Gauges

WVGA Display With 2D and 3D Graphics

WQVGA HUD Display with 2D Graphics

Speaker

Amplifier

Motor Position

Button

Camera

Watchdog I/O Expansion

PSoC

MediaLB / MOST

Ethernet AVB

CAN FD

Transceiver

CXPI

CXPI Transceiver

Battery

2.5 - 42 V

Enable

PMIC Power Management

3.3 V

1.2 V

5.0 V

MCU

3.3 V / 1.8 V

3.3 V / 1.8 V

Semper NOR Flash

Quad SPI

Semper Flash + RAM

HyperBus Flash + RAM MCP

How Safety is Implemented in Automotive Today
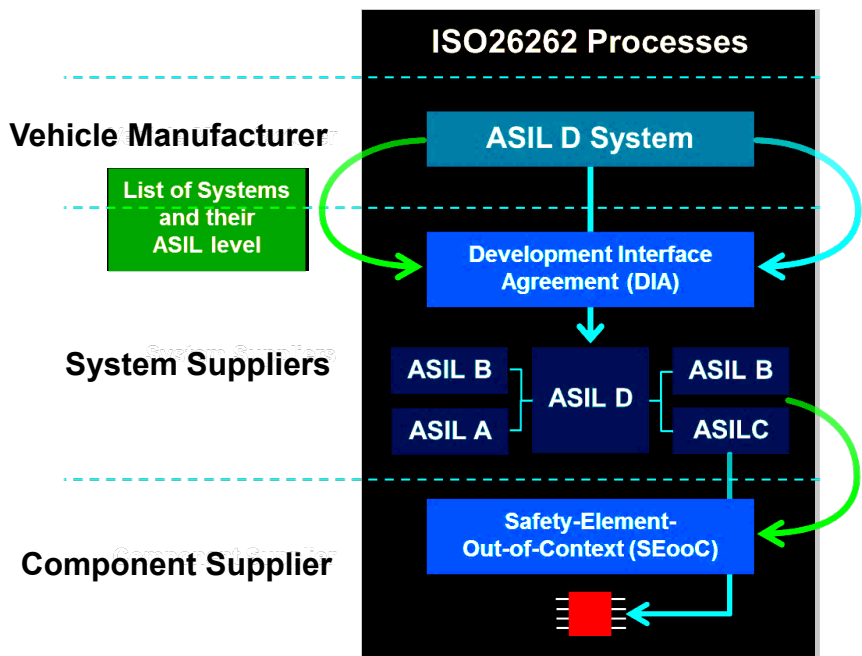
Detection and Management

- Random and Systematic Faults
- Single-Point Faults – 99% for ASIL-D System
- Latent Faults – 90% for ASIL-D System
- Probabilistic Metric Hardware Faults – 10-9h-1
- Fault-Tolerant Time Interval – 10ms

Safety Documentation

- Safety manual
- Failure Mode Effects and Diagnostic Analysis (FMEDA)
- Dependent Failure Analysis (DFA)
- Safety Element Out of Context (SEooC)
- Hardware Safety Requirements (HWSRs)

Functional Safety in NOR Flash
Diagnostics Provide the System with Critical NOR Flash Device Status

Category	Function	Provides
Data Integrity	ECC (SECDED)	Error detection and correction over memory array
	Data Integrity Check	Error detection over memory array
	Interface CRC	Error detection over memory interface
	Sector Protection	Prevents inadvertent writes to the device
Embedded Operation Error Reporting	SafeBoot	Reporting of proper flash device initialization
	Program Operation	Reporting of program failure
	Erase Operation	Reporting of erase failure
	Erase Status	Reporting of erase failure for sector selected by Evaluate Erase Status instruction
	Memory CRC	Reporting abort of CRC calculation
Operational Recovery	Configuration Data Corruption (Brown-out during Register Write)	Rebooting in SPI mode allowing host to program configuration registers
	Safe Reset	Graceful hardware system recovery using existing SPI signals
	Sector Erase Power Loss Detection	Erase power loss indicator status flag for each sector

Next-Generation System Requirements for Memory

Functional safety from product definition through production in accordance with ISO 26262 and IEC 61508

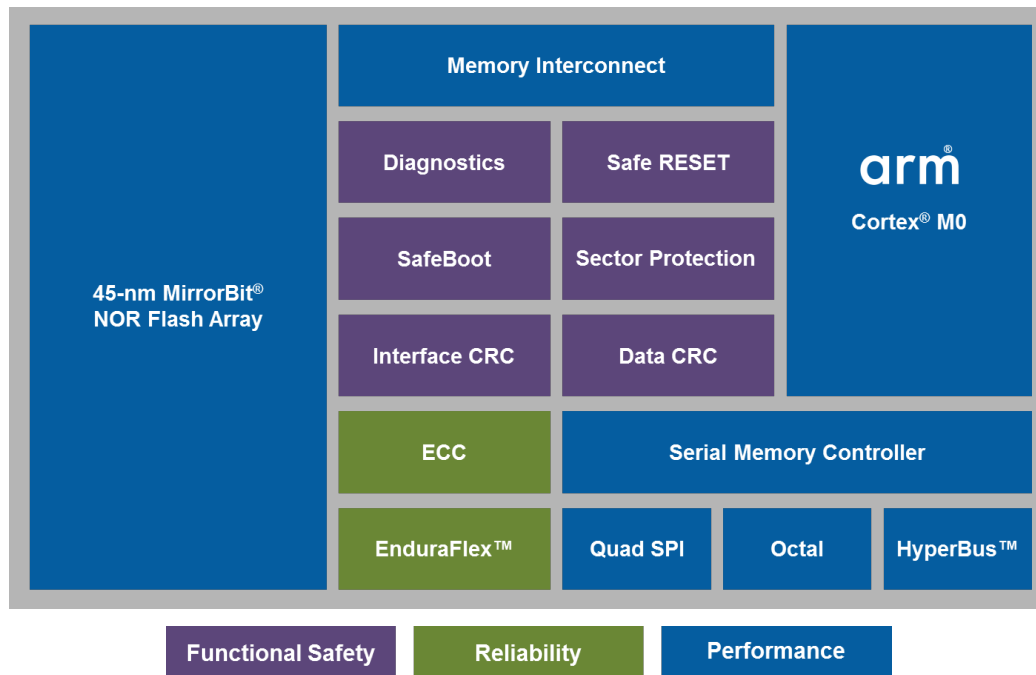Highest reliability and integrity of critical data, and early detection of possible failures

Scalable, high-density, high-performance interfaces that provide code and data storage and instant-on functionality

Zero-defect quality management processes and established longevity of supply

Semper NOR Flash Family Architecture

45-nm MirrorBit® NOR Flash Array	Memory Interconnect		arm® Cortex® M0
	Diagnostics	Safe RESET	
	SafeBoot	Sector Protection	
	Interface CRC	Data CRC	
	ECC	Serial Memory Controller	
	EnduraFlex™	Quad SPI / Octal / HyperBus™	

Legend: Functional Safety · Reliability · Performance

FEATURES

Functional Safety
- Architected and designed to automotive safety standards
- ASIL-B-compliant and ASIL-D ready

Best Reliability and Endurance
- EnduraFlex™ architecture enables >1M endurance cycles and 25 years data retention
- Grade-1 (125C) automotive qualified

Highest Density
- MirrorBit® technology delivers up to 4Gb with 400MB/s JEDEC xSPI

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