



Flash Memory Summit



New Technologies and New Standards Enable New Mobile Applications

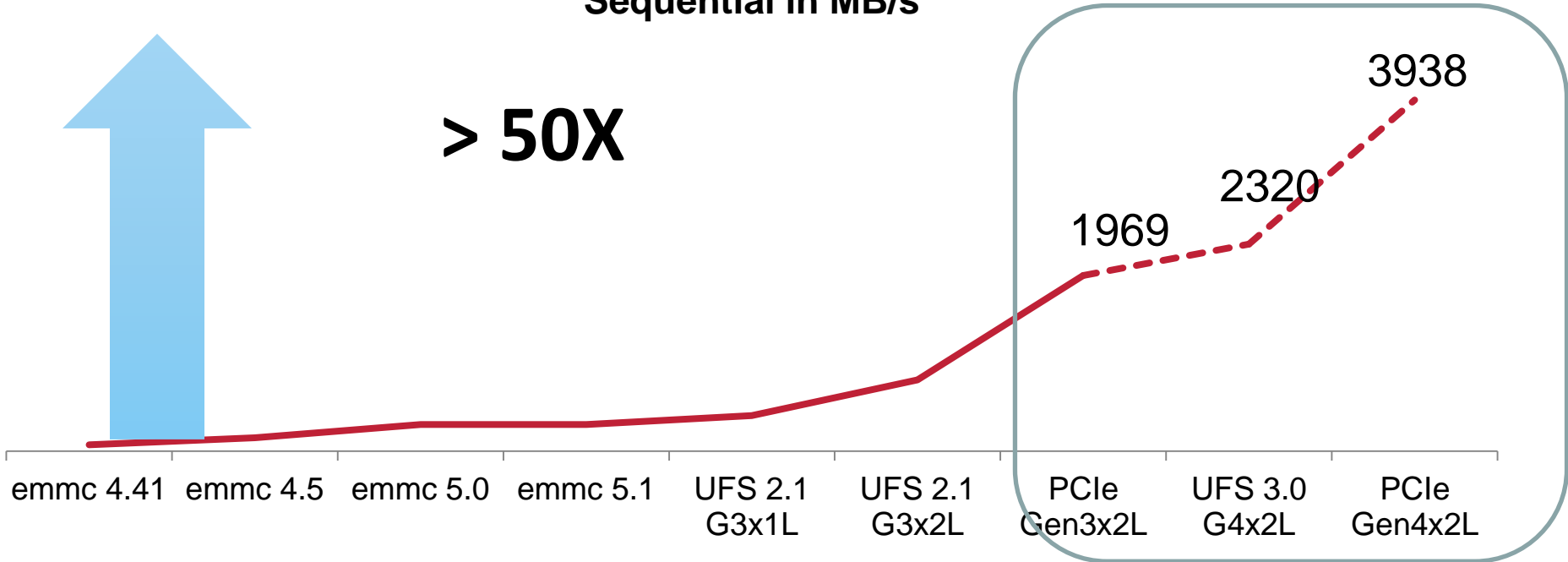
Robert Hsieh
Silicon Motion, Inc.



Mobile Storage Performance

Sequential in MB/s

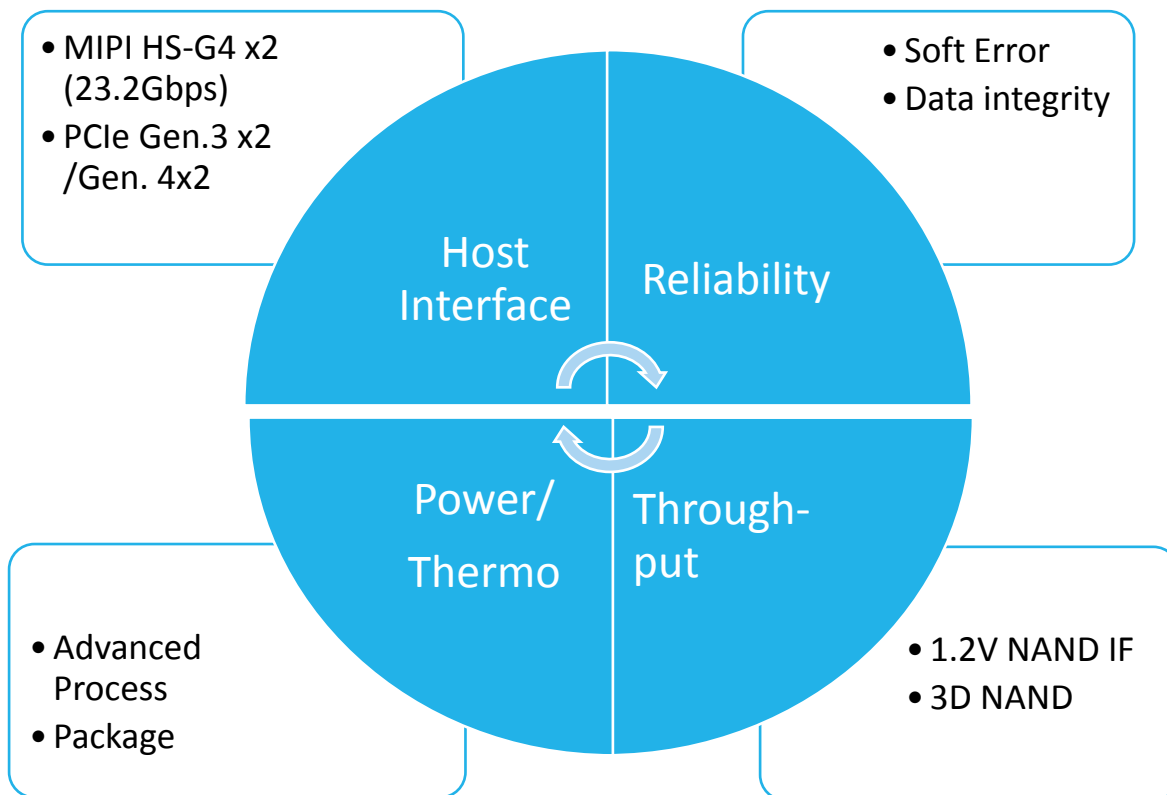
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Next Generation Mobile Storage Controller

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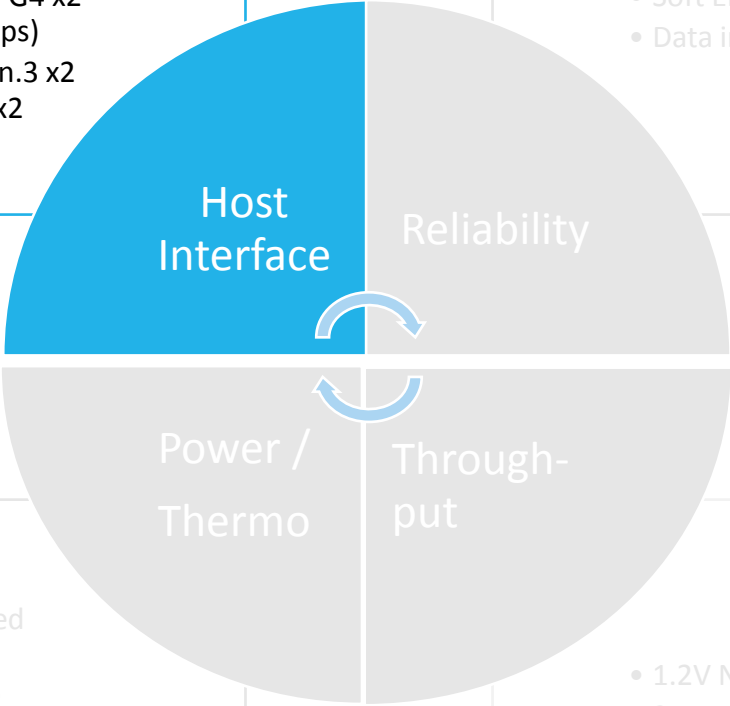


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- Host Memory Acceleration
- High Efficient

- MIPI HS-G4 x2 (23.2Gbps)
- PCIe Gen.3 x2 /Gen. 4x2



- Soft Error
- Data integrity

- Advanced Process
- Package

- 1.2V NAND IF
- 3D NAND



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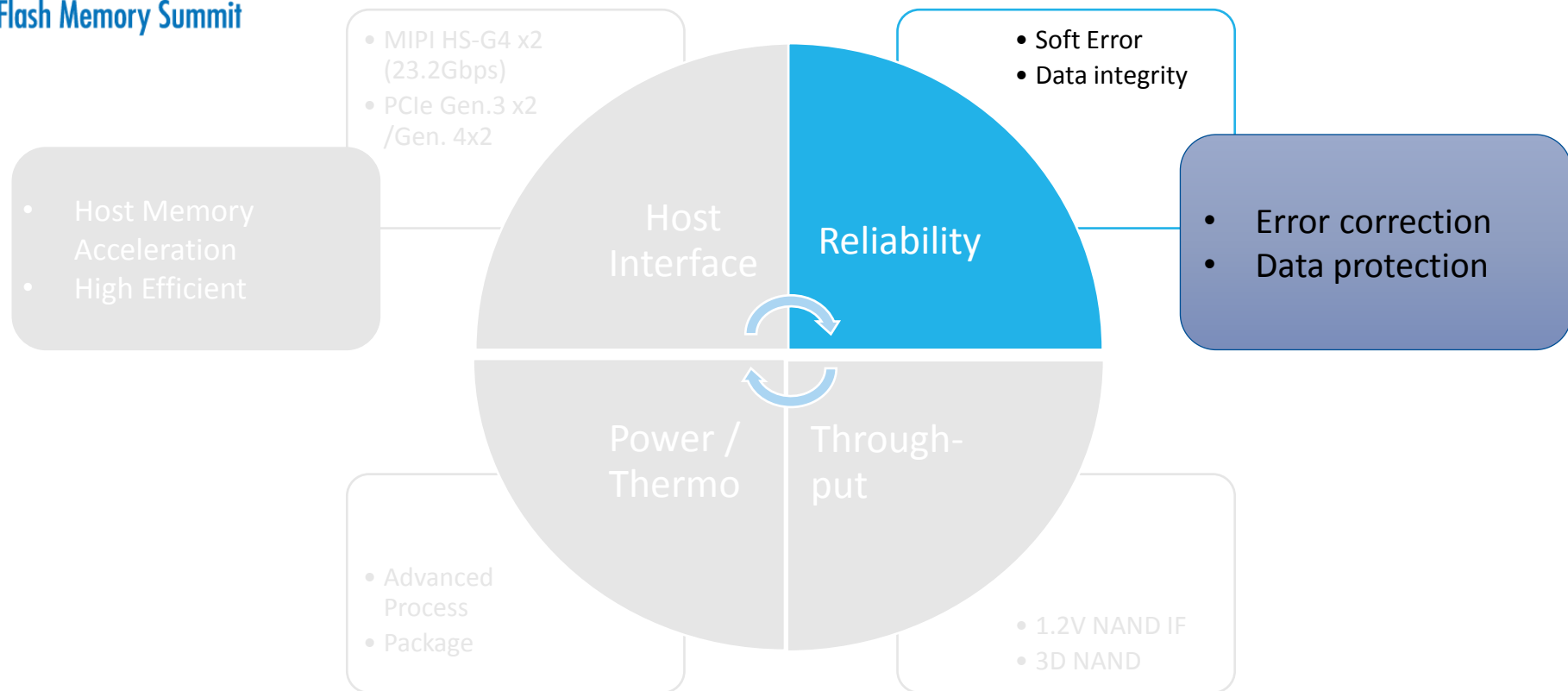
Host Interface

- **Utilize Host Memory to reduce the table update**
- **Advanced Line coding (128b/130b)**



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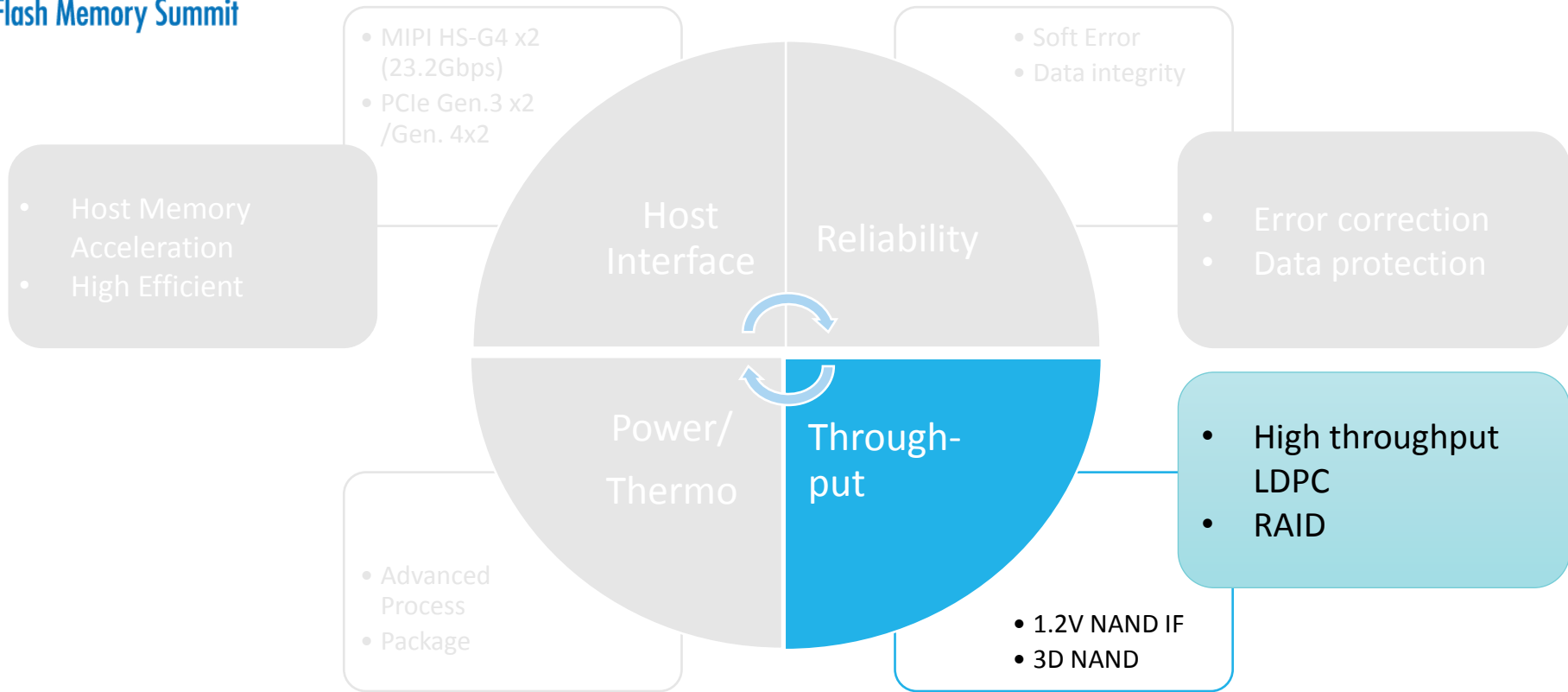
Reliability

- **More Soft bit error due to large SRAM density**
- **Error correction to prevent potential stuck**
- **Data protection/encryption**



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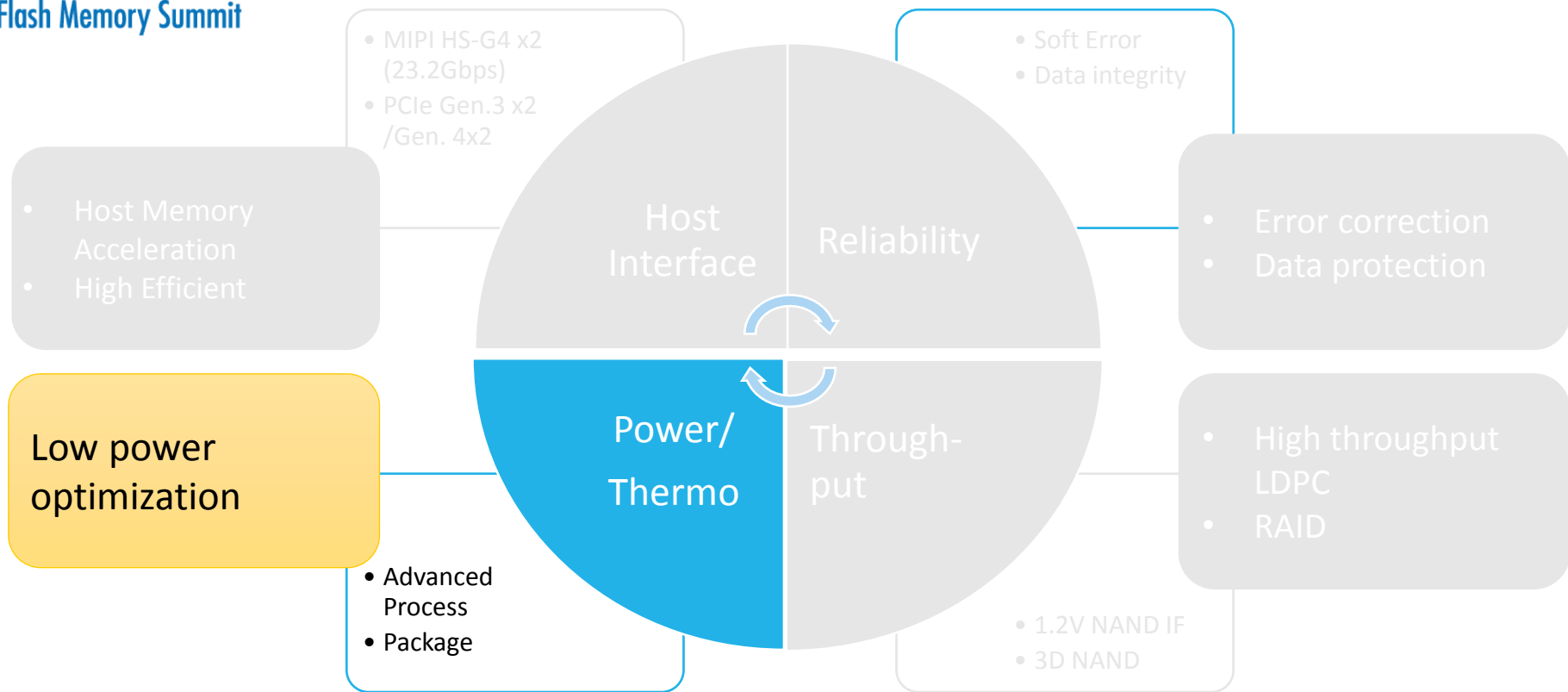
Performance/Throughput

- **1.2V 3D NAND can support 1200MT/s above**
- **2KB/4KB LDPC is expected for high throughput and higher performance**
- **Multi-core CPU**



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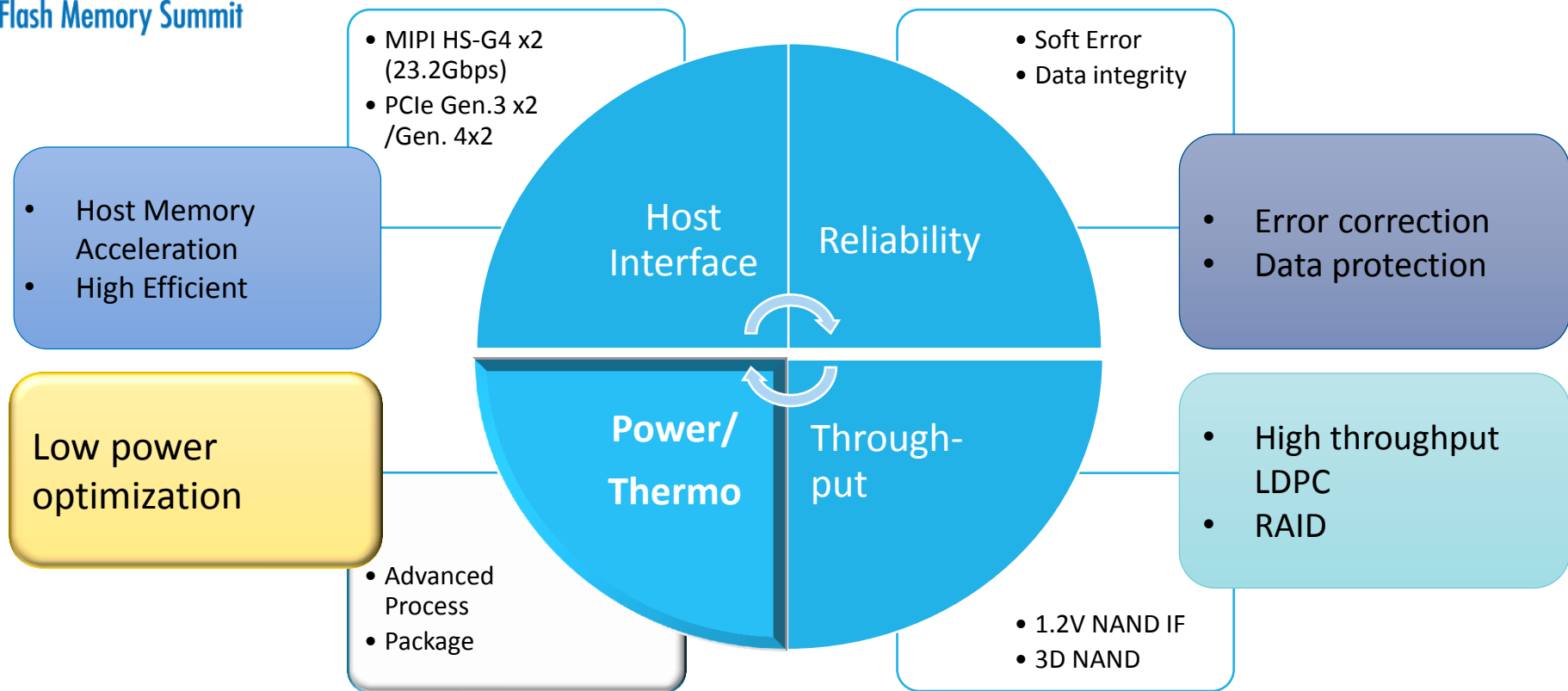
Power Consumption/Thermo

- **Advanced process with superior low leakage**
- **SRAM, Logic cell (SVT, HVT cell)**
- **Wire-bonding vs Flip-chip**



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Summary

- **Optimize the design of PCIe PHY/NVMe**
- **Consider the design trade-off between performance and power consumption**
- **PCIe/UFS3.x aim for Mobile computing and Automotive applications**



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Visit us at the Booth 413

Thank you

robert.hsieh@siliconmotion.com