Flash Memory Summit

3D NAND - Data Recovery and Erasure Verification

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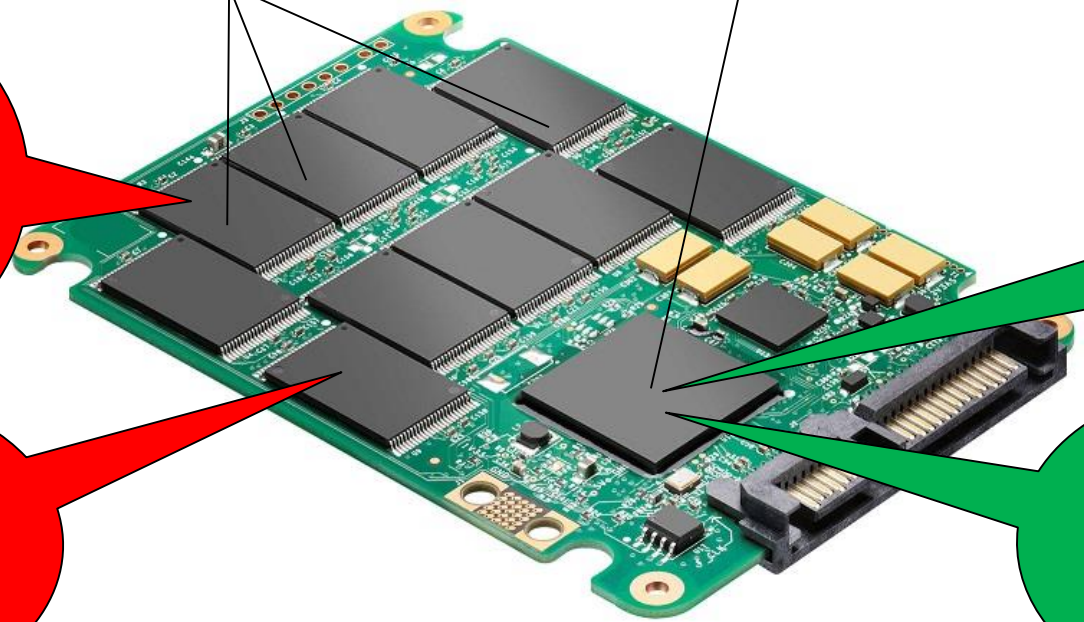
The Causes of SSD Data Loss – What can go wrong?

- Logical Damage
  - Data accidentally deleted, file system corrupted
- Physical Damage
  - Liquid, fire, physical stress
- Electronic components
  - Active and passive component failure
- Firmware
  - Main firmware cannot be loaded into memory from NAND reserved blocks
- System Area
  - Data tables corrupt or fail checksum
  - Improper shutdown caused loss of valid context / state information

NAND's Challenges and Controller's Solutions

- NAND has undesirable characteristics
- Controller must mitigate these through flash management techniques and Flash Translation Layer



Increase in BER
- Charge decay
- Inter-cell interference
- Read disturb
- Finite program-erase lifetime (write endurance)

Reduce bit errors
- Error correction (ECC)
- Data scrambling / encryption
- Wear-levelling

Others
- slow write-cycle
- block level only erase

Others
- Data striping
- Logical to physical (L2P) mapping
- Page & block management

- Physical data in NAND is not in its original format.
- Need to reverse controller's processing to restore original logical data

SSD Controller Recovery versus Chip-Off Recovery - Overview

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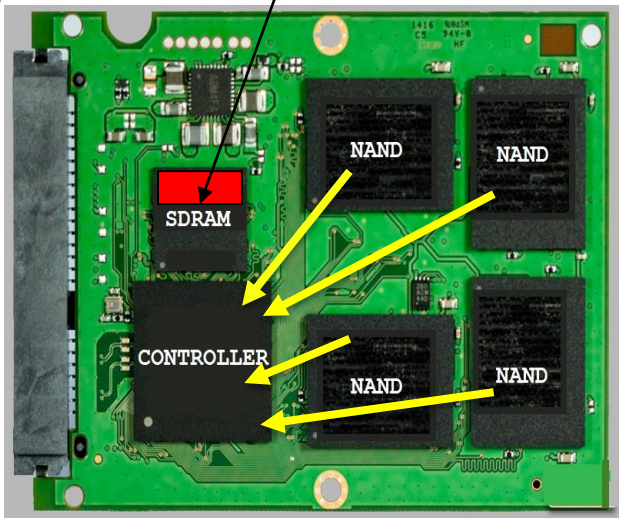
Transient firmware module



Data out *(Some external processing may still be required)*

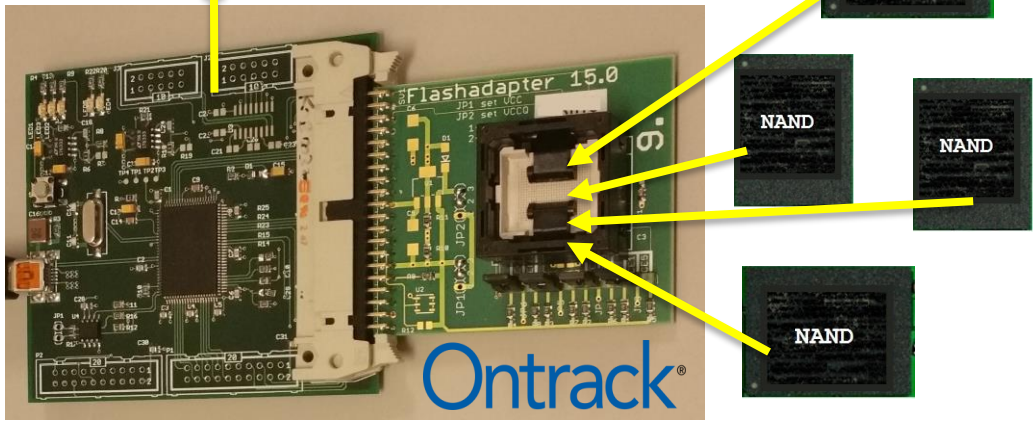
Special controller firmware processes physical NAND data

- Error-correction
- Descrambling / decryption
- Undo data striping
- Undo L2P mapping (possibly)
- Undo wear-levelling

Data out

Ontrack hardware & software processes physical NAND data

- Error-correction
- Descrambling / decryption
- Undo data striping
- Undo L2P mapping
- Undo wear-levelling



SSD Controller Recovery versus Chip-Off Recovery - Comparison

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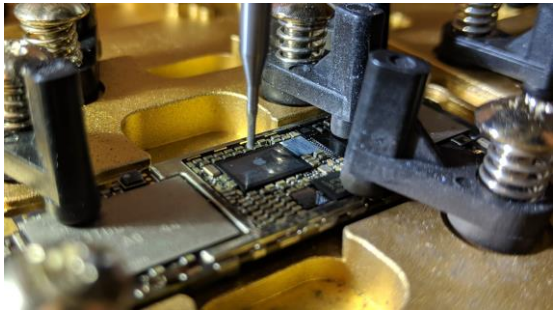
Advantages of Controller Recovery

- No need to heat NAND
- Faster recovery turnaround
- Easier - some / all processing (often) done for us by controller

Advantages of Chip-Off Recovery

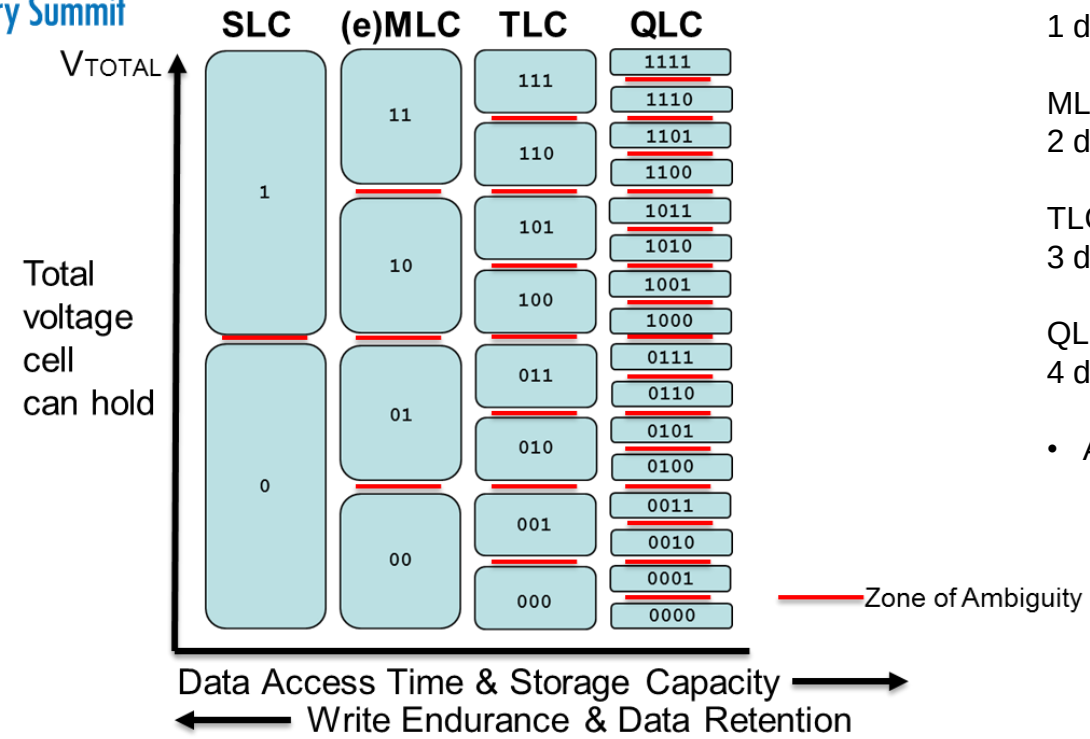
- None of the NAND is hidden from us
- We get a faithful copy of physical data
- Gain knowledge of controller internal processes
- Recovery still possible if:-
  - controller not functioning
  - no special firmware available
  - transient upload not supported by controller
  - Bad NAND element
  - SSD firmware damaged beyond repair
- Garbage collection / re-allocation is not changing flash content

The “Chip-Off” Recovery Process



- Remove NAND
  - Minimise heat during removal (or use milling) and re-balling
  - Avoid damage to package / pads
- Read NAND
  - Socket, pin-out (interface)
  - Logical addressing scheme (page, block, plane, die)
  - Command set
  - Use voltage control and read-retries (special features)
  - Error-correction
- Extract (re-assemble logical data copy)
  - Deal with striping, scrambling, decryption, L2P mapping etc..
    - Use information within SA where possible / applicable

NAND Cell Data Density (SLC, MLC, TLC and QLC)



SLC = Single-Level Cell:-
1 data bit represented per cell

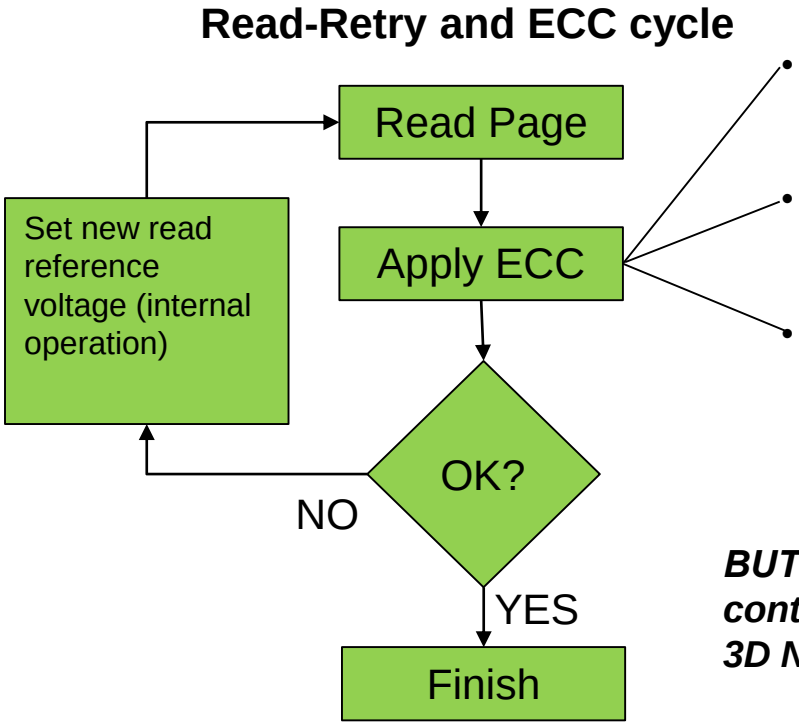
MLC = Multi-Level Cell:-
2 data bits represented per cell

TLC = Triple-Level Cell:-
3 data bits represented per cell

QLC = Quad-Level Cell:-
4 data bits represented per cell

- As cell data density increases:-
  - Storage capacity, data access latency increases.
  - Write endurance and data retention decreases
  - Bit Error Rate (BER) increases as does the need for Read-Retry and better ECC algorithms

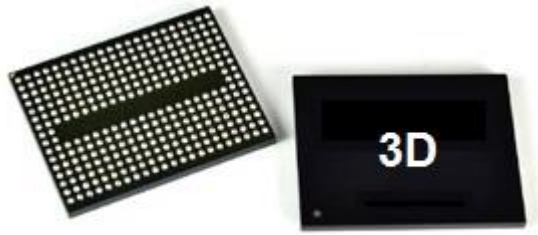
MLC, TLC and QLC NAND – Error Correction (ECC)

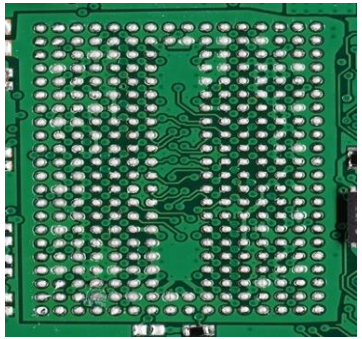


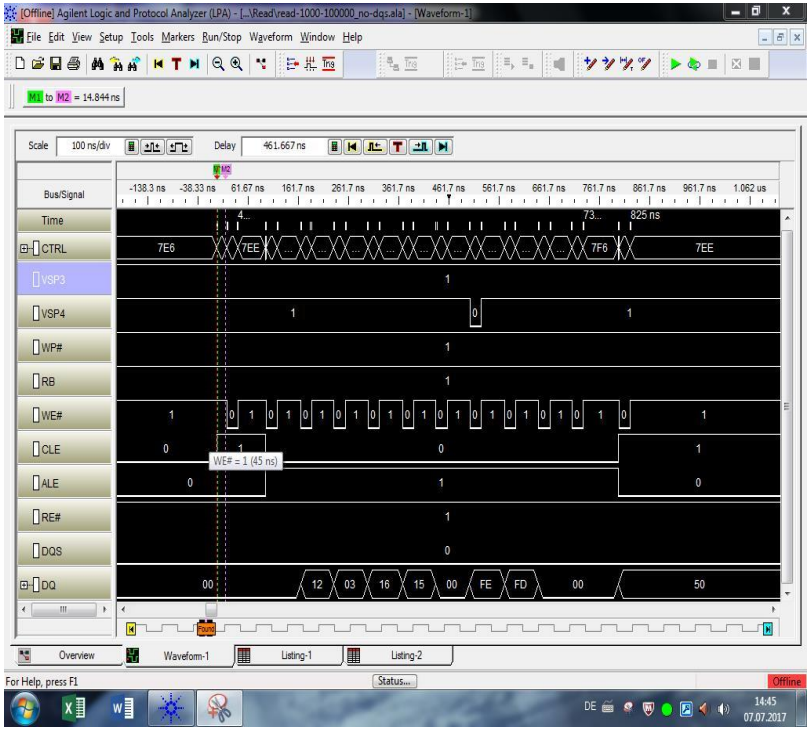
- BCH (Bose–Chaudhuri–Hocquenghem)
  - hard-decision decoding with read-retry
- LDPC – (Low-Density Parity Check)
  - supports soft-decision decoding with read-retry
- Adaptive LDPC
  - code changes throughout life of NAND
  - smaller (weaker) ECC when new
  - larger (stronger) ECC as NAND ages

BUT… Adoption of LDPC seems to be more to do with controller development roadmap than a requirement of 3D NAND due to current use of MLC!

3D NAND – New Challenges - Reading







- Custom (non-ONFI) pinout
- Vendor-unique signals
- Extended addressing modes
- Vendor-unique commands
- New set features parameters
- New read-retry thresholds

3D NAND – New Challenges - Processing

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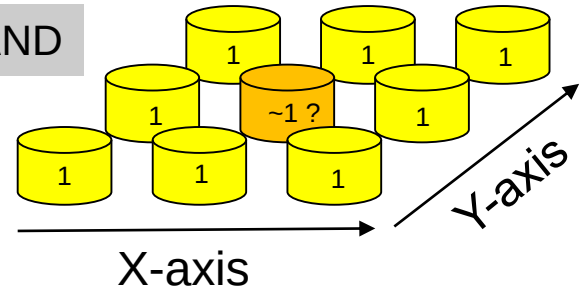
Data randomisation pattern is XOR'ed with user data before storage in NAND to reduce the occurrence of bit patterns which can cause inter-cell interference

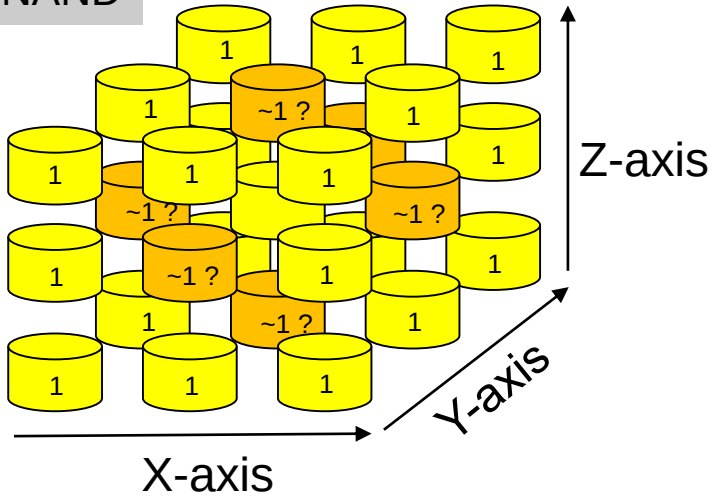
1 = cell programmed / erased with '1'

~1 ? = victim cell, was programmed with '0' …but reads closer to '1'

2D NAND

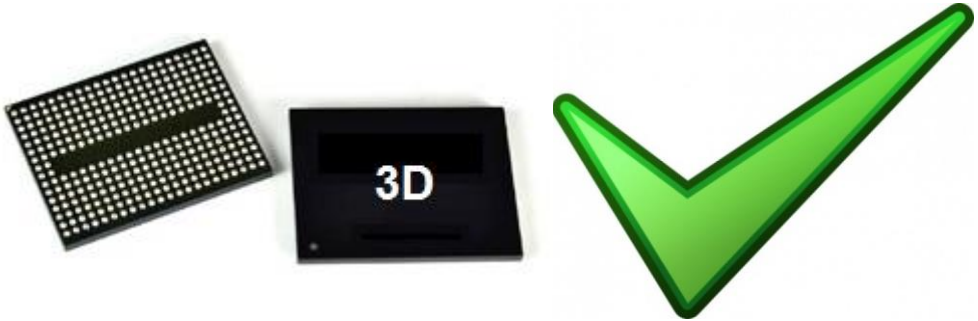


3D NAND



- Data randomisation pattern generated typically using LFSR (Linear-Feedback Shift Register)
- Polynomial and pattern distribution tailored to physical layout of NAND
- 3D NAND adds Z-axis

The **Benefits** of 3D NAND to Data Recovery



Low BER (Bit Error Rate)

- 3D NAND is mostly MLC

- Has a bigger cell size than 2D TLC
  - May change as cell size shrinks and 3D TLC is adopted but is good news for us right now!

- Low BER helps data recovery:-
  - Requires less-intensive ECC which improves speed of processing
  - Fewer read-retries required, which improves chip imaging speed
  - Fewer uncorrectable pages, which simplifies mapping and increases quality of recovered data

Ontrack SSD Erasure Verification Service (EVS)

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Purpose

- Tests the real-world effectiveness of a data erasure / sanitization method on SSD (also HDD) for manufacturers, vendors and integrators (among others)

Procedure

- Write known byte patterns to all logical blocks (two pass, two different byte values)
- Run client's erase process, then analyse:-

Level I (Logical)

- Read LBAs via SSD interface, look for known data pattern (also include host-protected logical areas)

Level II (Physical)

- In-depth examination of all SSD NAND flash content using "Chip-Off"

Summary

- “Chip-Off” is needed for proper Erasure Verification on SSD and some SSD failure modes make this approach the only way to recover data
- Initially a steep learning curve to add support for 3D NAND as there are vendor-unique elements associated with reading and new challenges in processing
- However, **3D NAND is good news for Data Recovery!** The current generation of 3D NAND is MLC, so there are real benefits over 2D TLC NAND
- We enjoy working with NAND vendors, drive manufacturers and controller chip manufacturers and collaboration helps us deliver a better service to our mutual clients

Thank You!

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