Artificial Neural Network Coupled LDPC ECC for 3D-NAND Flash Memories

Toshiki Nakamura and Ken Takeuchi

Chuo University, Japan

Outline

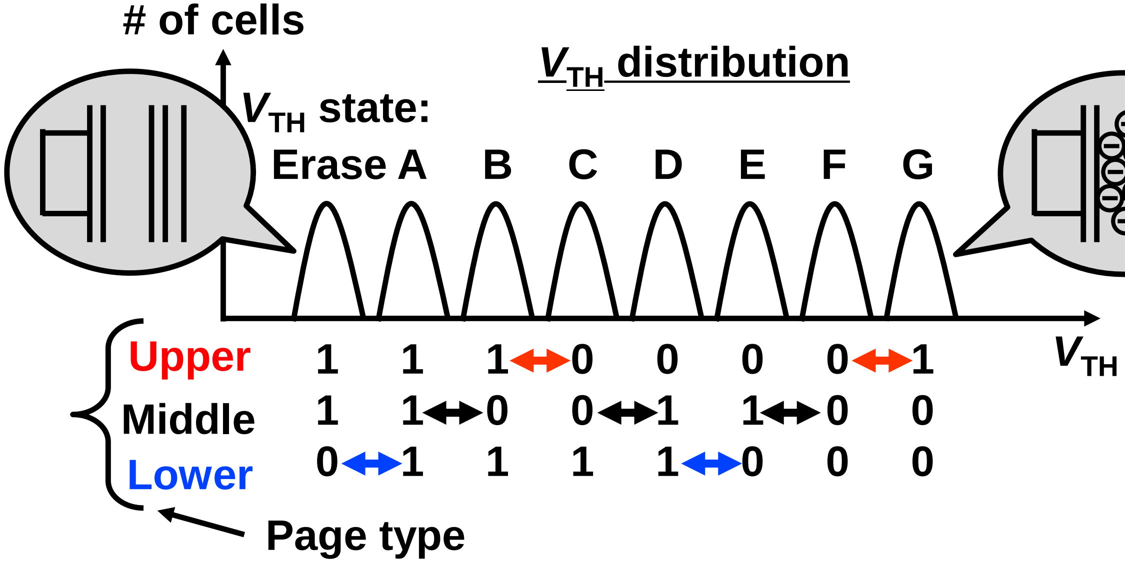
- Introduction
- Proposed Artificial Neural Network Coupled (ANN) LDPC ECC (ANN-LDPC ECC)
  - Training of ANN
  - Case 1-3 (1 hidden layer ANN)
  - Case 4 and 5 (2 hidden layer ANN)
- Conclusion

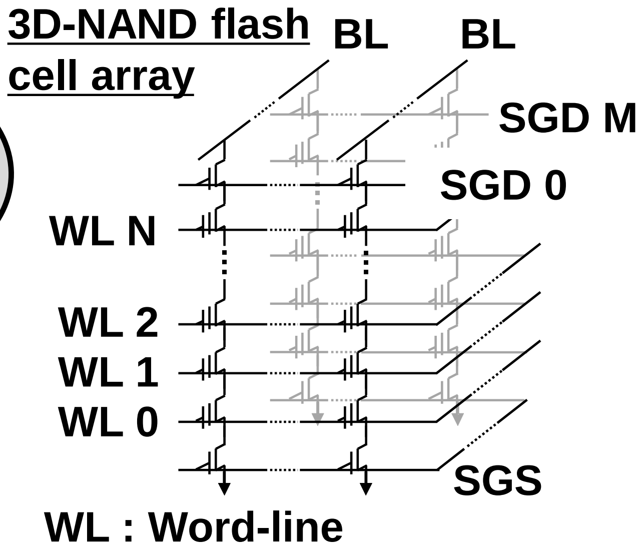
Outline

- Introduction
- Proposed Artificial Neural Network Coupled (ANN) LDPC ECC (ANN-LDPC ECC)
  - Training of ANN
  - Case 1-3 (1 hidden layer ANN)
  - Case 4 and 5 (2 hidden layer ANN)
- Conclusion

3D-TLC NAND Flash Memory

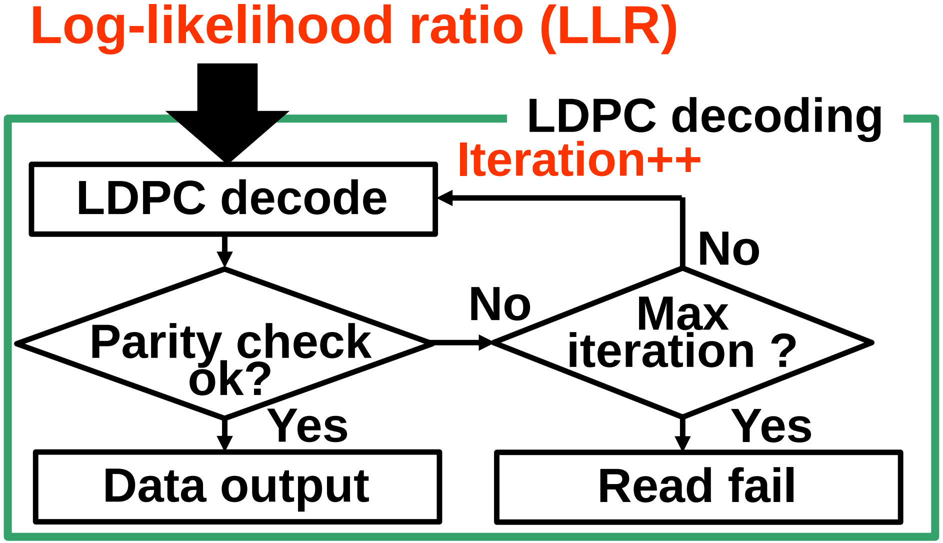
- TLC NAND flash memory stores 3 bits/cell
- Data is stored by controlling amount of electrons



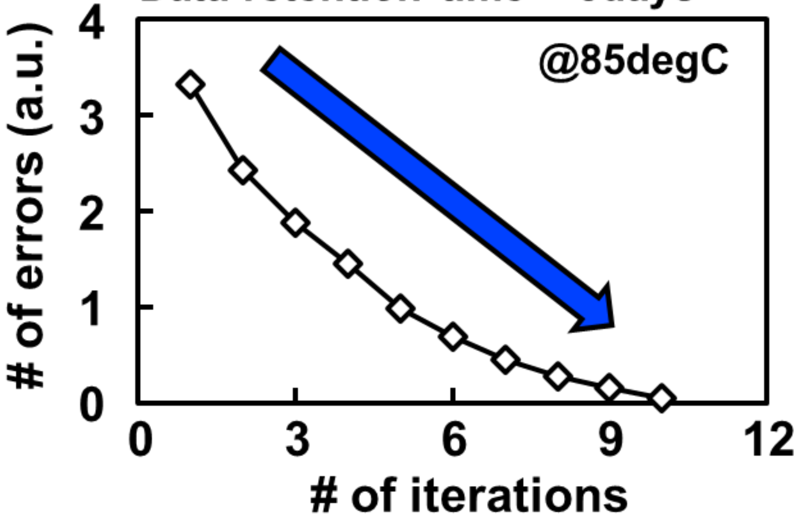


Low-Density Parity-Check (LDPC) ECC

- LDPC ECC corrects errors gradually by repeating decoding
- Log-likelihood ratio (LLR) is required for LDPC decoding

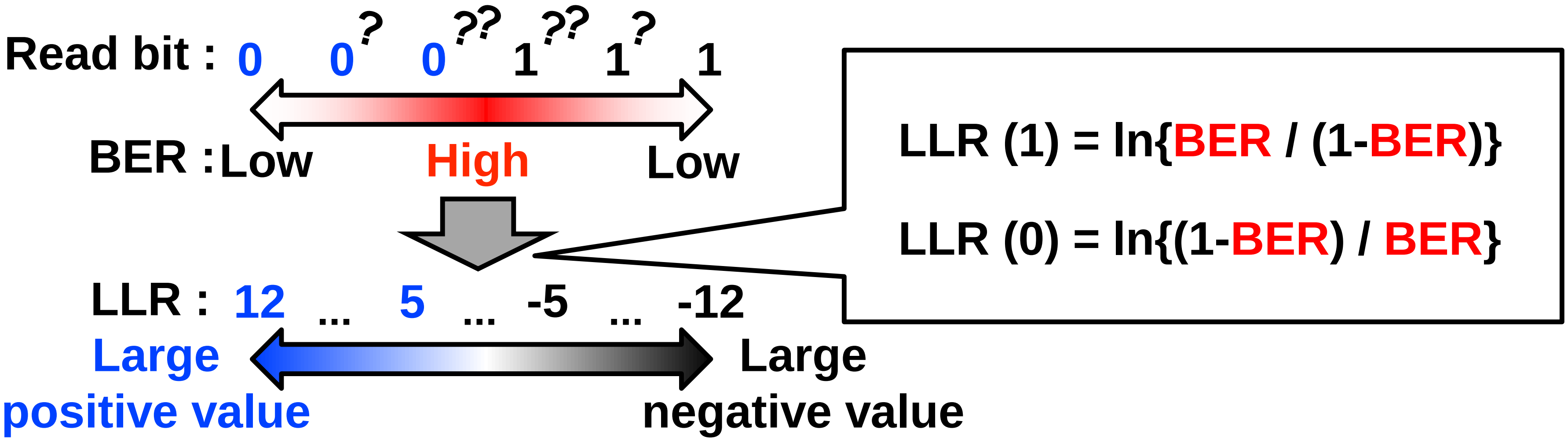


Charge-trap 3D-TLC NAND flash,
Write/erase cycles ($N_{W/E}$) = 500,
Data-retention time = 3days



Relation between LLR and BER

- **LLR represents reliability of each bit data**
- **Error-correcting capability depends on accuracy of LLR**
- **LLR is calculated based on bit-error rate (BER)**



Read bit : 0 0? 0?? 1?? 1? 1

BER : Low High Low

LLR : 12 ... 5 ... -5 ... -12

Large positive value

Large negative value

LLR (1) = ln{BER / (1-BER)}

LLR (0) = ln{(1-BER) / BER}

Problem of Conventional LDPC ECC

- **BER varies complicatedly in 3D-NAND flash**

  ➡ **Conventional LDPC ECC cannot predict BER precisely**

Reliability parameters of 3D-NAND flash

Static information

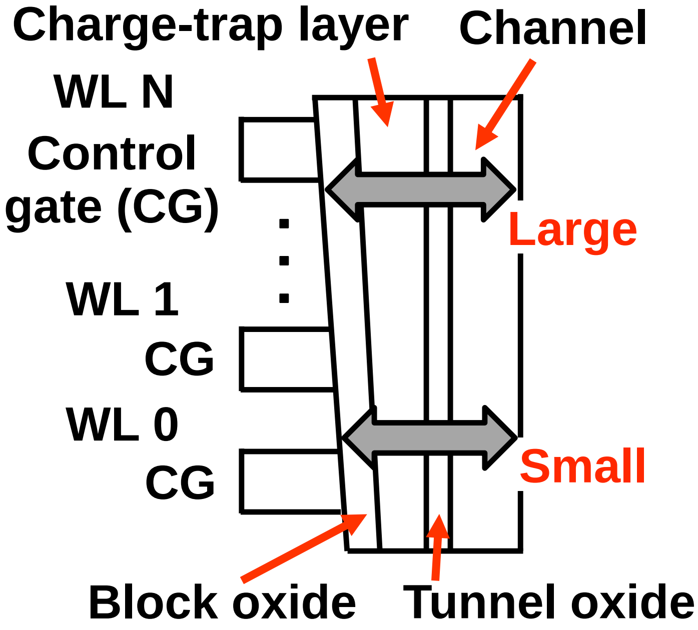
- V_{TH} **state**
- **Page type (Lower/Middle/Upper)**
- **Neighboring cell data**
- **WL number**

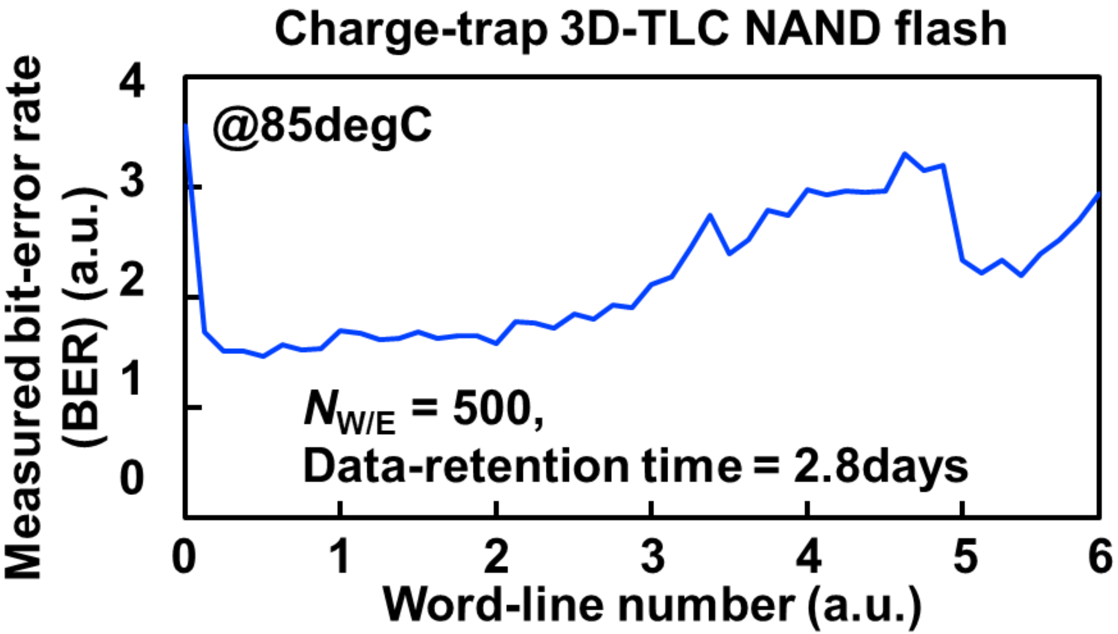
Dynamic information

- **Data-retention time**
- **Write/erase cycles**

Word-line Variations

- Complicated inter word-line variations of errors exist [1]

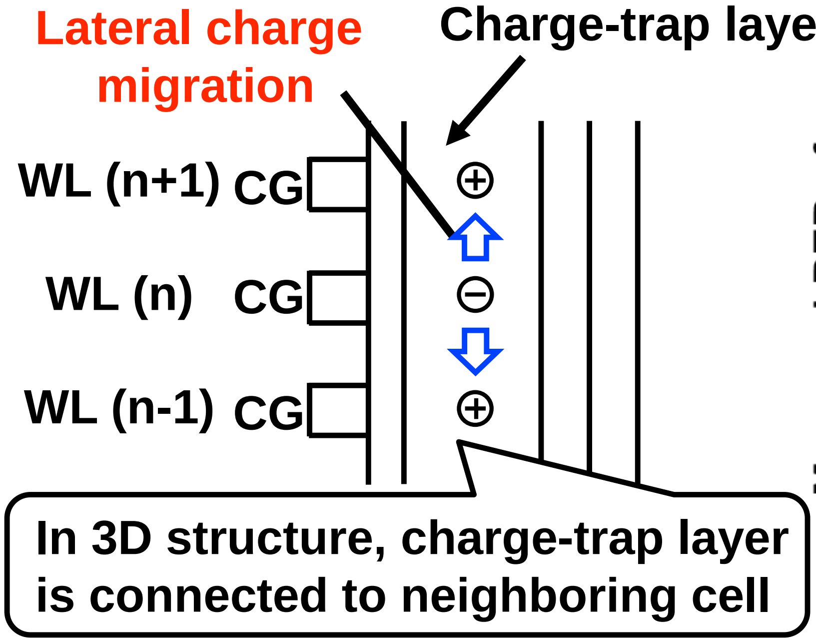




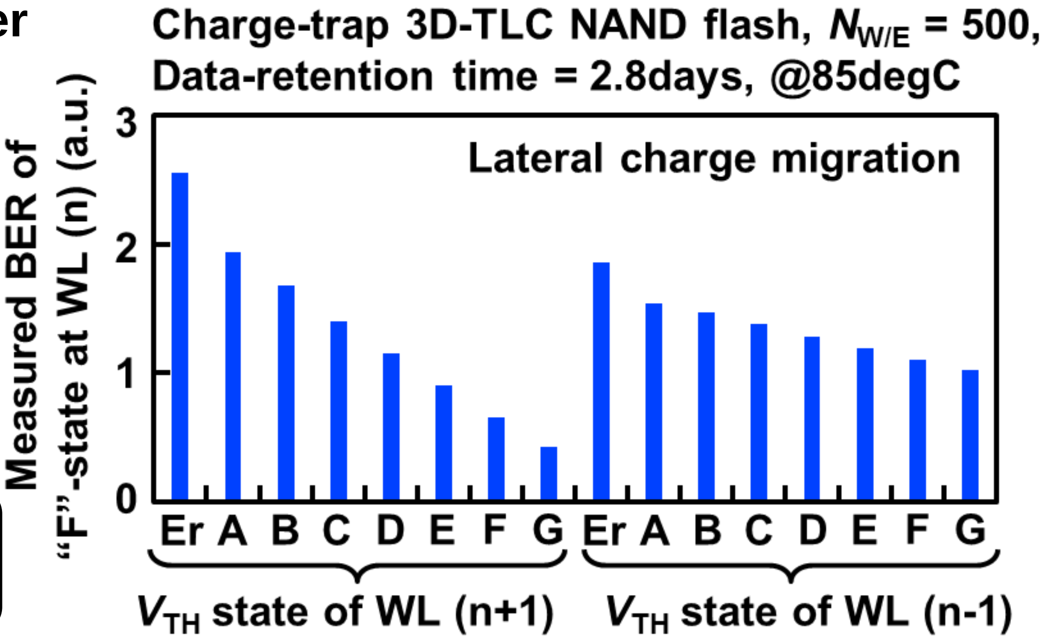
[1] K. Mizoguchi *et al.*, *IMW*, pp. 119-122, May 2017

Lateral Charge Migration

- Charge loss is caused by lateral charge migration [2]



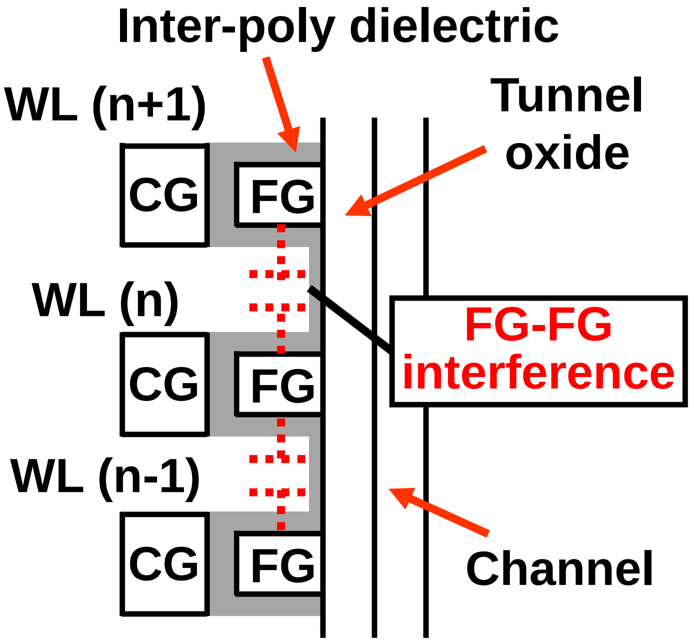
In 3D structure, charge-trap layer is connected to neighboring cell

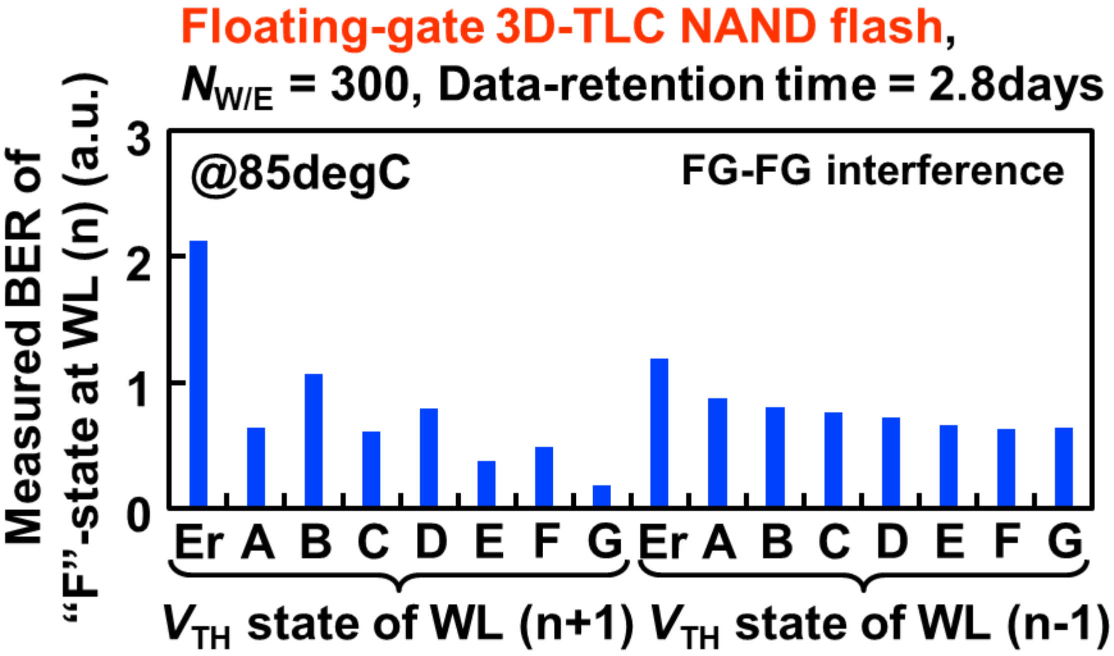

Charge-trap 3D-TLC NAND flash, $N_{W/E}$ = 500, Data-retention time = 2.8days, @85degC

[2] B. Choi *et al.*, *Symp. VLSI Tech.*, pp. 78-79, June 2016

Floating-Gate (FG) Cell

- Inter floating-gate capacitive coupling noise cause errors [3]





[3] K. Parat and C. Dennison, *IEDM* pp. 3.3.1-3.3.4, Dec. 2015.

Concept of Proposed ANN-LDPC

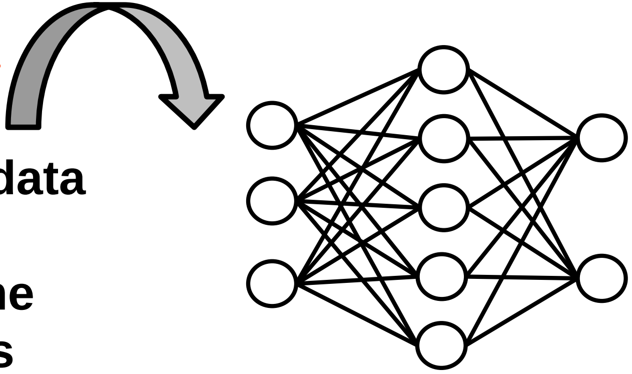
Read data → **Input parameter x** $\xrightarrow{x_1 \sim x_K}$ **Predict BER** $\xrightarrow{\text{BER}}$ **Calculate LLR** $\xrightarrow{\text{LLR}}$ **LDPC decode**

Proposed Artificial Neural Network Coupled (ANN) LDPC ECC (ANN-LDPC ECC)

Reliability parameters of 3D-NAND flash

Input

- V_{TH} state
- Page type
- Neighboring cell data
- WL number
- Data-retention time
- Write/erase cycles



Output

Predicted BER

○ **Proposed ANN-LDPC adaptively and automatically correct errors [4]**

[4] T. Nakamura *et al*., *CICC*., Apr. 2018

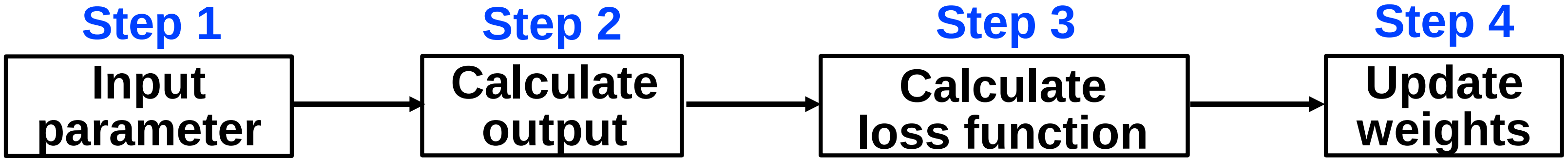
Outline

- Introduction
- Proposed Artificial Neural Network Coupled (ANN) LDPC ECC (ANN-LDPC ECC)
    - Training of ANN
    - Case 1-3 (1 hidden layer ANN)
    - Case 4 and 5 (2 hidden layer ANN)
- Conclusion

Training of ANN

Training flowchart

Supervised learning



Step 1

Input parameter

Step 2

Calculate output

Step 3

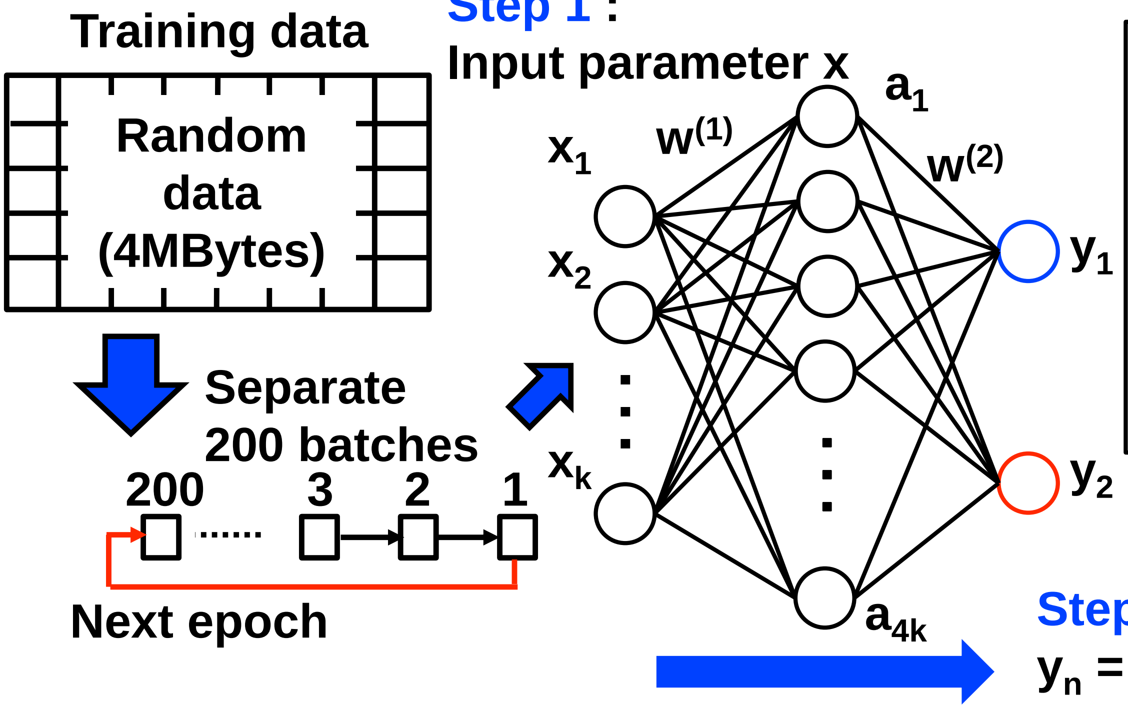
Calculate loss function

Step 4

Update weights

- **Training of ANN is performed before product shipment**
- **Calculated synaptic weights are pre-recorded in proposed storage controller**

Training of ANN (Step 1 and 2)



Training data

Random data (4MBytes)

Separate 200 batches

Next epoch

Step 1 : Input parameter x

Activation function

- ReLU (hidden layer)

$$h_1(x) = \begin{cases} x & (x \geq 0) \\ 0 & (x < 0) \end{cases}$$

- Softmax (output layer)

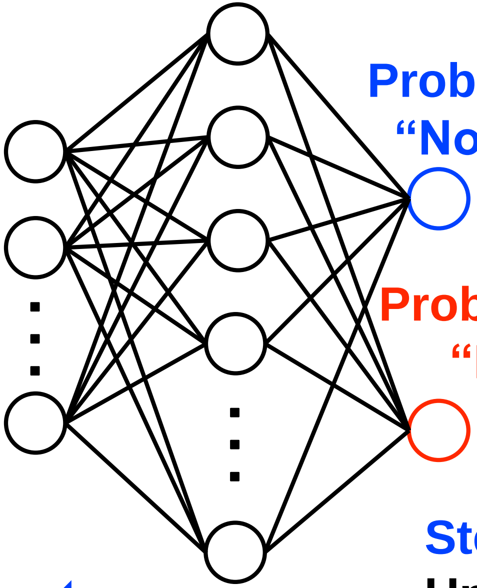
$h_2(x_n) =$
$\exp(x_n) / \{\exp(x_1) + \exp(x_2)\}$

Step 2 : Calculate output y

$$y_n = h_2\{\sum w^{(2)} h_1(\sum w^{(1)} x)\}$$

Training of ANN (Step 3 and 4)

Step 3 : Calculate loss function E



Probability of “Not error”

y_1 ←··· **Answer, L_1**

Probability of “Error”

y_2 ←··· **Answer, L_2**

Loss function

- **Softmax cross entropy**

$$E = - \{L_1 \ln(y_1) + L_2 \ln(y_2)\}$$

Ex. 1 : Bad training

$$\begin{cases} y_1 = 0.9,\ L_1 = 0 \\ y_2 = 0.1,\ L_2 = 1 \end{cases} \quad E = - \ln(0.1) = 2.3$$

Ex. 2 : Good training

$$\begin{cases} y_1 = 0.1,\ L_1 = 0 \\ y_2 = 0.9,\ L_2 = 1 \end{cases} \quad E = - \ln(0.9) = 0.1$$

Step 4 :

Update weights

←

Backpropagation

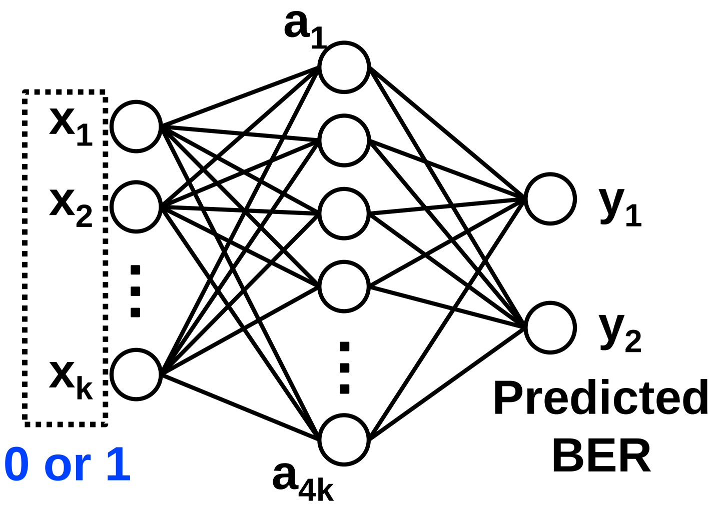
Outline

- Introduction
- Proposed Artificial Neural Network Coupled (ANN) LDPC ECC (ANN-LDPC ECC)
    - Training of ANN
    - Case 1-3 (1 hidden layer ANN)
    - Case 4 and 5 (2 hidden layer ANN)
- Conclusion

Case 1-3 (1 Hidden Layer ANN)

- Case 1-3 consider only static information
- Value of input parameters is 0 or 1

1 hidden layer ANN



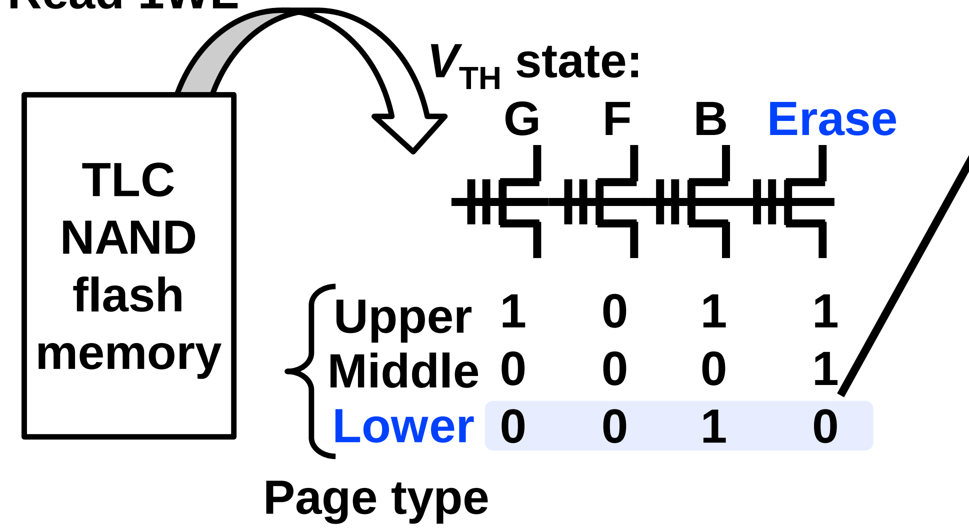
	Input parameters	Case 1	Case 2	Case 3
Static Information	V_{TH} state	○	○	○
	Page type	○	○	○
	Neighboring cell data		○	○
	WL number		○	○
	Read offset level			○

Example : Input Parameters of Case 1

Ex.

V_{TH} state : "Erase" ⋯▸ $x_1 = 1$

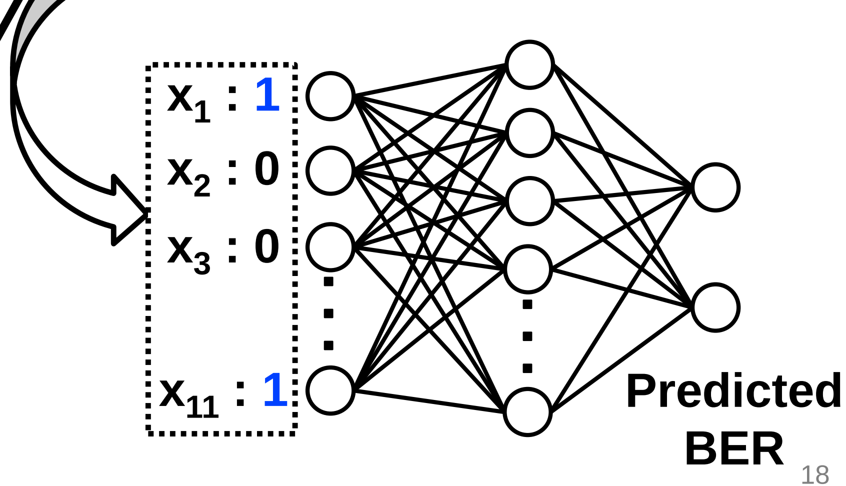
Page type : "Lower" ⋯▸ $x_{11} = 1$



	G	F	B	Erase
Upper	1	0	1	1
Middle	0	0	0	1
Lower	0	0	1	0

Page type

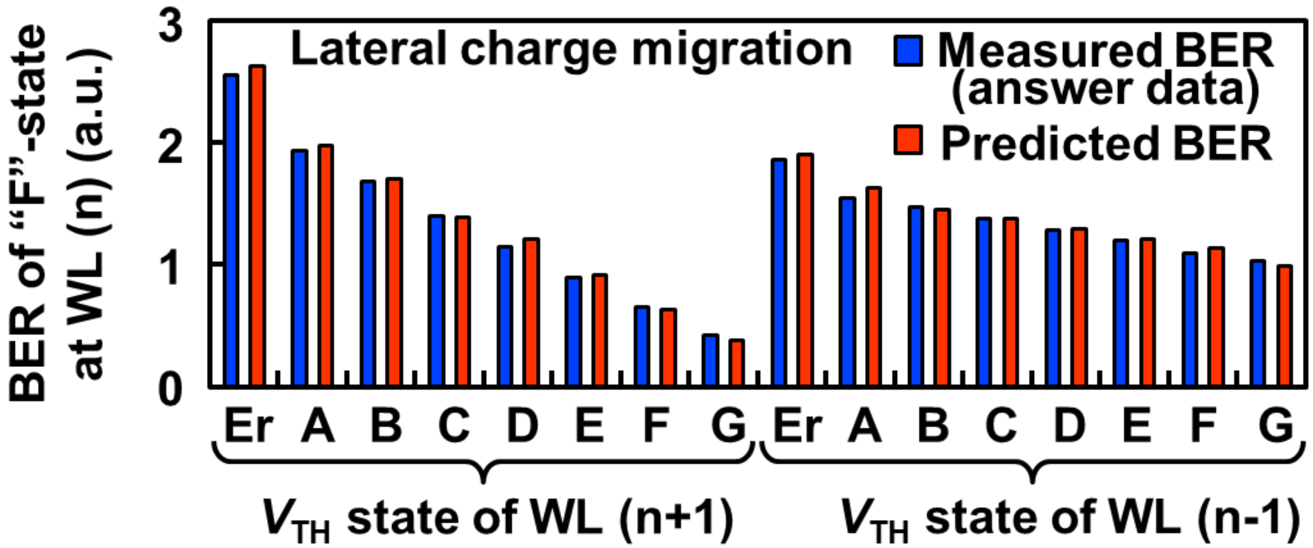
Input parameters						
V_{TH} state				Page type		
Erase	A	…	G	U	M	L
x_1	x_2	…	x_8	x_9	x_{10}	x_{11}
1	0	…	0	0	0	1



Predicted BER of Case 2

- Case 2 reproduces lateral charge migration successfully

Charge-trap, $N_{W/E}$ = 500, Data-retention time = 2.8days, @85degC

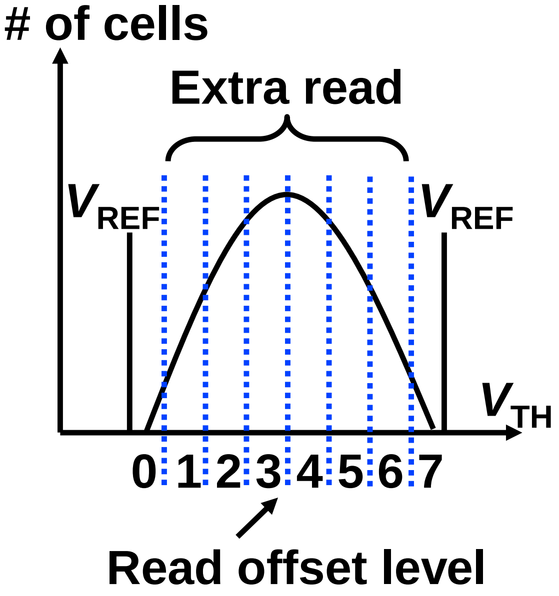


Case 2 Input parameters
V_{TH} state
Page type
Neighboring cell data
WL number

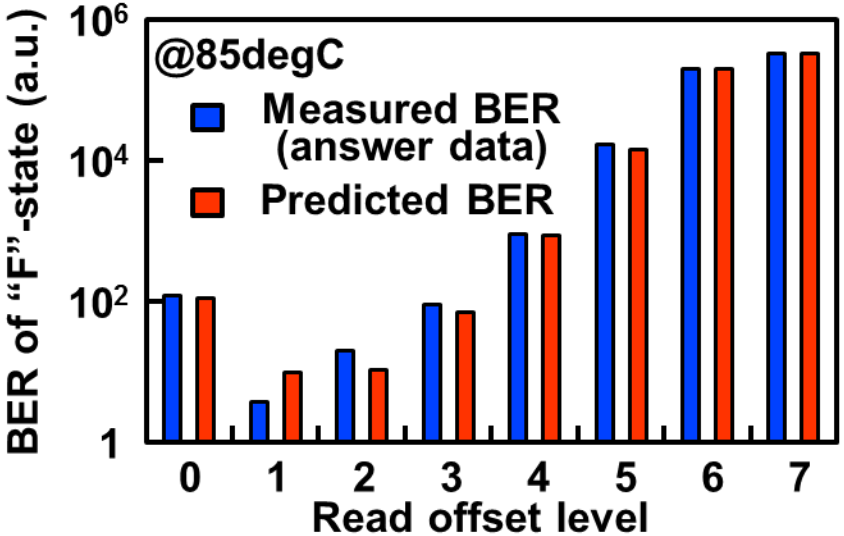
- More precise BER is obtained to consider analog V_{TH}

Predicted BER of Case 3

- In Case 3, analog V_{TH} value within each V_{TH} state is included



Charge-trap, $N_{W/E}$ = 500, Data-retention time = 18days

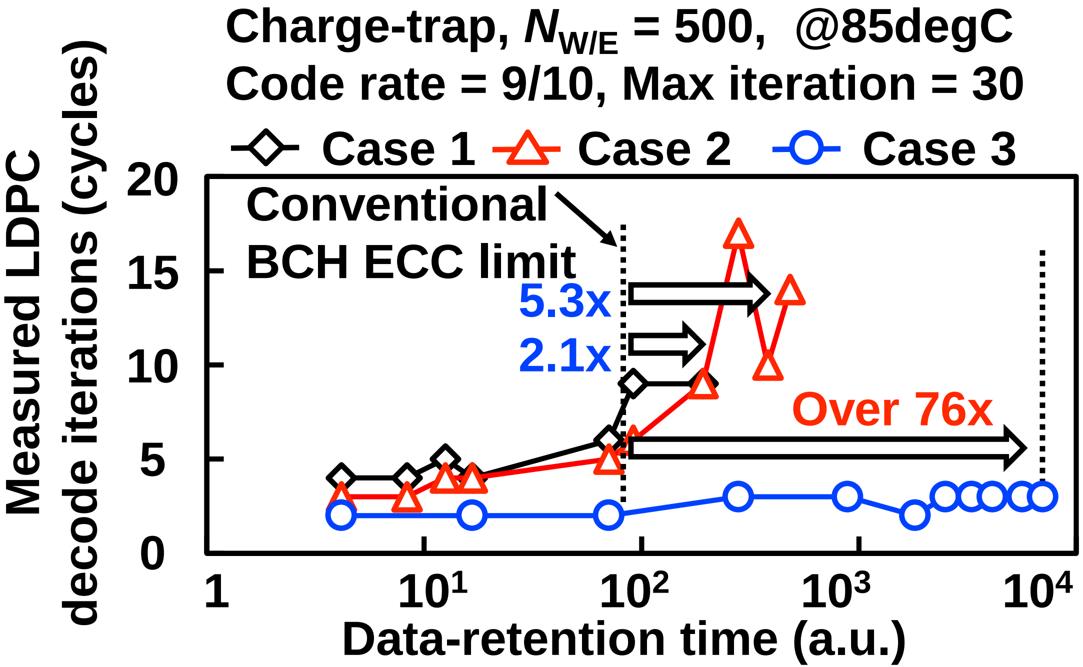


Case 3 input parameters
V_{TH} state
Page type
Neighboring cell data
WL number
Read offset level

- BER is most precisely predicted with extra reads

Case 1-3 Decoding Result

- **Acceptable data-retention time increases by 76-times**



Charge-trap, $N_{W/E}$ = 500, @85degC
Code rate = 9/10, Max iteration = 30

Input parameters	Case 1	Case 2	Case 3
V_{TH} state	○	○	○
Page type	○	○	○
Neighboring cell data		○	○
WL number		○	○
Read offset level			○

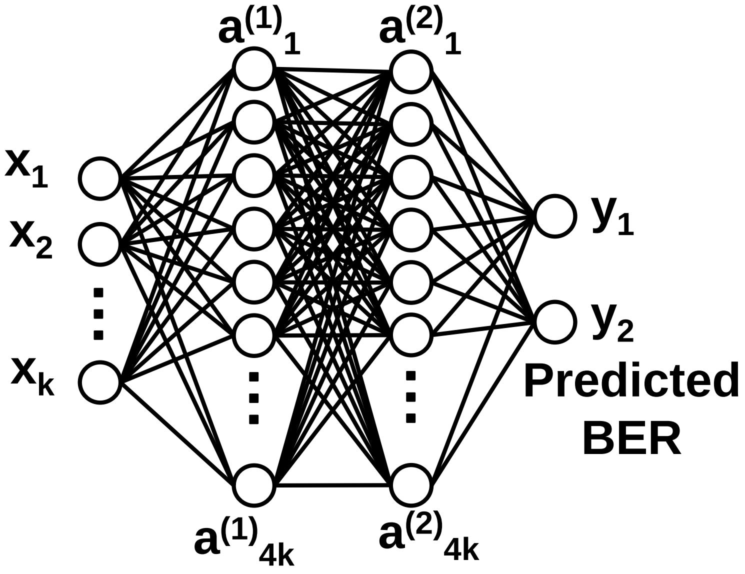
Outline

- Introduction
- Proposed Artificial Neural Network Coupled (ANN) LDPC ECC (ANN-LDPC ECC)
  - Training of ANN
  - Case 1-3 (1 hidden layer ANN)
  - Case 4 and 5 (2 hidden layer ANN)
- Conclusion

Case 4 and 5 (2 Hidden Layer ANN)

- Case 4 and 5 consider both static and dynamic information

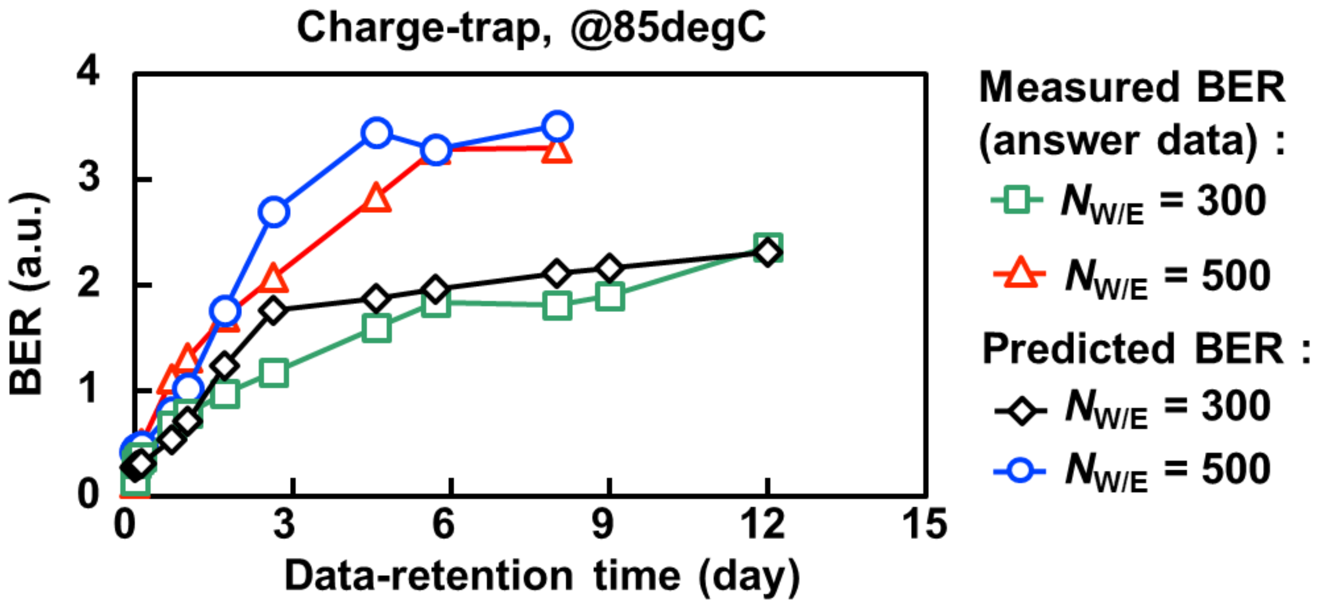
2 hidden layer ANN



Input parameters		Case 4	Case 5
Static information	V_{TH} state	○	○
	Page type	○	○
	Neighboring cell data		○
	WL number		○
Dynamic Information	Data-retention time	○	○
	Write/erase cycles	○	○

Predicted BER of Case 4

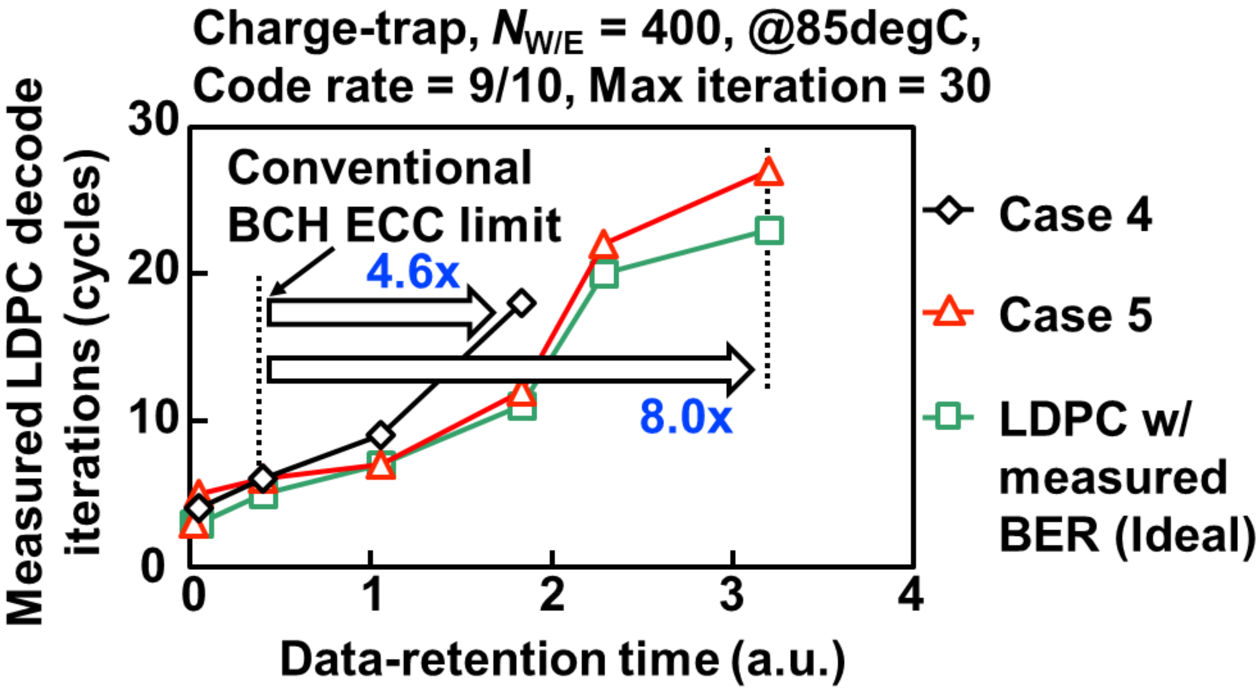
- Predicted BER fits well with measured BER at various data-retention time and endurance



Case 4 Input parameters
V_{TH} state
Page type
Data-retention time
Write/erase cycles

Case 4 and 5 Decoding Result

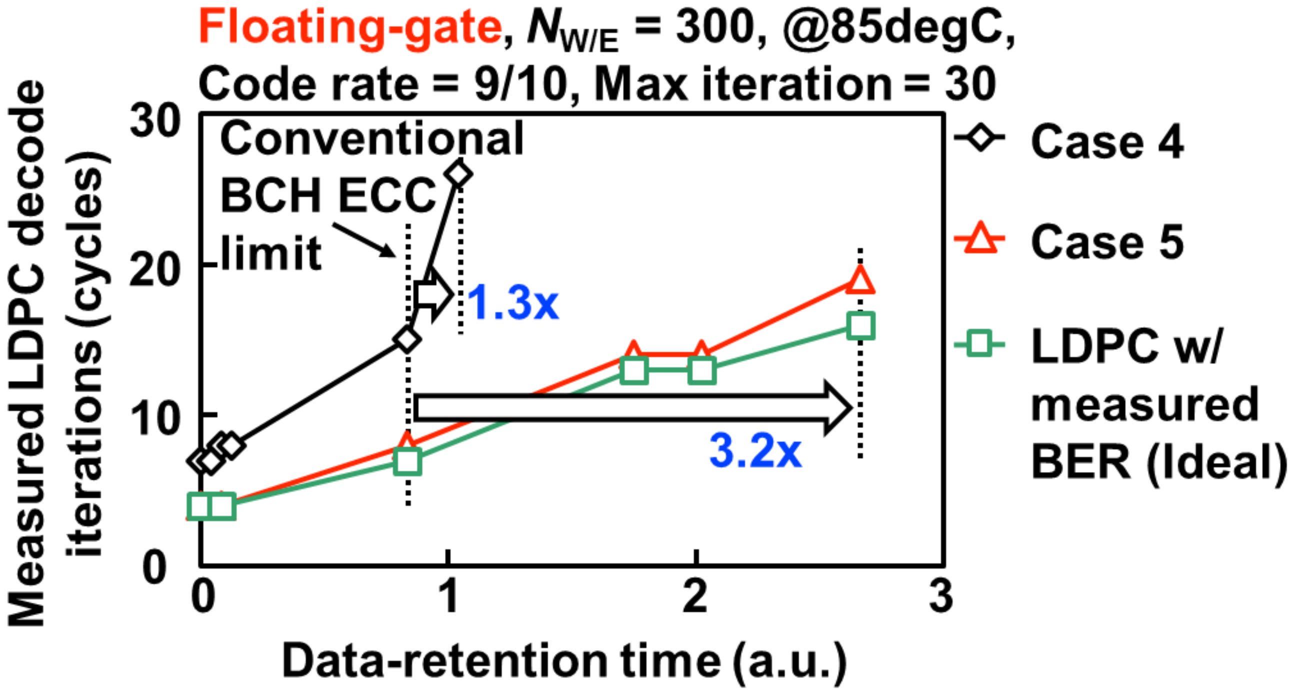
- **Acceptable data-retention time increases by 8-times**



Input parameters	Case 4	Case 5
V_{TH} state	○	○
Page type	○	○
Neighboring cell data		○
WL number		○
Data-retention time	○	○
Write/erase cycles	○	○

Case 4 and 5 Decoding Result

- **ANN corrects errors in both charge-trap and floating-gate 3D-NAND**



Input parameters	Case 4	Case 5
V_{TH} state	○	○
Page type	○	○
Neighboring cell data		○
WL number		○
Data-retention time	○	○
Write/erase cycles	○	○

Outline

- Introduction
- Proposed Artificial Neural Network Coupled (ANN) LDPC ECC (ANN-LDPC ECC)
    - Training of ANN
    - Case 1-3 (1 hidden layer ANN)
    - Case 4 and 5 (2 hidden layer ANN)
- Conclusion

Conclusion

Charge-trap 3D-TLC NAND flash	$N_{W/E}$ = 500			$N_{W/E}$ = 400	
	Case 1	Case 2	Case 3	Case 4	Case 5
Read operation	$7V_{REF}$ sensing (1WL)	$21V_{REF}$ sensing (3WL)	$77V_{REF}$ sensing (3WL)	$7V_{REF}$ sensing (1WL)	$21V_{REF}$ sensing (3WL)
Acceptable data-retention time compared with BCH ECC	2.1x	5.3x	Over 76x	4.6x	8.0x
Weight table size	22MB	928MB	1.1GB	14KB	490KB

- Case 5 achieves high reliability with small weight tables
- Case 3 is applied if reliability is seriously degraded

Thank you for your attention

This work was supported by JST CREST Grant Number JPMJCR1532, Japan