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Measuring 3D NAND Voltage Distributions and Optimized Read Threshold Calibration

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Think Bucket

- 3D array of buckets
- fill with water to store information
- we can overfill, spill, leak, etc

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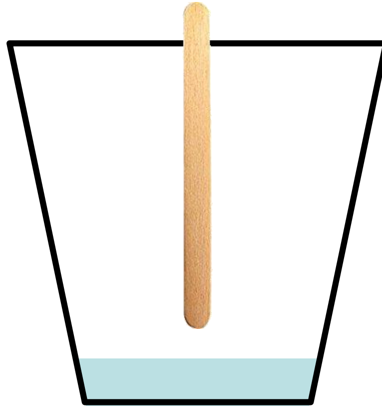
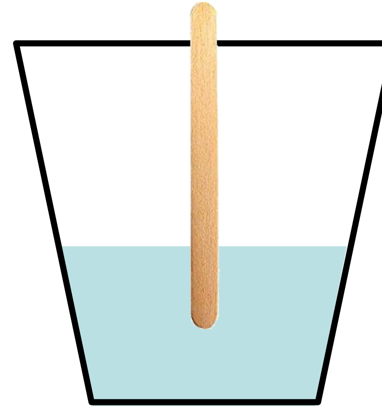
Measuring the Water Level

- insert stick





stick is dry – read as 1

stick is wet – read as 0

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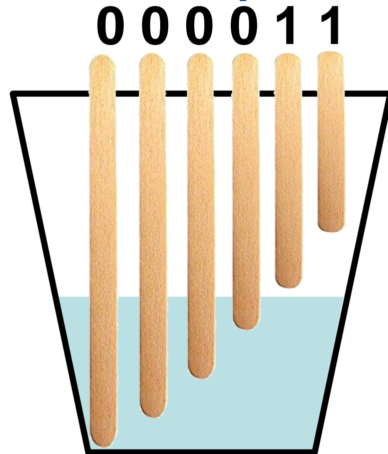
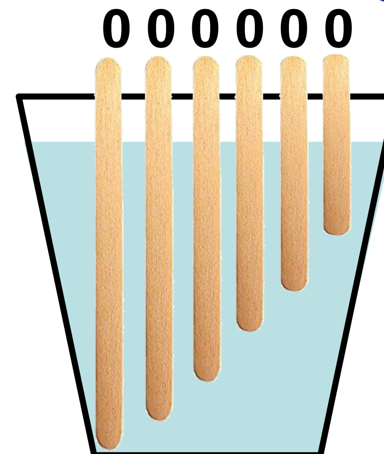
How Wet is Wet?

- accurate measurement of water level?
- insert multiple sticks of different lengths





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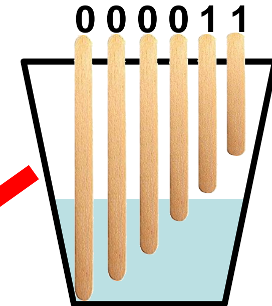
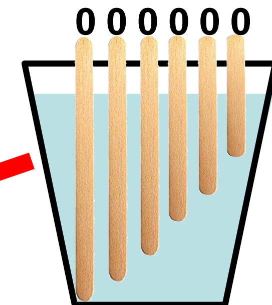
Getting the Distribution

70
60
50
40
30
20
10
0





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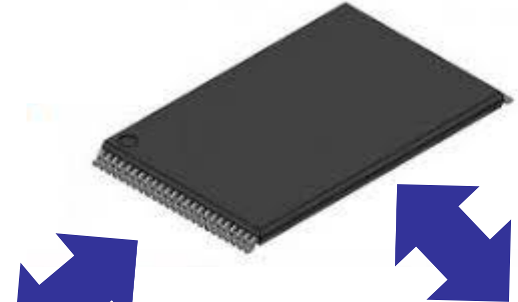
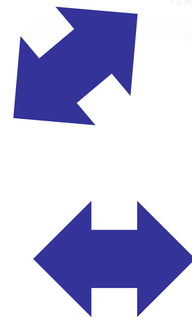
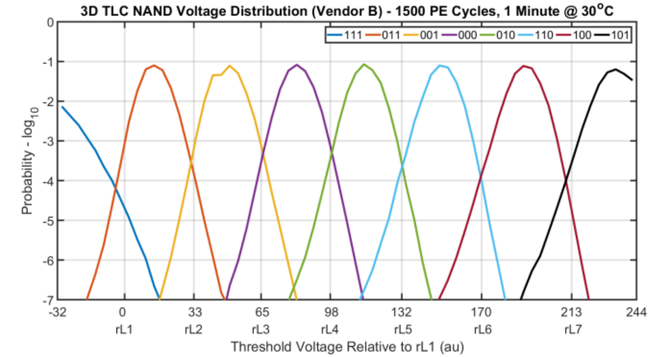
Making the Connection

- bucket – floating gate
- water – electrons
- stick – read threshold







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Well… Almost

- NAND limitations
  - can we change the read thresholds?
  - can we read using a single threshold?
  - is the range of thresholds available large enough to capture the extremes of the voltage distribution?
  - can me make these measurements quickly?

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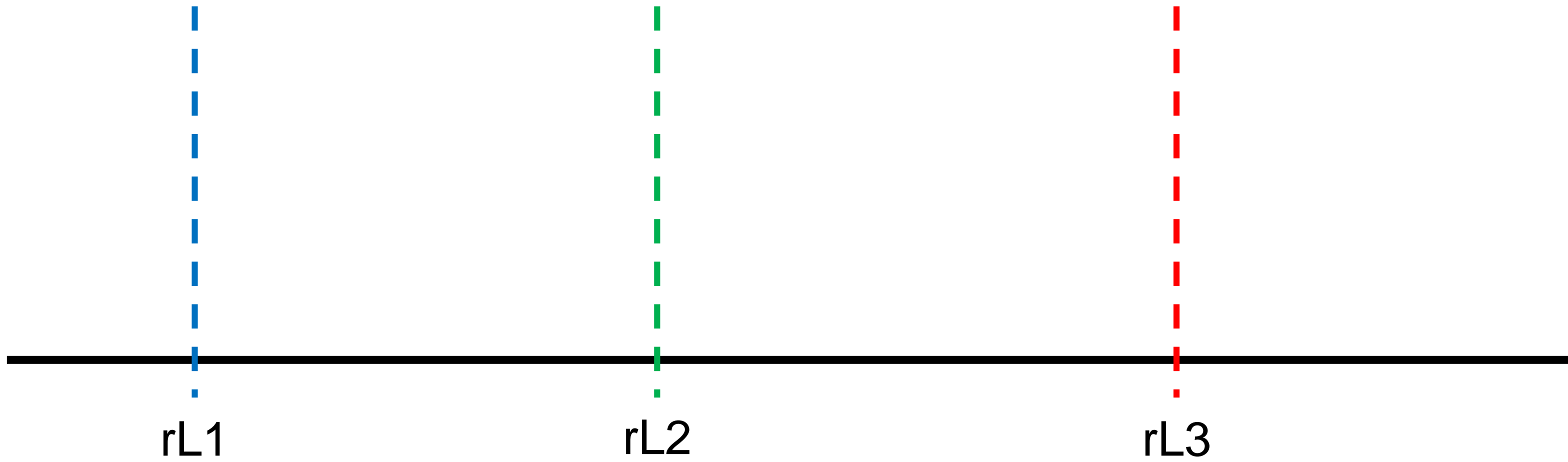
The Technical Part (1)



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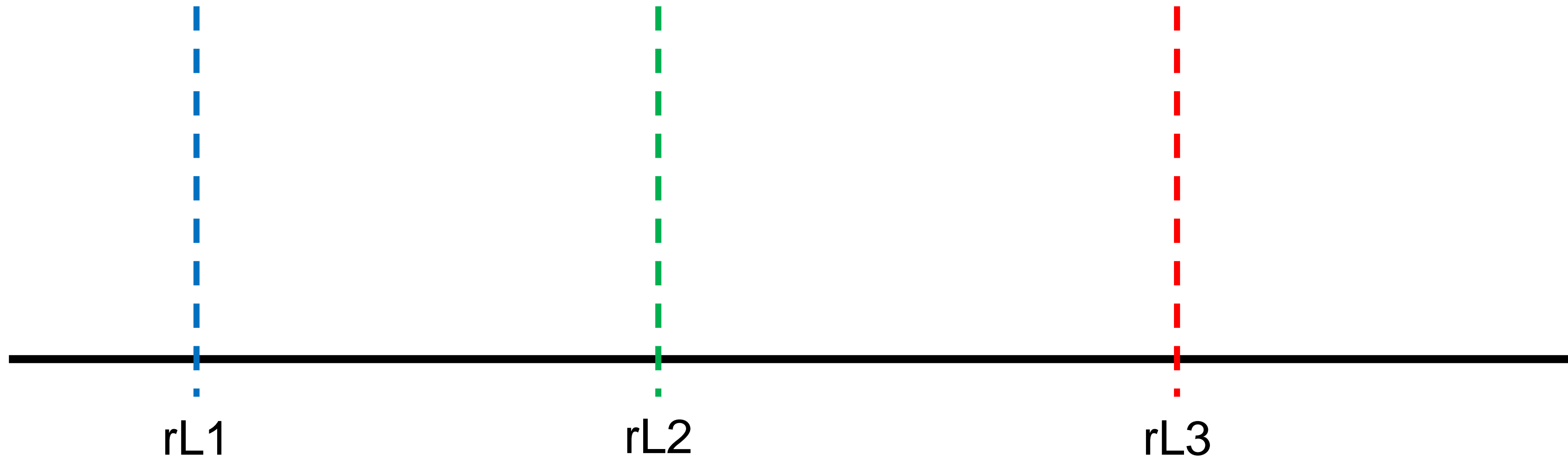
The Technical Part (2)

- set all read levels to minimum threshold



The Technical Part (3)

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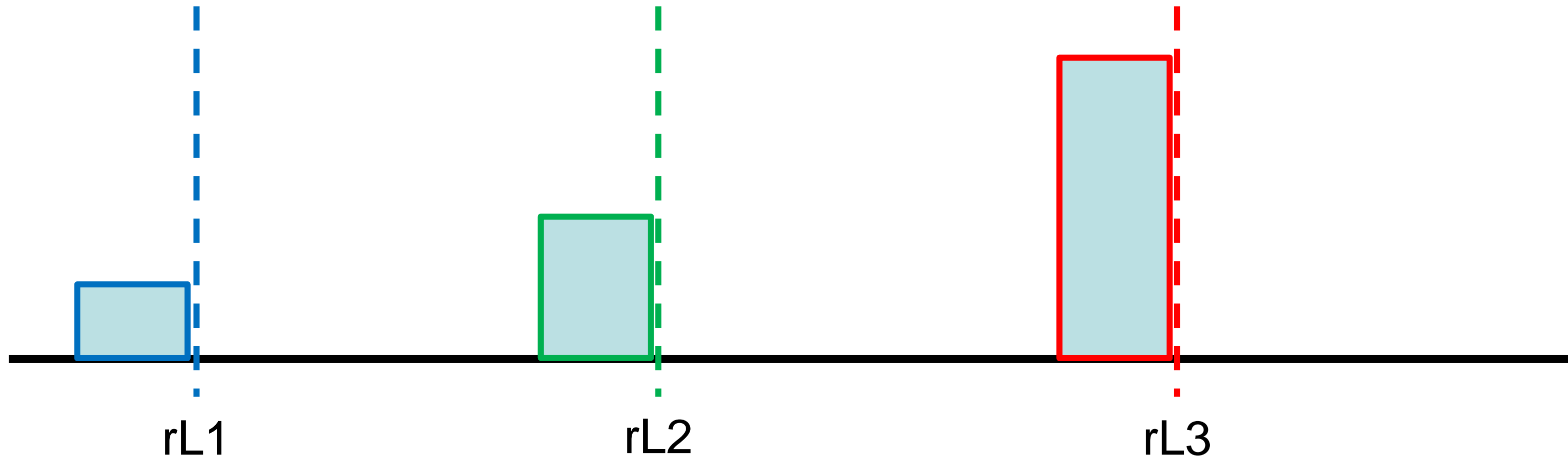
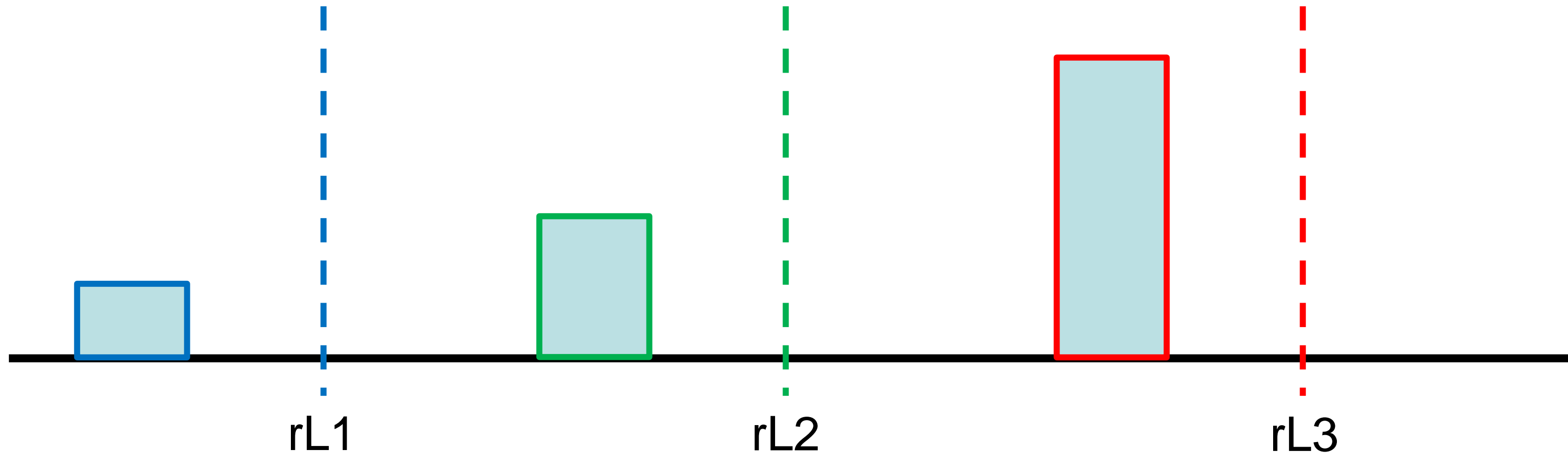
- for each read level, record number of cells below threshold



The Technical Part (4)

- for each read level, increase the threshold by the same amount



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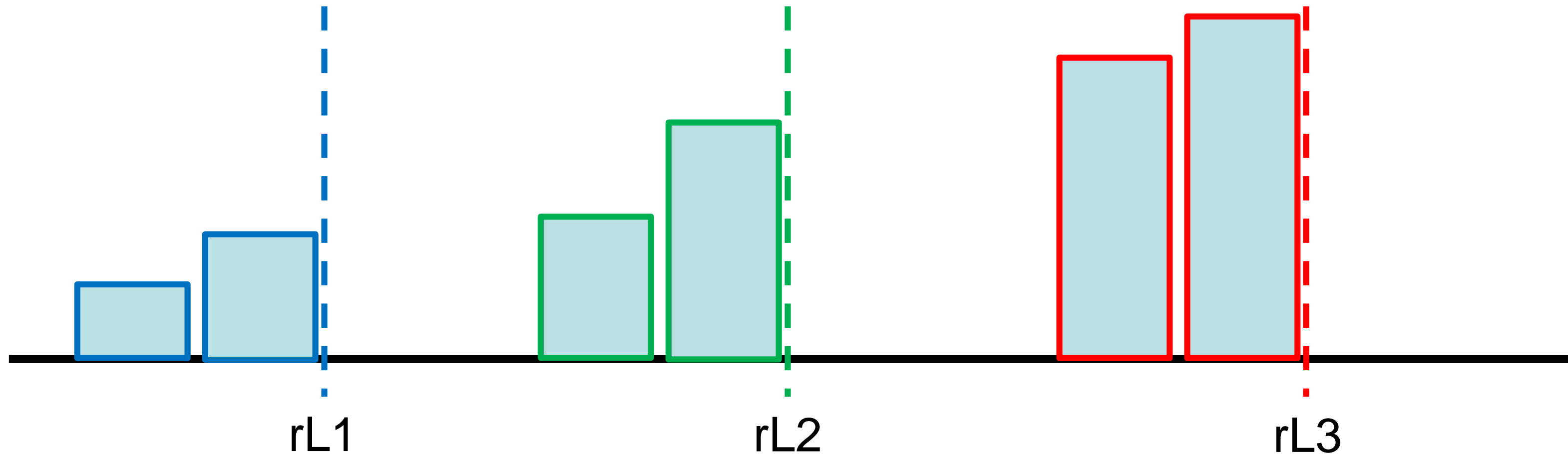
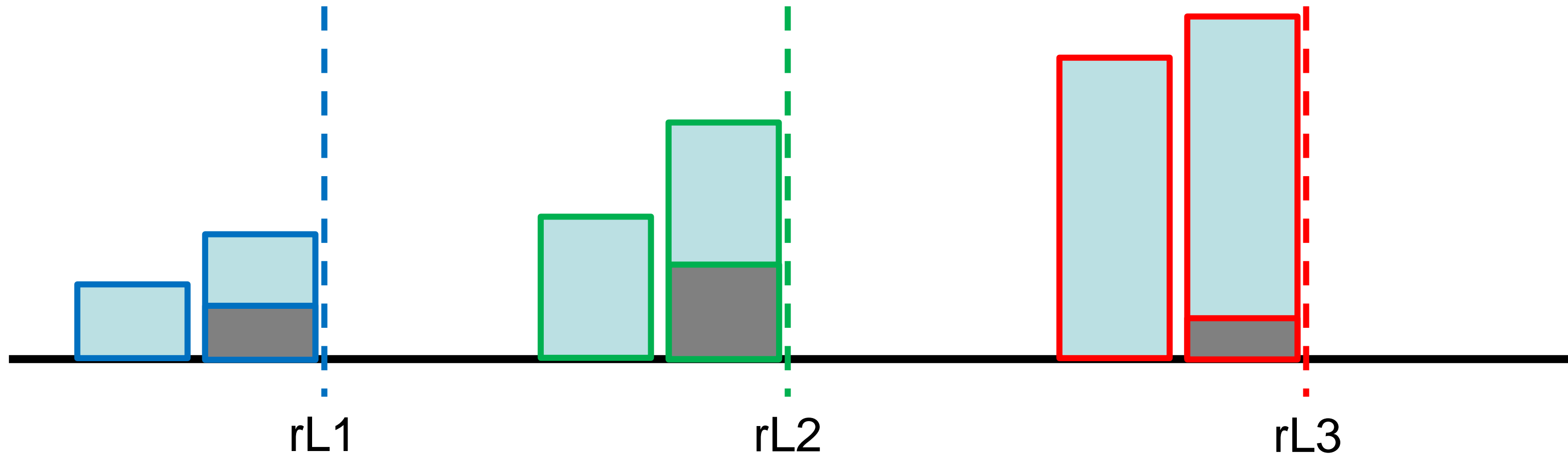
The Technical Part (5)

- for each read level, record number of cells below new threshold



The Technical Part (6)

- for each read level, subtract the previous threshold number from the current



The Technical Part (7)

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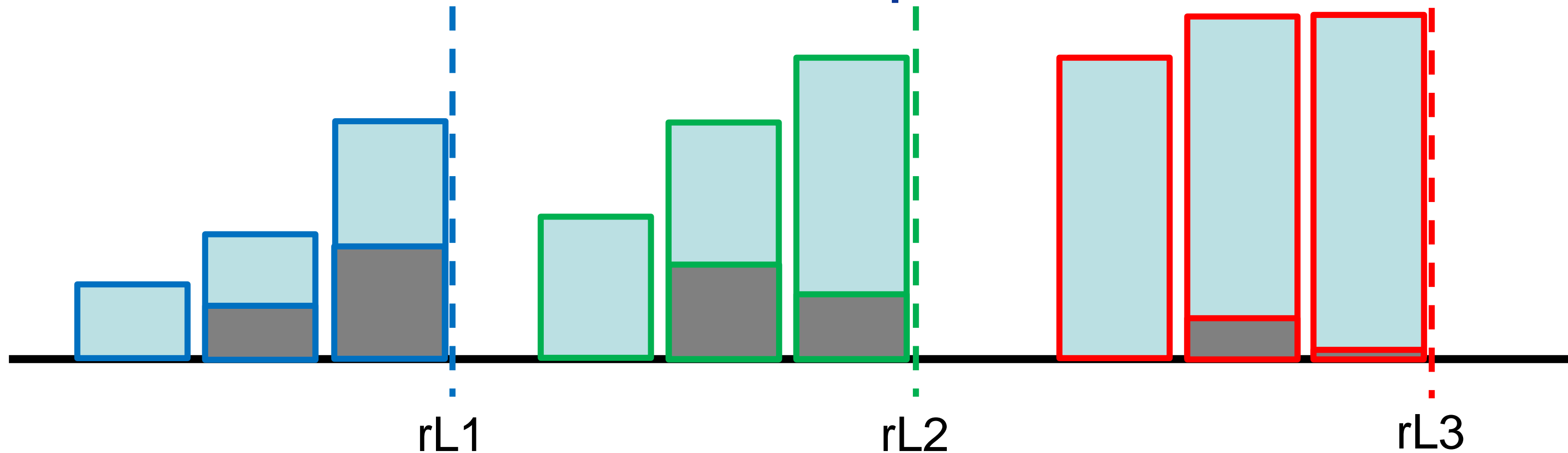
- for each real level, increase the threshold by the same amount and repeat etc…



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The Technical Part (8)

- for each real level, increase the threshold by the same amount and repeat etc…

rL1 rL2 rL3

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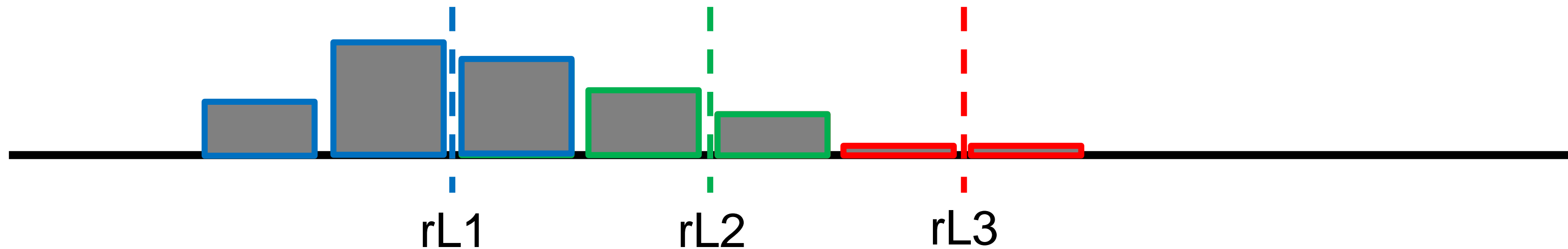
The Technical Part (9)

- stitch together voltage distribution for each read level to get overall distribution
- NOTE: the overlap tells us how far apart each default read level is!!!



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3D TLC NAND Voltage Distribution (Vendor B) - 1500 PE Cycles, 1 Minute @ 30°C

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3D TLC NAND Voltage Distribution (Vendor B) - 1500 PE Cycles, 8 Months @ 30°C

111 011 001 000 010 110 100 101

Probability - $\log_{10}$

0
-1
-2
-3
-4
-5
-6
-7

-32 | 0 | 33 | 65 | 98 | 132 | 170 | 213 | 244

rL1 | rL2 | rL3 | rL4 | rL5 | rL6 | rL7

Threshold Voltage Relative to rL1 (au)

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3D TLC NAND Voltage Distribution (Vendor C) - 1500 PE Cycles, 1 Minute @ 30°C

111 011 001 101 100 000 010 110

Probability - $\log_{10}$

0 -1 -2 -3 -4 -5 -6 -7

-40 0 66 126 185 244 309 370 410

rL1 rL2 rL3 rL4 rL5 rL6 rL7

Threshold Voltage Relative to rL1 (au)

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3D TLC NAND Voltage Distribution (Vendor C) - 1500 PE Cycles, 12 Months @ 30°C

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Wordline RBER (Vendor C) - <100 PE Cycles, 1 Minute at 30°C

Lower Page
Middle Page
Upper Page

RBER - $\log_{10}$

-3.2
-3.4
-3.6
-3.8
-4
-4.2

0 16 32 48 64 80 96 112 128 144 160 176 192 208 224 240 256 272 288 304 320 336 352 368 384 400 416 432 448 464

Wordline Index

SIGLEAD

Wordline RBER (Vendor C) - <100 PE Cycles, 1 Minute at 30°C

Lower Page
Middle Page
Upper Page

RBER - $\log_{10}$

-3.2
-3.4
-3.6
-3.8
-4
-4.2

0 16 32 48 64 80 96 112 128 144 160 176 192 208 224 240 256 272 288 304 320 336 352 368 384 400 416 432 448 464

Wordline Index

notice the grouping of RBER for each layer

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Wordline RBER (Vendor C) - <100 PE Cycles, 1 Minute at 30°C

Lower Page, Middle Page, Upper Page

RBER - $\log_{10}$

-3.2, -3.4, -3.6, -3.8, -4.2

0 16 32 48 64 80 96 112 128 144 160 176 192 208 224 240 256 272 288 304 320 336 352 368 384 400 416 432 448 464

Wordline Index

grouping typically demarked by different RBER behaviour in the 1st wordline of the layer

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What are They Good For?

- optimized read threshold calibration
  - reduce raw bit error rate
    - improves hard ECC correction performance
  - improve quality of soft data (LLR generation)
    - improves soft ECC correction performance
- NAND quality estimation
  - theoretic channel capacity

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Read Voltage Calibration

- minimize cell error rate over all read level configurations
  - for TLC there are 7 read levels, scales badly
- approximate by minimizing error rate at each read level individually
  - low complexity, reasonably accurate in most situations

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3D TLC NAND Voltage Distribution (Vendor B) - 1500 PE Cycles, 8 Months @ 30°C

111 011 001 000 010 110 100 101

Probability - $\log_{10}$

-1
-2
-3
-4
-5
-6
-7

-32
0 rL1
33 rL2
65 rL3
98 rL4
132 rL5
170 rL6
213 rL7

Threshold Voltage Relative to rL1 (au)

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3D TLC NAND Voltage Distribution (Vendor B) - 1500 PE Cycles, 8 Months @ 30°C

- average raw bit error rate drops from $10^{-1.7}$ to $10^{-2.5}$
  - from 1 in 50 to 1 in 320
  - BCH code is still enough!

Want to Learn More?

- visit our booth – 800
  - NAND tester live demonstrations (with 3D NAND)!
  - discussion!
  - and more…!