Flash Memory Summit

Spin Transfer Technologies
An Allied Minds Company

The Engine

SRAM & DRAM Endurance and Speed with STT MRAM

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  - The Performance, Energy and Cost Advantage
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The Leaking Creaking Pyramid (1)

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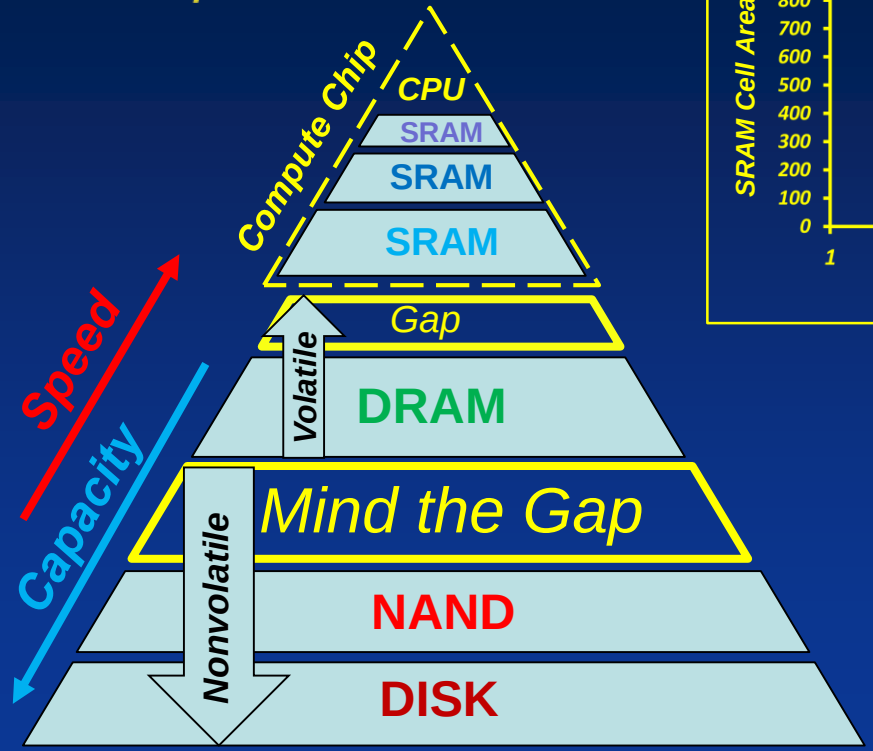

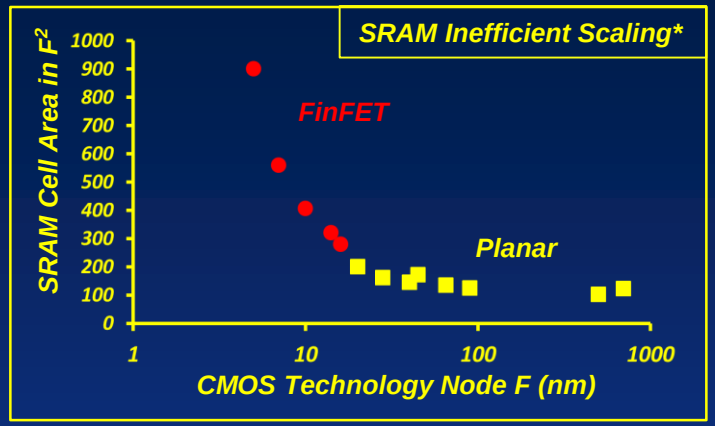

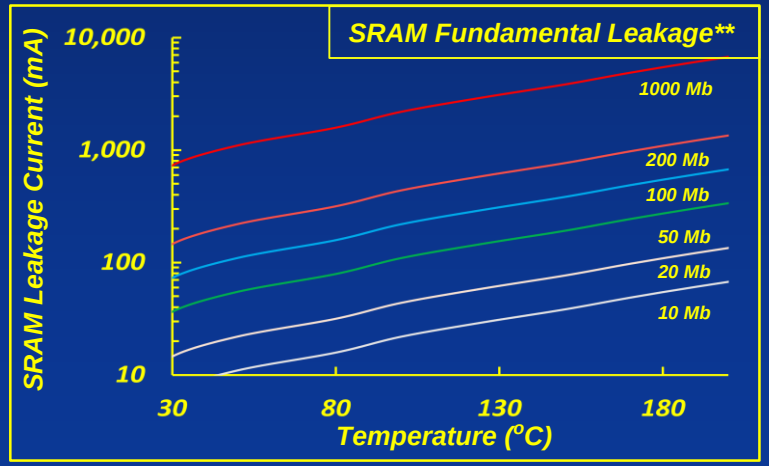

* R. de Werdt et al., IEDM87; R.D.J. Verhaar et al., IEDM90; S.H. Kang et al., IEDM17

** Simulations/estimates from 7nm transistor data in IEDM 2017

The Leaking Creaking Pyramid (2)

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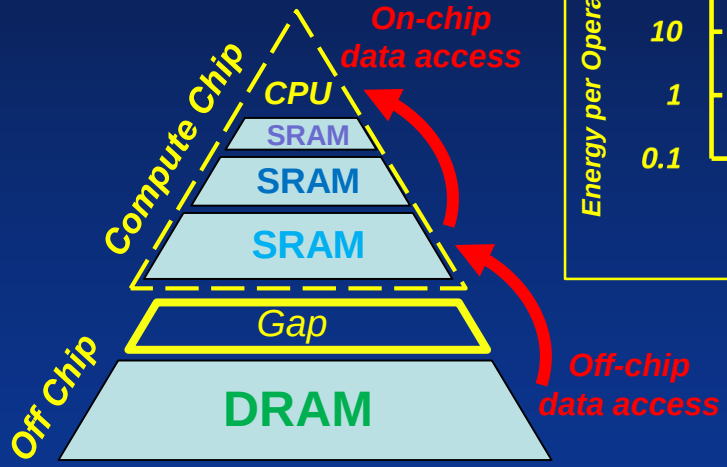

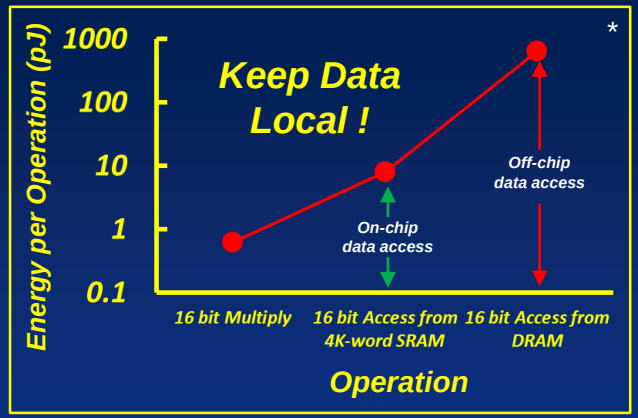

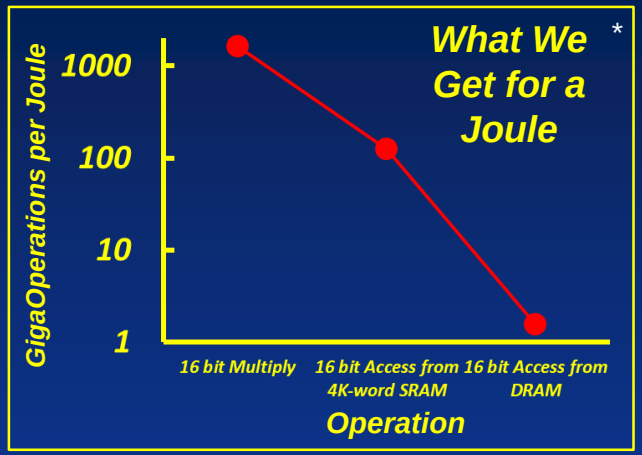

Memory access energy grows as the "length of the wire" *

> 60% of system energy used is in data movements to and from DRAM **

** A. Pedram et al., "Dark Memory and Accelerator-Rich System Optimization in the Dark Silicon Era", IEEE Design & Test, vol.34, April 2017*

*** A. Boroumand et al., "Google Workloads for Consumer Devices: Mitigating Data Movement Bottlenecks", ASPLOS'18, March 2018*

STT-MRAM : A Compelling SRAM Replacement

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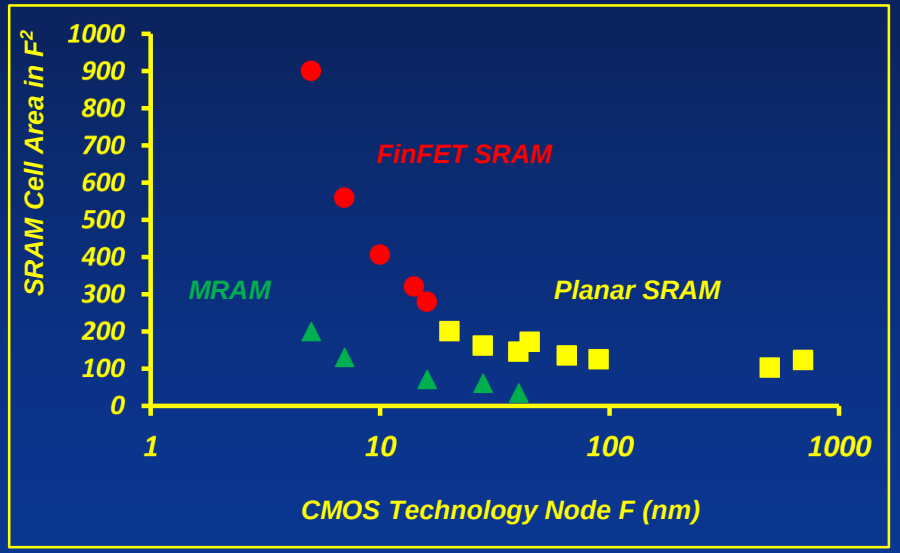
- ✓ ***Size*** : Dramatic bitcell reduction
- ✓ ***Leakage*** : No array leakage
- ✓ ***Persistence*** : Data retained
- ✓ ***On-chip*** : Reduces DRAM accesses
- ✓ ***Rad-Hard***
- ✓ ***But:***
  - Limiting Endurance Conundrum
  - Non-symmetric R/W
  - Disturbs with fast read



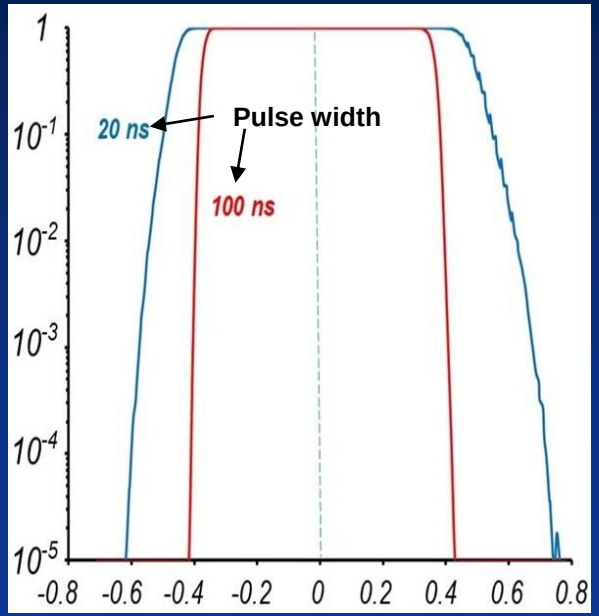
STT-MRAM: A Unique Endurance Conundrum

Magnetic Tunnel Junction (MTJ)

Free layer	↑	*CoFeB*
Tunnel barrier		*MgO*
Reference layer	↑	*CoPt*

- ***Low Write Error Rate needs large tunnel current***
  - *Limits endurance due to oxide wear out mechanism*
- ***High endurance with low Write Error Rate needs reduced tunnel current***
  - *Make Free Layer magnetically less "stiff"*
  - *Reduce MTJ area*
  - *Use special design techniques -* ***The ENGINE***

The Stochastic "Top Hat"



The Physics of the ENGINE

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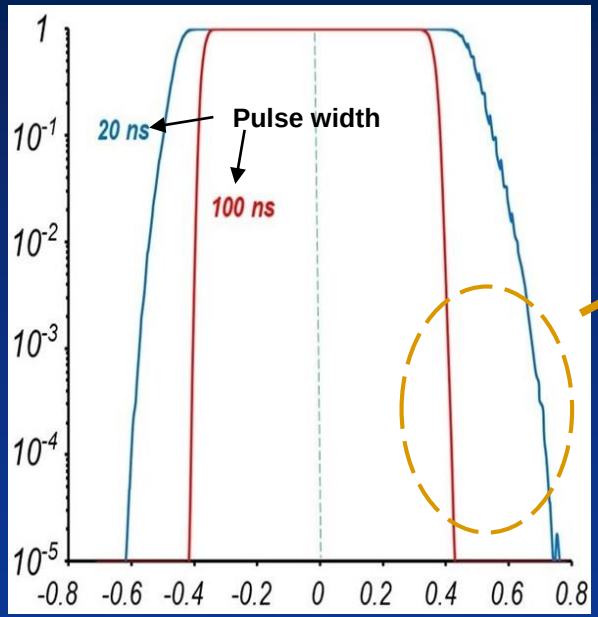
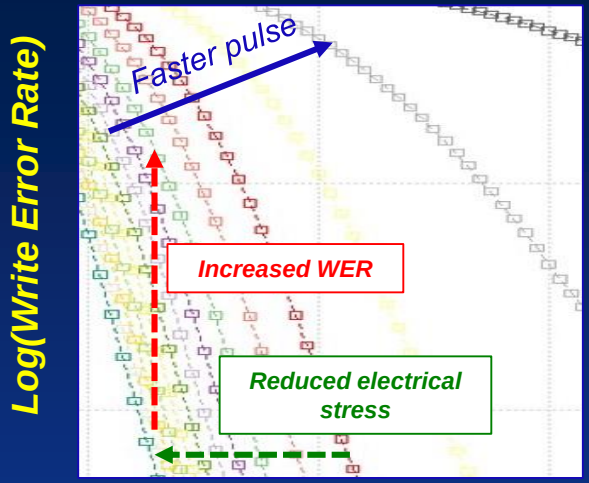
The Stochastic "Top Hat"





Proprietary Circuit Design *allows* ***reduced electrical stress***

- *Results in large endurance increase* ***(~ 6 orders of magnitude)***

Circuit Deals *with resultant* ***Write Error Rate increase***

- *Managed transparently to the user*
- *No change in latency*
- *Allows for faster pulses at high endurance*

ENGINE Emulation

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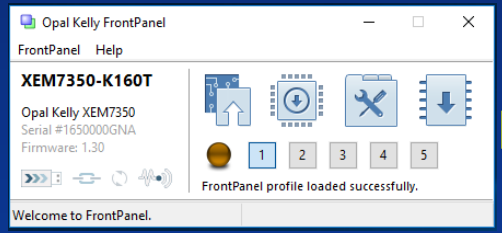
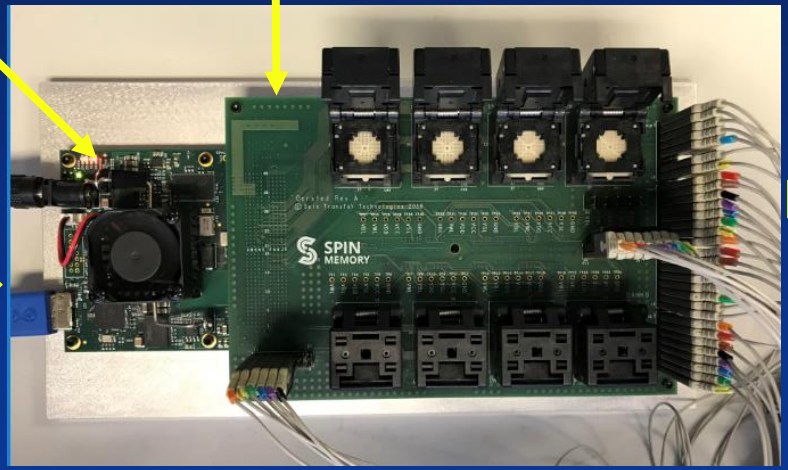
Emulation Board
(FPGA emulation of Engine)

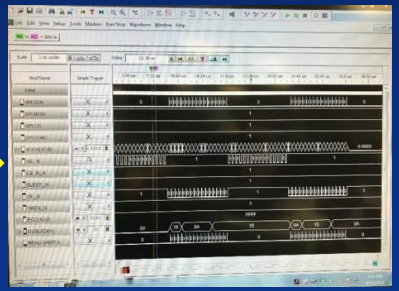
Front Panel
(Control timing, address, patterns, W/R ops etc.)



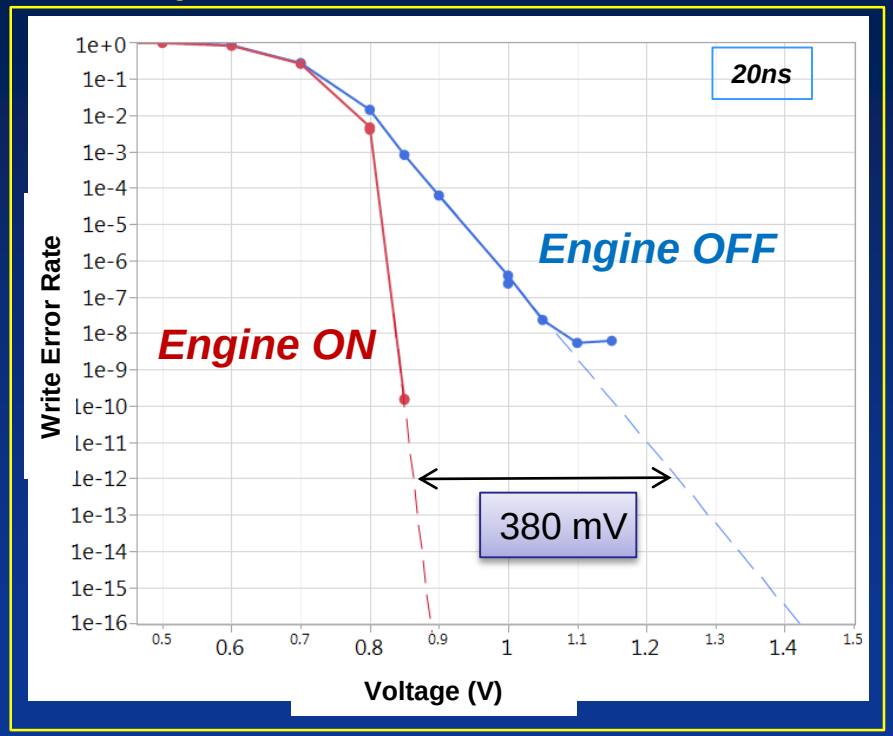
Daughter Board
(Contains SPIN's own 4Mb STT-MRAMs)

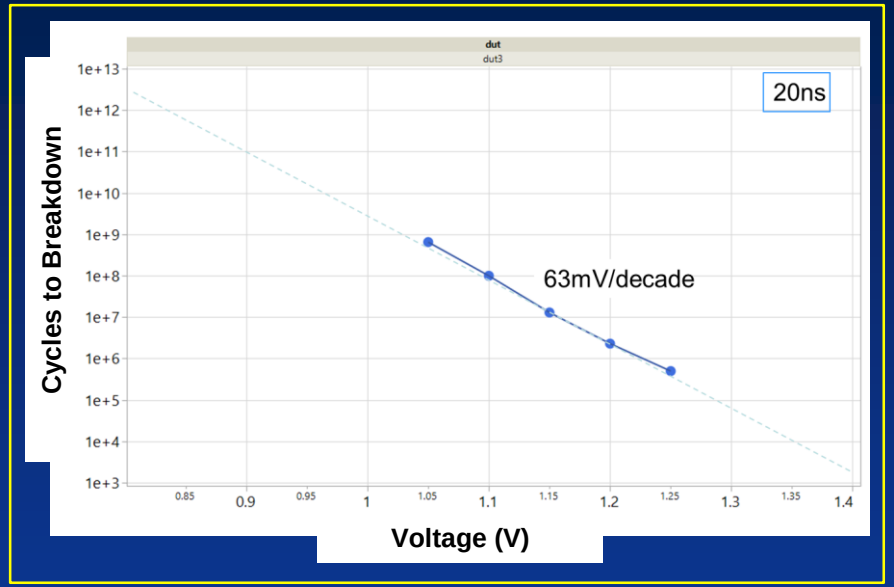


Logic Analyzer
(Verify addresses, timing, patterns, W/R etc.)



Data from Emulated ENGINE





~ 6 orders of magnitude endurance boost

ENGINE Benefits – Takes MRAM Mainstream!

- SRAM/DRAM-like Endurance
  - ~ 6 orders of magnitude improvement with circuitry alone
- Symmetric R/W
  - 10ns capable
- Random R/W
  - Looks and feels like an SRAM
- Corrects Read Disturbs allowing Fast Reads
- No user visible errors

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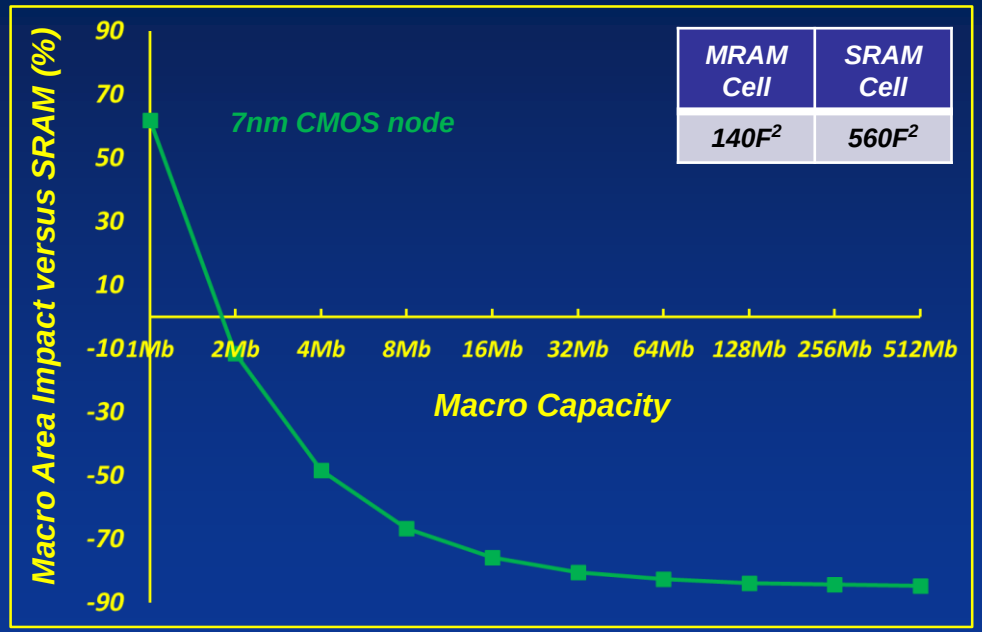
The Performance, Energy and Cost Advantage



- Dramatic area impact
- Maximize large on-chip cache and memory capacity
- Allows persistence on-chip
- Reduces DRAM accesses
- ~ Zero array leakage
- Symmetric Read/Write

Conclusions

- The ENGINE takes MRAM into the mainstream
- Provides a path for MRAM as SRAM/DRAM replacement
- Uses evolving ecosystem for embedded NV MRAM as a foundation
- Combines low Write Error Rates with SRAM/DRAM-like endurance resulting in zero user-visible errors
- Achieves fast and symmetric read and write
- Makes MRAM the most likely candidate for SRAM replacement and, eventually, DRAM