

FPGA Based PCI Express Gen4 NVMe SSD Platform

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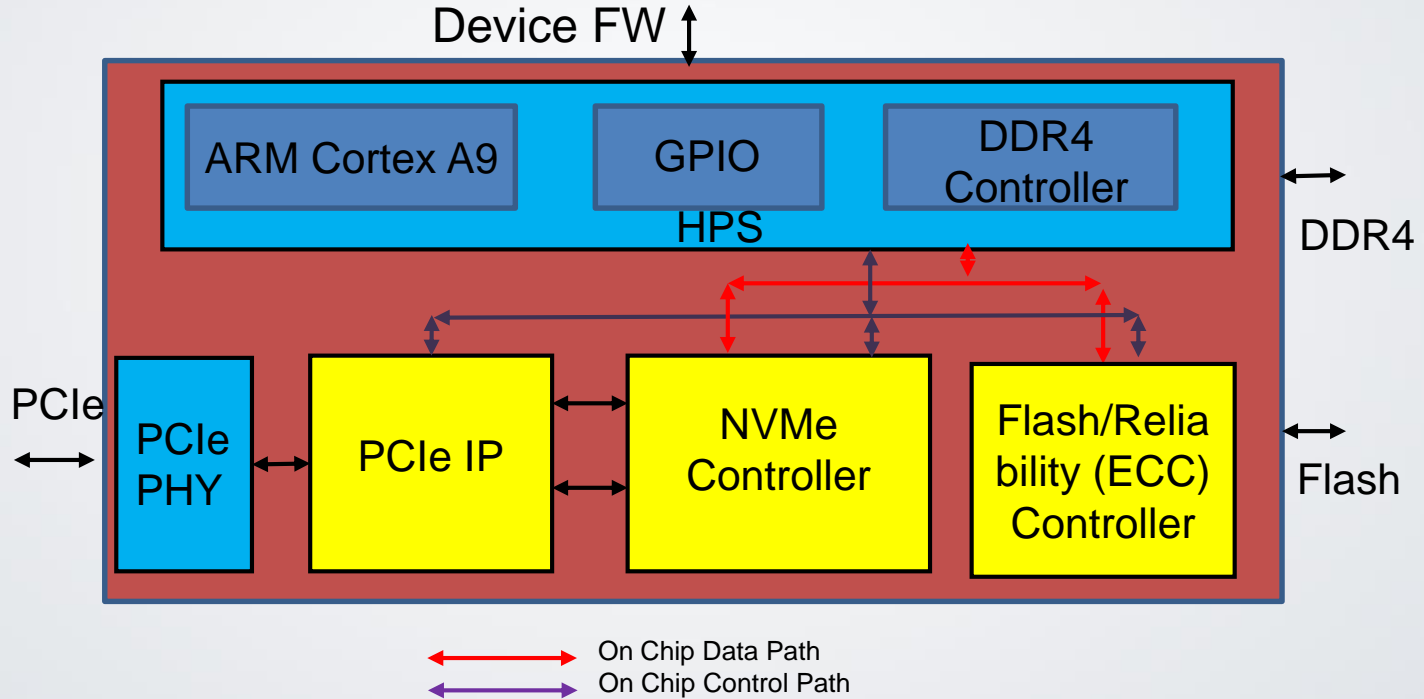
“The IP enabled solutions provider”

AGENDA

- **FPGA Based PCI Express Gen4 NVMe SSDC**
- **Design Challenges**
- **Configurable IP Components**
- **Mobiveil PCI Express Gen4 NVMe SSD Platform**
- **Summary**

FPGA Based PCI Express Gen4 NVMe SSDC Platform

FPGA Based PCI Express Gen4 NVMe SSDC Platform



Design Challenges

- Reference Design should be flexible to support different hardware configurations
- Reference Design should be able to handle various target technologies
 - It should be able to handle performance targets across technologies
- Reference Design should allow customization for individual implementations
- Reference Design should provide hooks for Statistics gathering, Error recovery, Reclaim and other value added Enterprise SSD functions
- *Design Reuse* is Critical

Feature Configurability

PCIe

- Number of Virtual Channels
- SRIOV Needed
- Bifurcation Support
- DMA Needed
- INT/MSI/MSIX Support
- SRNS/SRIS

ECC

- BCH/LDPC
- Code Rate
- Programmable Padding/Puncturing
- User Defined LDPC Matrix
- Single/Dual Core
- Soft Read Procedure



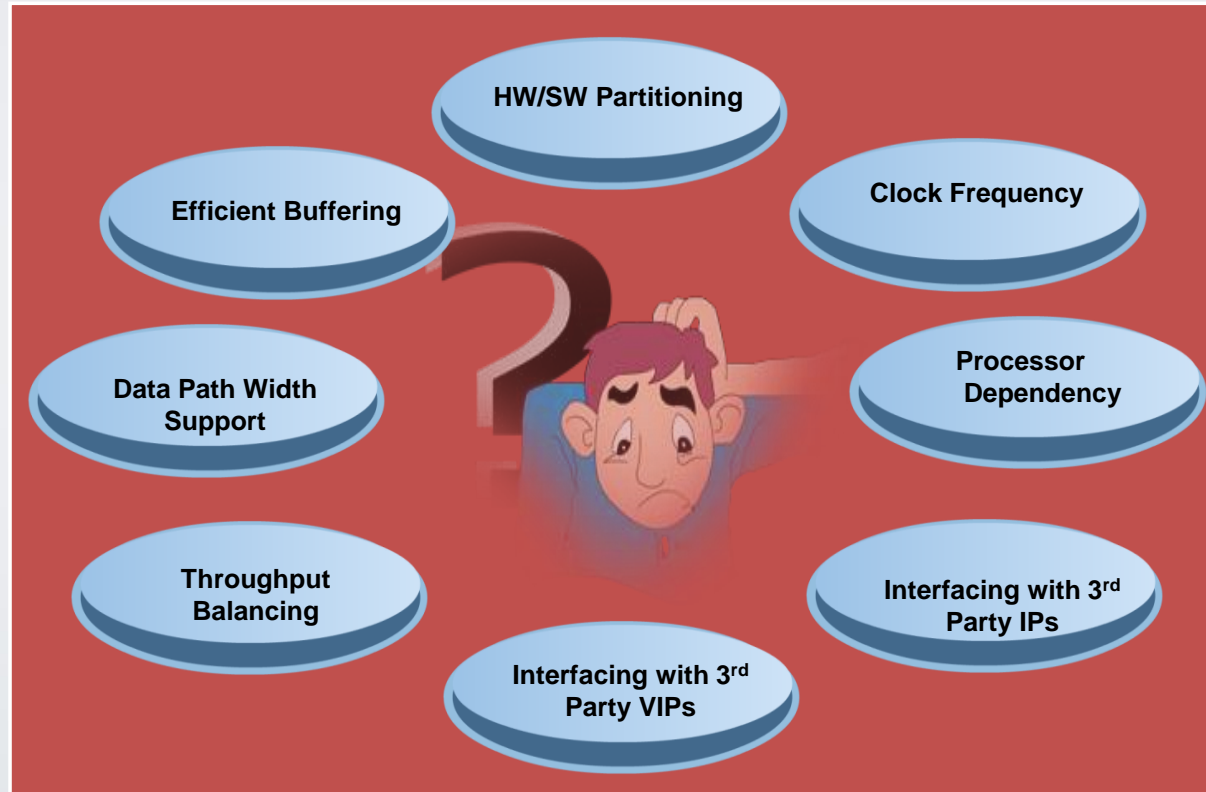
NVMe

- Multipath IO Support
- LBA Size
- Number of IO Queues
- Vendor Command Support
- Optional Feature Support
- Vendor specific Arbitration

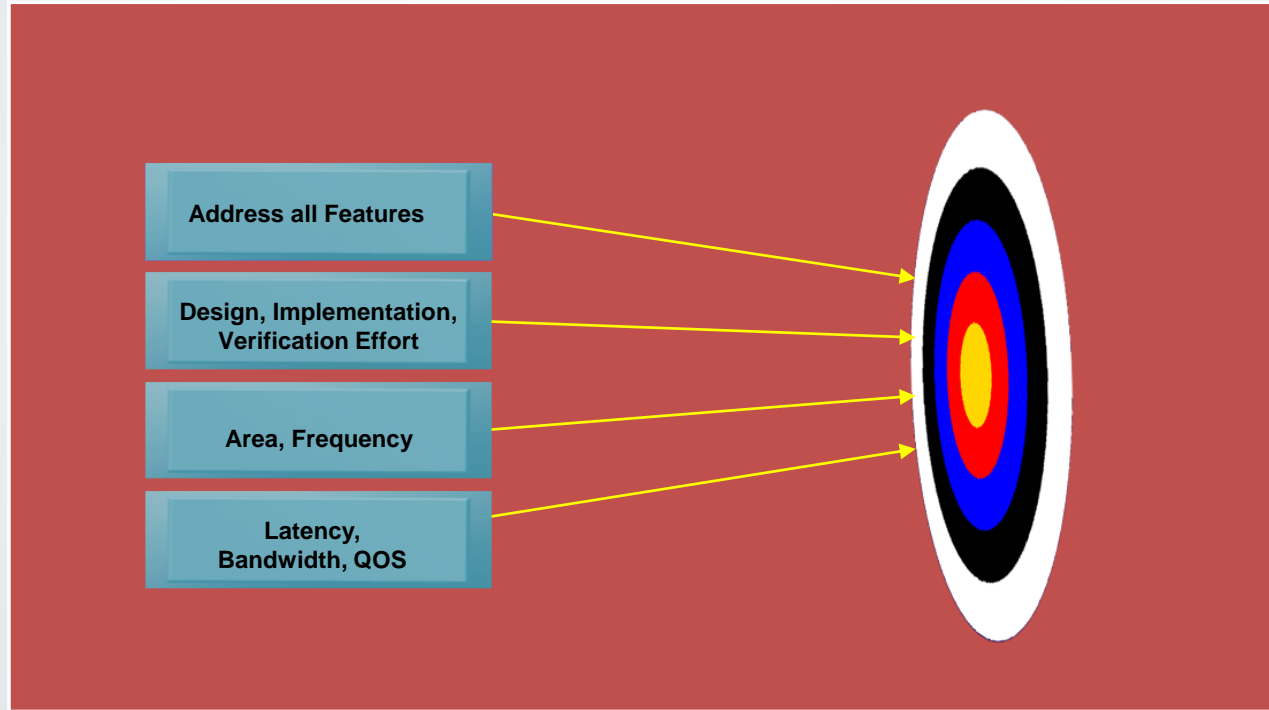
Flash Controller

- ONFI/Toggle IF
- Full Rate/Half rate/Quarter Rate Support
- Custom Command Support
- Number of LUNs
- Command Arbitration LUN Based
- Suspend/Resume Support

Implementation Challenges



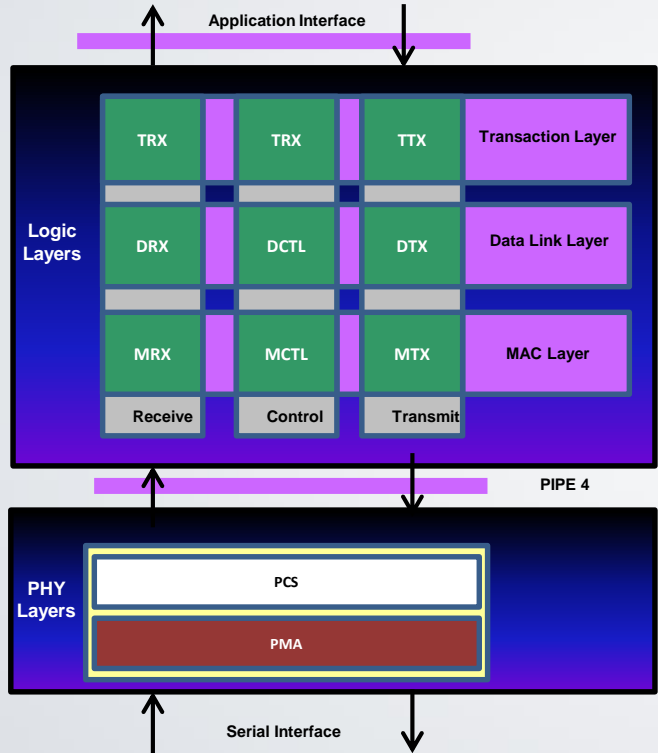
Configurable IP Blocks



Configurable IP Components

PCI Express Controller (GPEX)

PCI Express (GPEX)



Compliant to PCI Express Base 4.0

- PCISIG Certified IP
- Supports Gen4, Gen3, Gen2 and Gen1 rates
- Compliant to PIPE 4.3 specification
- Supports x1, x2, x4, x8 and x16 lanes
- Supports INTR, MSI, MSIX
- 32, 64, 128, 256 and 512 Bit Data path support
- Supports 8, 16, 32 and 64 bit PIPE

Optional Feature Support

- SR-IOV
- ATS
- ARI
- FLR
- LTR
- SRIS

Provides PCS

Advanced Power Management

- ASPM L1, Auxiliary power, beacon
- Clock and Power Gating
- L1 PM Substate

Value Added Features

- End to End Data parity protection
- Device specific control and status Registers, Loopback and test features
- Supports up to 8 virtual channels and traffic classes
- Supports isochronous transfer
- Supports RR, WRR and strict priority VC arbitration scheme
- Infinite credit option for selected types of traffic
- Supports all in-band messages including vendor defined message and broadcast message

LDPC Encoder/Decoder

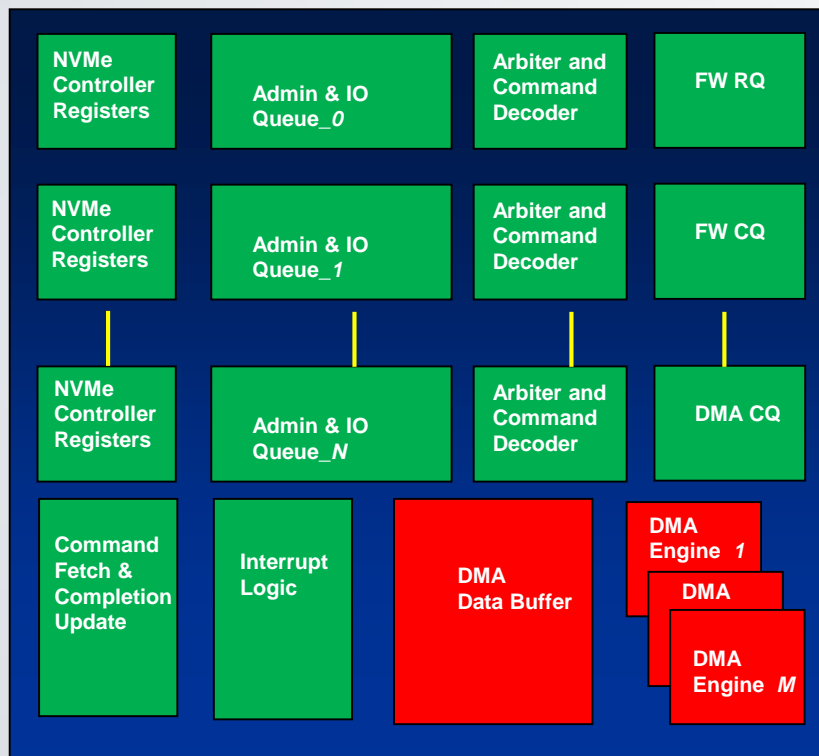
LDPC Encoder/Decoder

- LDPC scalable IP
 - Supporting wide range of data-rates
 - 50MB/s to 4.0GB/s for a single LDPC instance
 - Major scalability parameters are (before IP instantiation):
 - Codeword size (0.5KB vs. 1KB vs. 2KB, 4KB or 8KB)
 - Maximum amount of supported parity
 - Several parameters for degree of parallelism
 - Memory access options
 - IP Core Programmability Parameters (after IP instantiation):
 - Simultaneous support for different amounts of parity
 - Simultaneous support for several LDPC codes
 - On-the-fly switching from one LDPC code to another
 - User can program its own LDPC code/Matrix
- Lowest power LDPC decoder
 - Code word size is 1KB+parity
 - Total power is measured for TT, 0.9V, 25C
 - TSMC 28 HPC process

Throughput @ EOL (MBPS)	Freq (MHz)	Cell Area (um2)	Memory (KB)	Power	
				Dynamic (mW)	Leakage (mW)
405	500	55,247	58	27.65	0.027
1183	500	127,880	57	66.79	0.059
1581	500	137,183	36	78.94	0.063
2214	700	135,604	57	102.82	0.206

UnH Certified NVM Express Controller IP
(UNEX)

NVM Express (UNEX) Controller



Compliant to NVM Express 1.3a specification

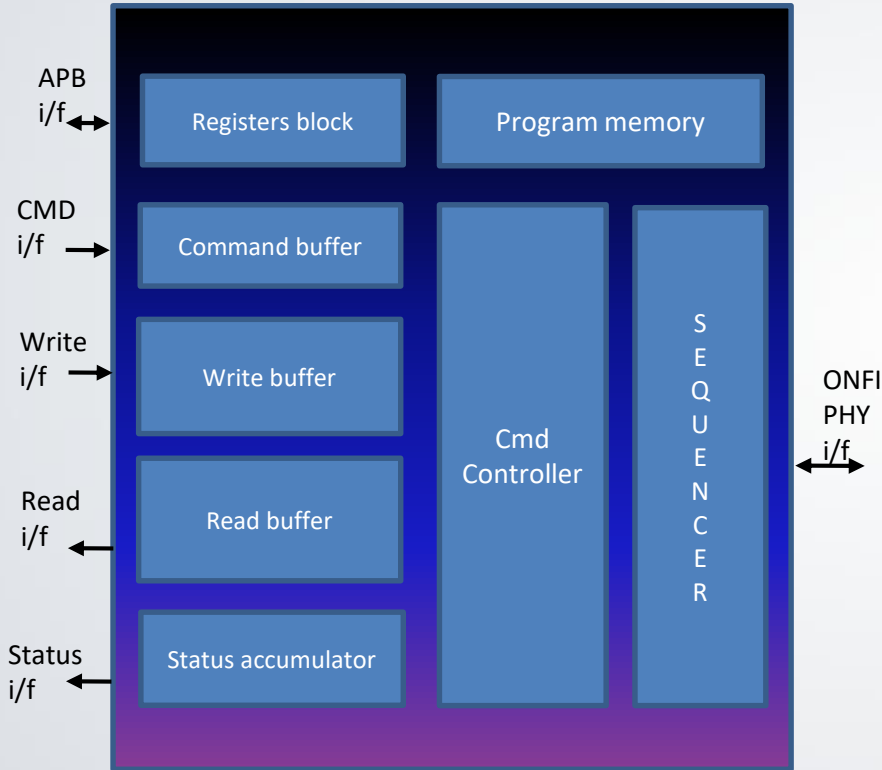
- UnH Certified IP
- Supports Multi-Port Controller for Multi-path IO Support
- Supports configurable number of IO Queues
- Supports configurable Queue depth
- Supports Round Robin or Weighted Round Robin with Urgent Priority arbitration mechanism
- Host memory page size support of 128MB
- Efficient and Streamlined Command handling
- Supports Fused Operations
- Supports All Optional Admin Commands

Value Added Features

- Supports All Optional NVM Commands
- Supports Multi-Path IO and Namespace Sharing capabilities
- Supports Reservations
- Supports multiple name spaces
- Optional AXI interfaces for NVMe implementation in SoC
- Well defined Command Interface for local CPU to perform subsystem initialization and to handle all non-hardware accelerated commands

Enterprise Flash Controller

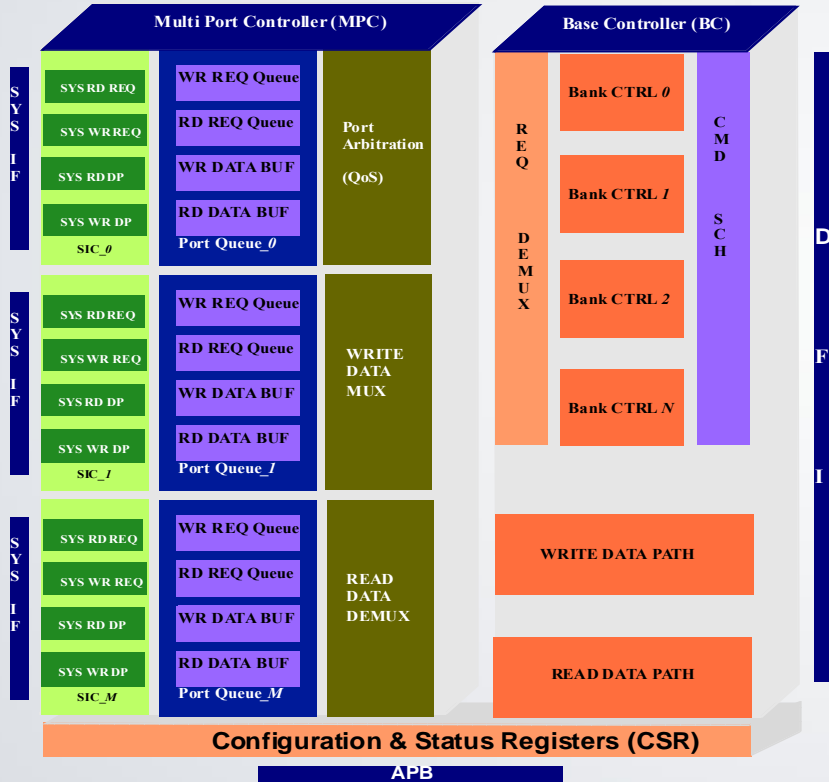
Enterprise Flash Controller



- Supports NAND interface standards such as ONFI and Toggle
- Supports LUN based CMD arbitration to maximize parallel execution
- Supports suspend/resume commands per LUN for executing software overridden priority IO commands.
- Programmable command sequences
- Supports up to 64 LUNs per channel
- Supports following modes
 - 1:1 (Full-rate Mode)
 - 1:2 (Half-rate Mode)
 - 1:4 (Quarter rate Mode)
- Supports data path width upto 256 bits on user interface
- Supports software based programming of commands
- Supports programming custom command definitions
- Supports randomization requirements
- Supports integration of per channel ECC.

UMMC Memory Controller

UMMC Memory Controller

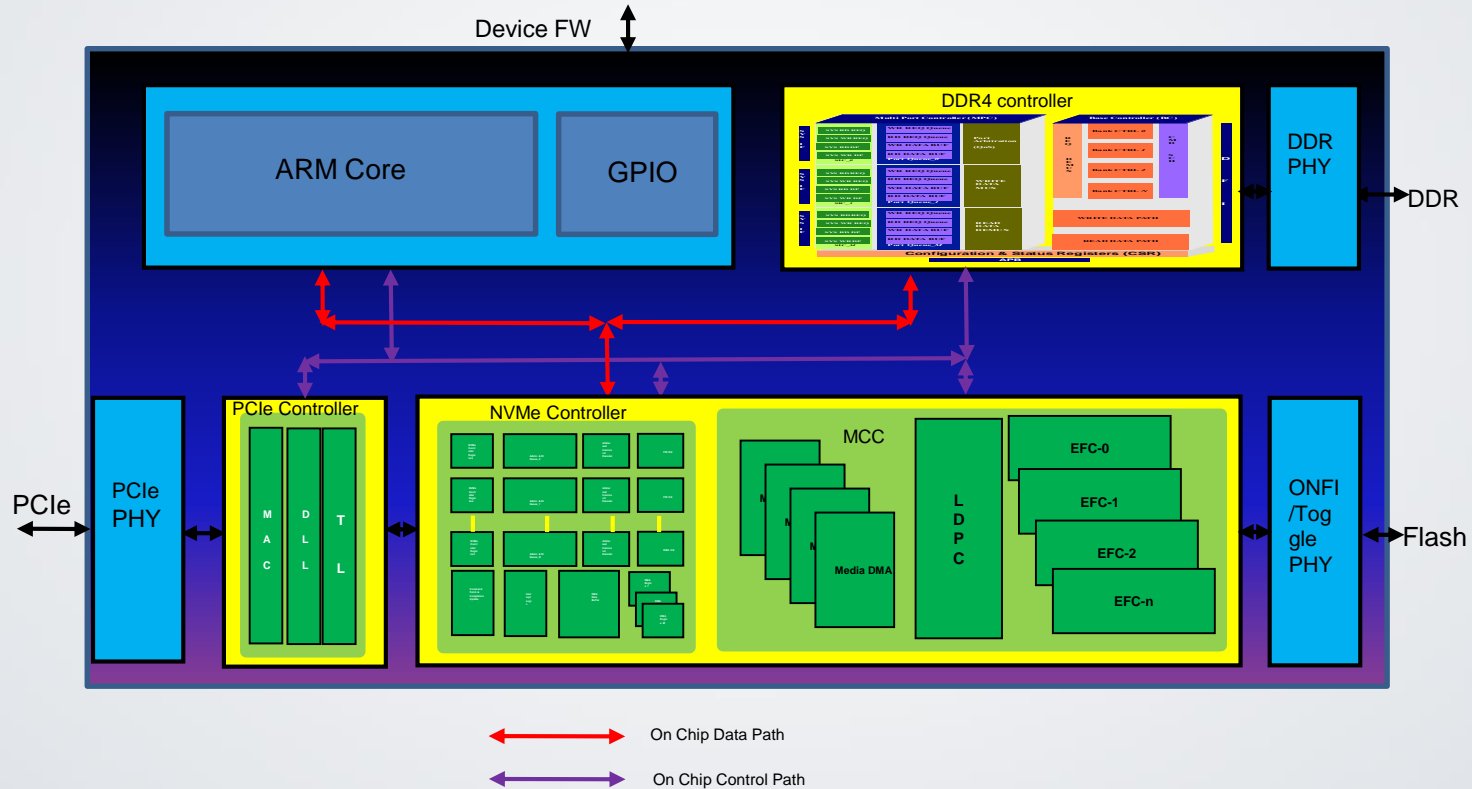


Compliant to AXI4 and DFI3.1

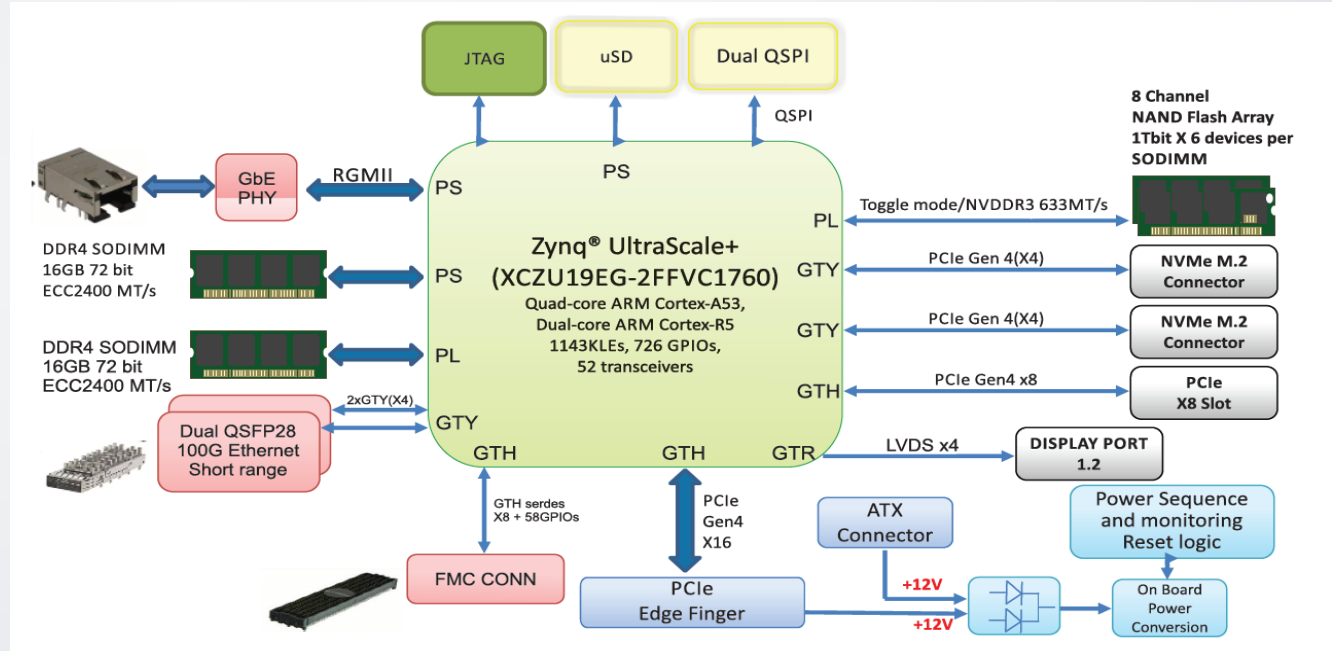
- Supports all major memory standards – DDR3, DDR4, LPDDR2, LPDDR3, HBM2
- Supports Multiport Configuration
- Supports QoS through various arbitration schemes
- Configurable and programmable address mapping
- Supports up to 4 ranks
- Supports following BC Clock to PHY Clock ratio
 - 1:1 (Full-rate Mode)
 - 1:2 (Half-rate Mode)
 - 1:4 (Quarter rate Mode)
- Supports Burst Length 4, 8, 16
- Supports Active/Precharge Power down
- Supports ECC Checking and Correction
- Supports Inline ECC

Mobiveil PCI Express Gen4 NVMe SSDC Platform

Mobiveil PCI Express Gen4 NVMe SSDC Platform



Mobiveil PCIe Gen4 Configurable NVMe SSDC Platform



Unique Subsystem Development Solution

- **Provides Full NVMe Based Reference Design Using Mobiveil's Controllers**
 - **PCIe Gen4.0 PCIe Controller (GPEX)**
 - **Multiport NVMe (UNEX)**
 - **LDPC**
 - **Enterprise Flash Controller (EFC)**
 - **UMMC**
 - **Media Control Cluster**
- **Reference FW is also provided**
- **Allows various Flash parts to be used**
- **Customer can add their custom value add in SW or HW**

The Mobiveil Team

Vision

Provide Technology, Platform and value added services to develop storage solutions

- RTL IP
- FPGA Platform
- Engineering services for Custom Designs

Leadership

Management with 30+ years experience in Semiconductor/ Silicon IP/ Product Engineering Services

Team working together developing Silicon IP & Engineering Services for 15+ years

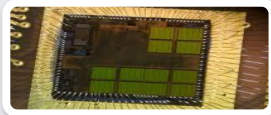
Previously founded GDA (1997) developed several IP blocks

6 Patents in Flash Storage and Reliability

Location : Headquarters in Milpitas, Engineering Centers in Chennai, Bangalore and Hyderabad. Total headcount ~180



Mobiveil IP Advantages



Market leading & most exhaustively proven cores in the market:
Industry leaders are using these cores



Consortium Participation : *RIO – Member, PCISIG – Member, HMC – Member*



Superior Technical Solution: *Most Feature rich IP, Complete Customization and delivery Solution*



Support: *Clear IP Focus & Worldwide Support*



3rd Party Partnerships for complete Solution: *(Verification and PHY IPs)*



Standard Body Certified Cores: *All Mobiveil IPs are validated and certified: PCI Plug fest, UNH, RTA*

Thank you.

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