Flash Memory Summit

A New Erasure Pointer Generation Scheme for Storage Class Memory

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Topics

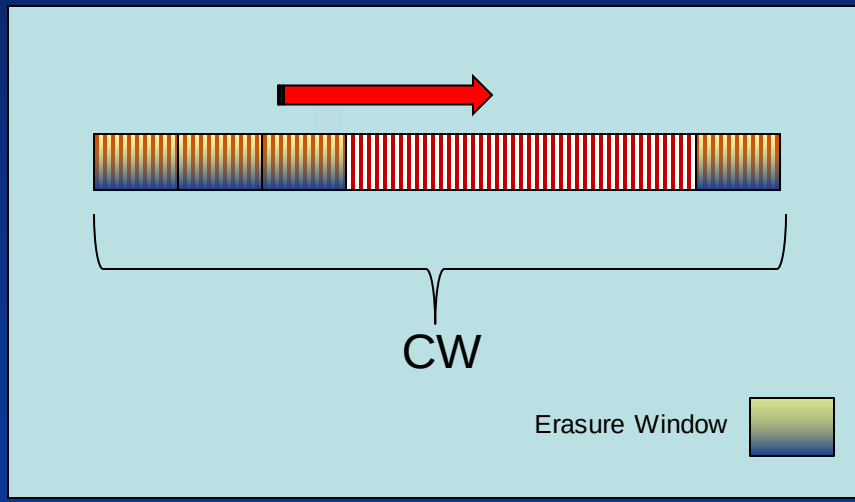
- Erasure
- Soft Erasure Concept for SCM
- SFR Gains w/ Soft Erasure
- Conclusion

Introduction

- Erasures are known bit locations with unreliable information
- ECC decoding power: Constructed using 2 degrees of freedom:
  - # of Errors
  - Locations
- Deployed with multiple ECC codes
- SFR Gain: ECC correction could double if erasure locations are identified
- Implementation Flexibility: HW or SW schemes can be used to identify erasure locations (erasure pointers)

Erasure Pointer Generation Methodologies

- Erasure pointers could be generated by either hardware and/or software (hard vs soft).
- In software, an iterative process is employed where a series of locations are marked as erasure by what is commonly referred to as Erasure window (EW).
  - Helpful mainly with burst defects

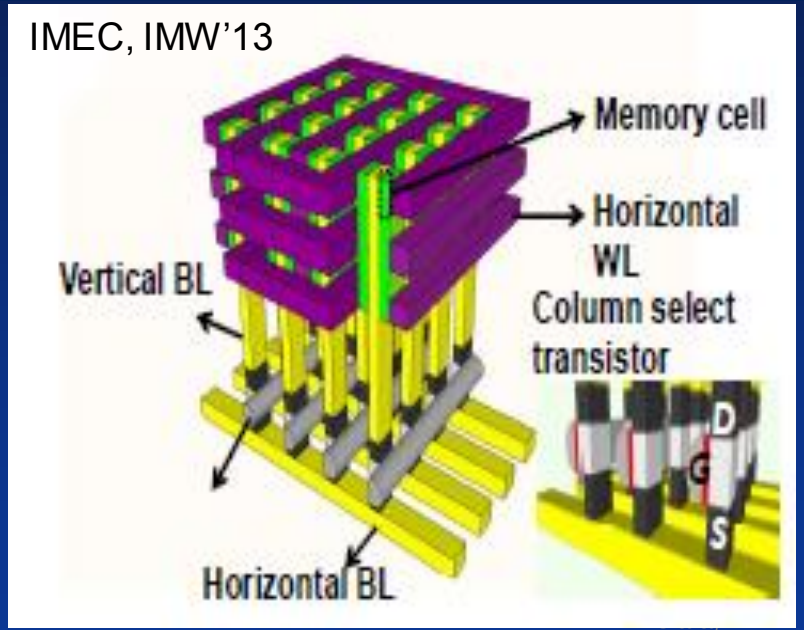


Erasure Application in SCM

- Emerging SCM (like ReRAM, PCM and MRAM) are NVM with high endurance, low latency and data persistency attributes
- SCM is byte addressable and performs write-in-place
  - No erase is needed and no garbage collection step
- This feature enables refreshing data-in-place and checking for defected/slow bits

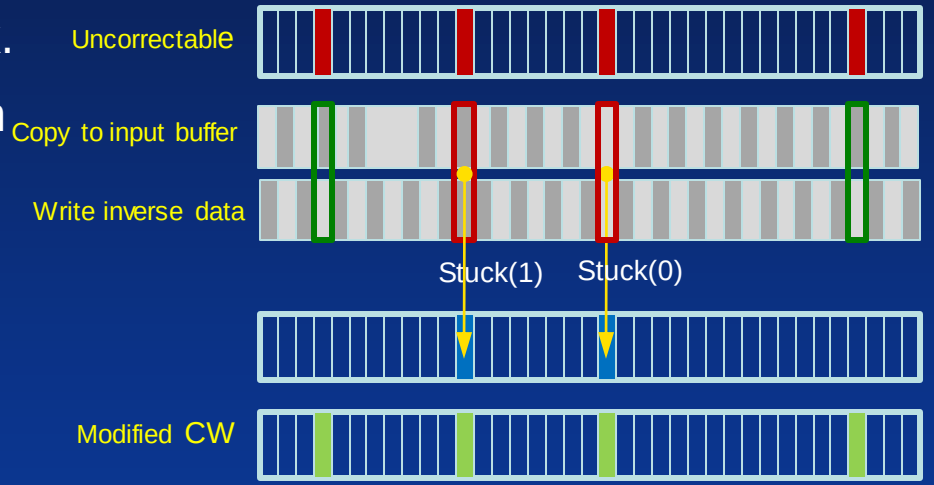
Erasure Pointers Through Short Detectionn

- SCM could utilize the device ucontroller to identify defects (BL-BL short)
- Column addresses serve as erasure pointers to the defected locations within the CW.
- Those locations/pointers could be transported through an erasure dedicated bus to the decoder



Soft Erasure: Basic concept

- Scheme for SCM utilizes write verify feature..
- Write in place and perform a read back.
- Log the errored column locations within the code word (CW)/page in the Error Register (ER).
- Random errors due to loss of endurance and/or retention will not repeat.
- Defects will fail to verify.
- ER will serve as erasure pointer buffer.



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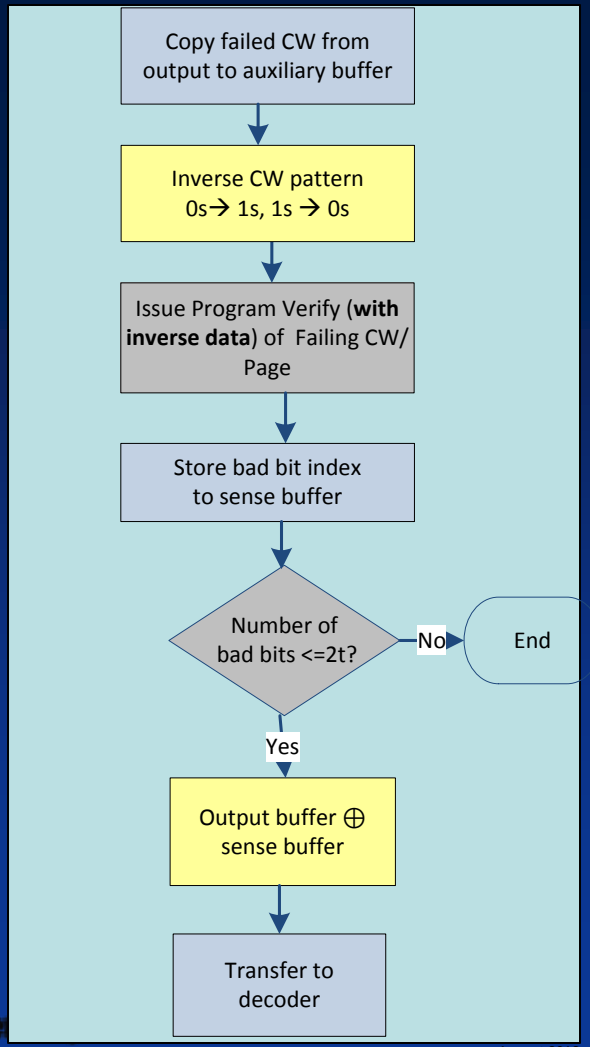
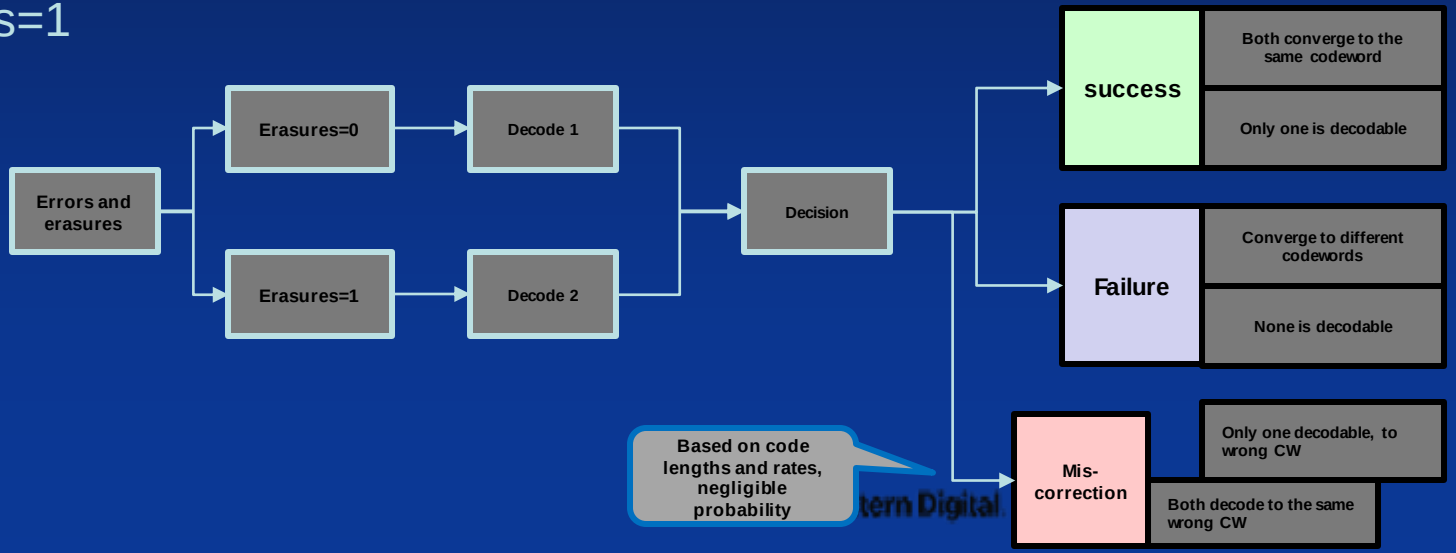
Soft Erasure details

1. Copy of the failed data → auxiliary buffer.
2. Inverse the failed; write verify
3. Bits failed miscompare → erasure pointers
4. Transfer the original data from the auxiliary buffer and erasure pointers to the decoder.
5. Or flip the locations of the bits that failed miscompare, send the modified data back to the decoder.



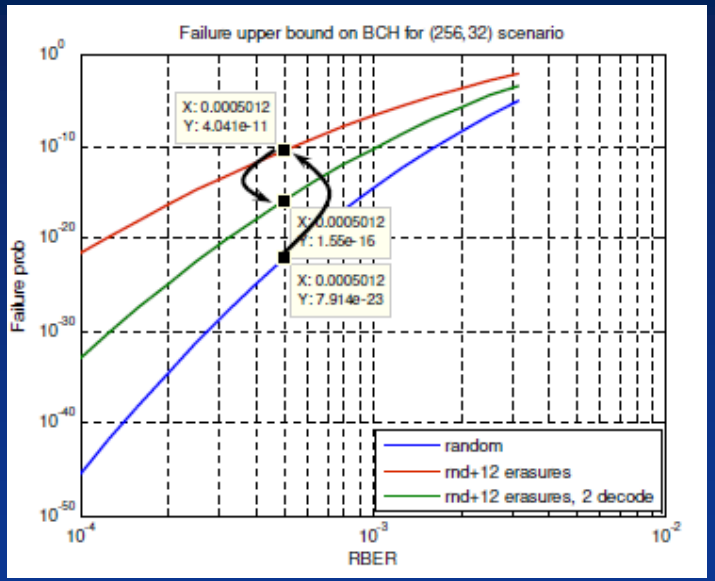
Erasures Modelling

- Some of the error locations are marked as erasure in addition to existing random errors.
  - i.e., overall error rate is increased
- To decode, two different scenarios were examined: all erasures=0 and all erasures=1



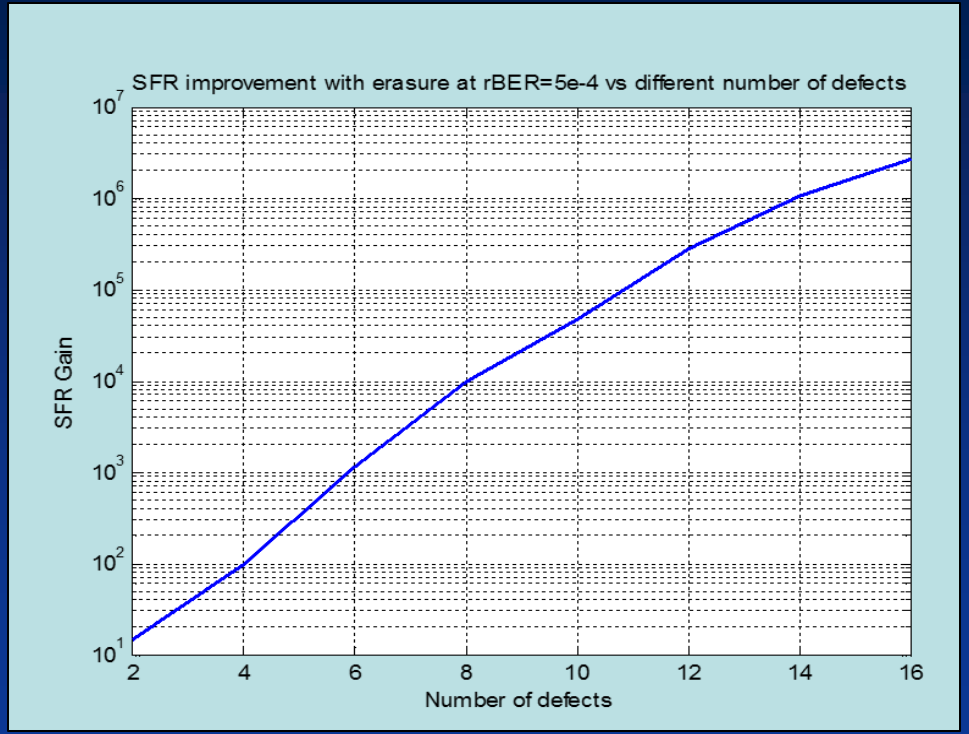
SFR Gain with Erasure

- Example BCH 288B CW (32B parity)
- At RBER of 5e-4 SFR is 8e-23
- Introducing 12 additional errors will degrade SFR by 7 decades.
- Effective Gain: Adding 12 erasures will improve SFR by 3 decades.



SFR Gain Vs. Erasure Count

- On a log scale, SFR gain is ~ linearly proportional to number of erasures.



Erasure-Managed Failure Modes

Category	Failure Cause	Management
Defects	Hard Defects (stuck bits or data line shorting)	**Erasure feature**
Multiple CW Failures	Correlated CW failure or EOL degradation	Iterative RAID and inner code+ **Erasure**

Concluding Remarks

- We developed an erasure pointer generation scheme for SCM applications that can be applied with multiple ECC engines.
- Correction capability gains: Potential to double the ECC max correction capability provided no other random errors exists in the CW.
- Implementation Flexibility: Deployment of Erasure algorithm can be achieved with dedicated ECC hardware or Software-only methods where the defect locations are flipped in buffer prior to decoding.