



Flash Memory Summit

Adapting Controllers for STT-MRAM

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CTRL 301-1 Flash Controller Design Options

Room: GAMR2 8:30 – 10:50AM

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Adapting Controllers for STT-MRAM

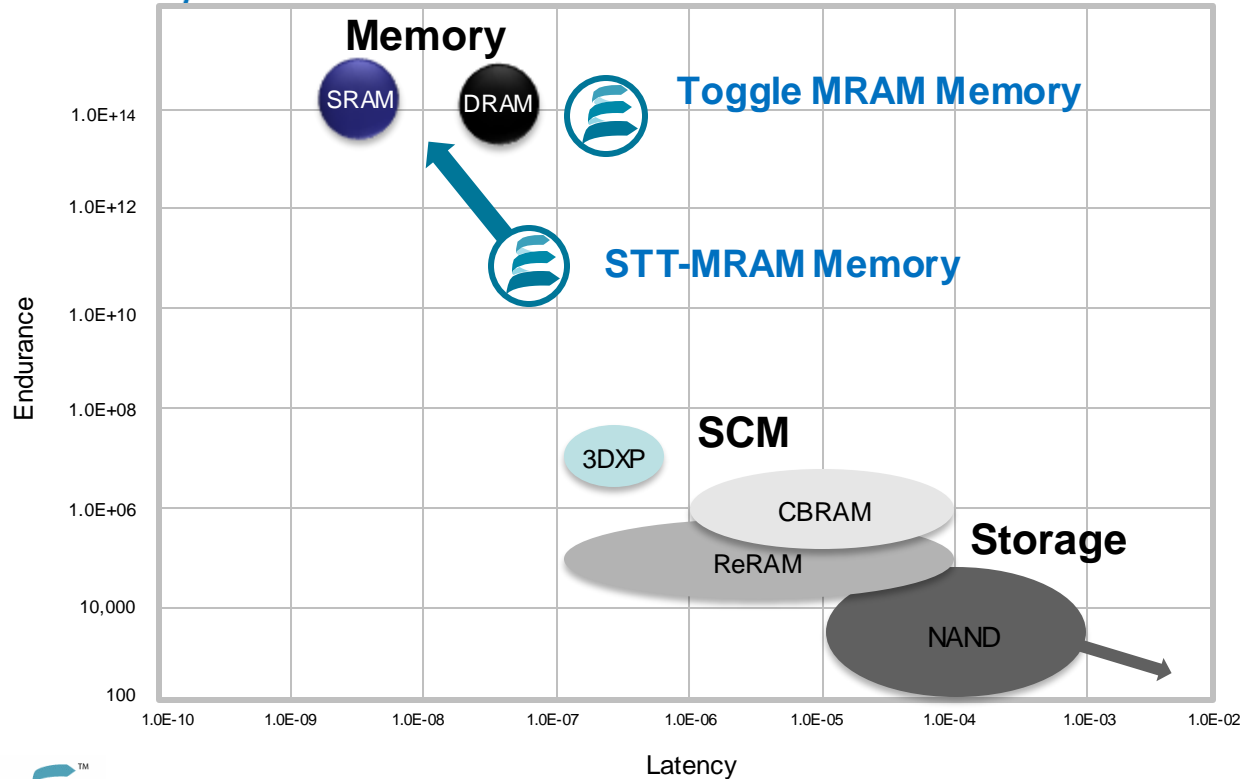
- MRAM Overview
 - Persistent SRAM and Persistent DRAM
- Choosing an Interface
 - What's the same, what's not
- Controller Design Considerations
 - Xilinx Memory Interface Generator (MIG) optimization
 - Additional design tips to get full benefit of MRAM
- Summary





MRAM – High Performance With Persistence

Flash Memory Summit



MRAM Combines Performance of Memory with Persistence of Storage

- High Performance: DRAM-class write performance
- Non-Volatile: Maintains memory without power
- Fast Write Speeds: Similar to SRAM and DRAM
- Superior Durability: Survives memory workloads
- No Refresh: Data requires no charge





Choosing an Interface for MRAM

- Familiar Standards for Toggle MRAM
 - SRAM- asynchronous with standard parallel I/O
 - Serial- SPI and multi variants (Single, Quad)
- Persistent DRAM with STT-MRAM
 - JEDEC DDR3 > ST-DDR3
 - DDR3 Controllers need to be adapted





ST-DDR3 has some timings differences vs. the JEDEC standard

Parameter	Symbol	DDR3-1333 DRAM		ST-DDR3-1333 STT-MRAM	
		ns (min)	ck (min)	ns (min)	ck (min)
ACTIVE to internal READ or WRITE delay time	<i>tRCD</i>	15	10	95	64
Precharge command period	<i>tRP</i>	15	10	66	44
ACTIVE to ACTIVE command period	<i>tRC</i>	51	34	170	114
ACTIVE to Precharge command period	<i>tRAS</i>	36	24	103	69
Write Recovery, WRITE to Precharge delay time	<i>tWR</i>	15	10	15	10
ACT to ACT Command Period, different banks	<i>tRRD</i>	6	4	30	20
Four ACTIVE Window	<i>tFAW</i>	30	20	120	80
REFRESH to ACT command delay (1Gb to 8Gb)	<i>tRFC</i>		74 – 234		Not Used

- Row latency, *tRCD*, and Precharge, *tRP*, are longer – typically outside the register range for these timings in most DDR3 controllers.
- Refresh is not required



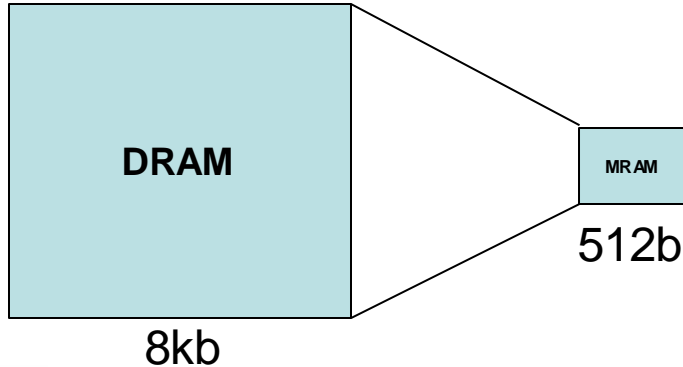


Page Size is Reduced for ST-DDR3

- DRAM Page sizes are optimized around REFRESH
- MRAM does not use REFRESH
- MRAM Page sizes are optimized to minimize power

Fewer Column Address bits

- DRAM Column Addr = 10b
- MRAM Column Addr = 6b



Parameter (bits)	JEDEC DDR3	256Mb ST-DDR3
<i>IO Width</i>	x8	x8
<i>Page size</i>	8,192	512
<i>tRASf</i>	3	6
<i>TXN_FIFO_DEPTH</i>	4	8
<i>TXN_FIFO_PWIDTH</i>	2	3
<i>CAS_FIFO_DEPTH</i>	4	8
<i>CAS_FIFO_PWIDTH</i>	2	3
<i>trcd_cntr / trcd_cntr_nxt</i>	4	6
<i>trp_cntr</i>	5	7
<i>tras_cntr_rb / tras_cntr_rb_nxt</i>	4	6
<i>Column Address Width (bits)</i>	$A_0 - A_9$ (10)	$A_0 - A_5$ (6)



Power-up with Persistent Data

- DRAM Controllers will calibrate after power-up by writing to the memory. With persistent memory, care must be taken to not overwrite user data.
- Mode register 2, bit 8 MR2[8] on the ST-DDR3 MRAM is used to provide a way to write to the device without overwriting user data.

- 1. Mode Register 2 (MR2) – 0x0110 MR2[8] = 1
 2. Mode Register 3 (MR3) – 0x0000
 3. Mode Register 1 (MR1) – 0x0044
 4. Mode Register 0 (MR0) – 0x0b60
 5. After Calibration and before normal operation
 6. Mode Register 2 (MR2) – 0x0010 MR2[8] = 0

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Power-down with Persistence

When power rail begins to: slump, over voltage, over current, over temperature

SCRAM Routine

1. Stop accepting any new commands
2. Process all pending commands
3. Complete all pending MRAM writes
 - a) **NOTE: To guarantee persistence, executing a Precharge (PRE) or Precharge All (PREA) command must be performed to move data in to the persistent memory array.**
4. Communicate that ALL pending writes are complete (assert **SCRAM_complete**)
5. It is now safe to power off MRAM without losing data.





Summary of Changes to Xilinx MIG

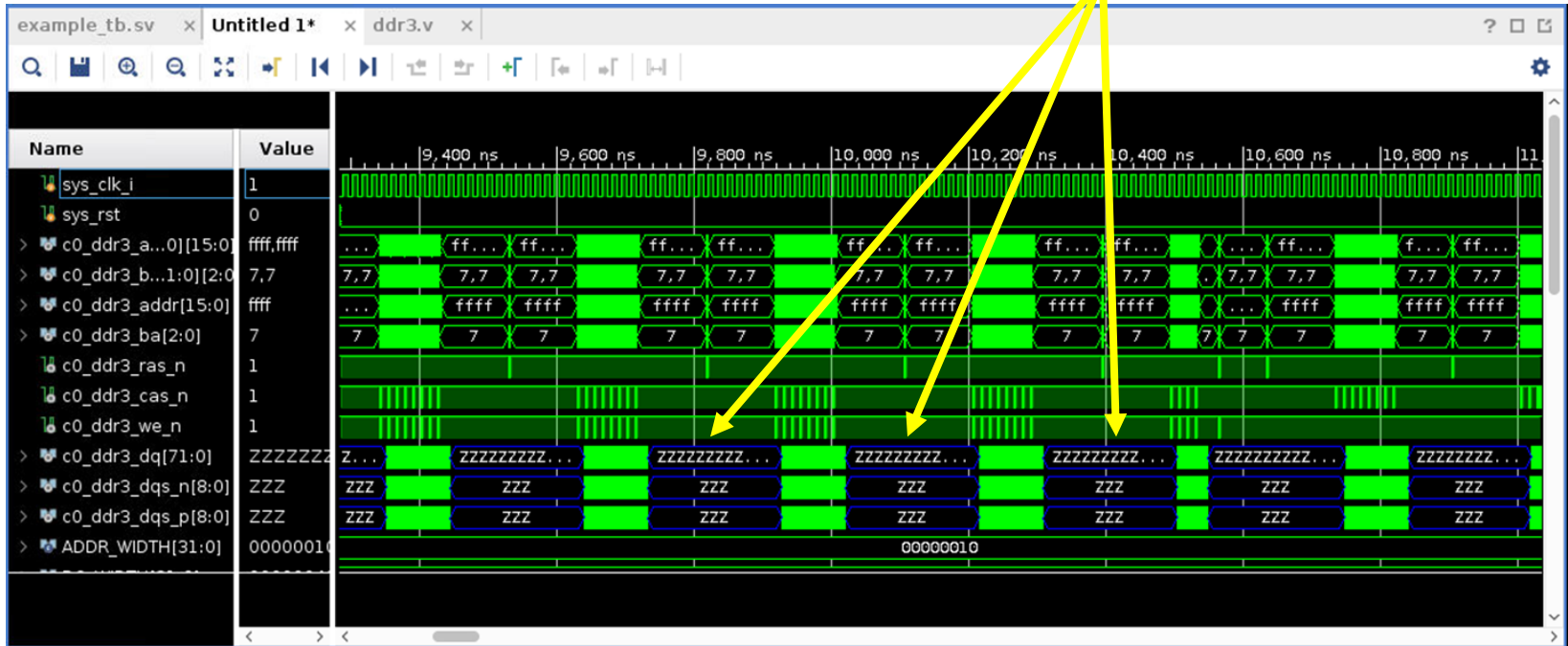
Category	STT-MRAM Timing Parameter and Performance Changes	<i>ddr3_0.sv</i>	<i>ddr3_0_ddr3.sv</i>	<i>ddr3_0_ddr3_mem_infc.sv</i>	<i>ddr3_v1_4_cal.sv</i>	<i>ddr3_v1_4_mc.sv</i>	<i>ddr3_v1_4_mc_arb_mux_p.sv</i>	<i>ddr3_v1_4_mc_group.sv</i>	<i>ddr3_v1_4_mc_ref.sv</i>	<i>ddr3_v1_4_ui.sv</i>	<i>ddr3_v1_4_ui_rd_data.sv</i>	<i>ddr3_v1_4_ui_wr_data.sv</i>
	File Number	1	2	3	4	5	6	7	8	9	10	11
Timing	Timing settings and counter width changes		X			X	X	X				
Power-up	Anti-scribbling changes (NOMEM mode)				X							
Power-down	SCRAM input signal to drain writes with CAS page closes	X	X	X		X			X			
Power-down	Created SCRAM output status signals	X	X	X		X		X		X		
Performance	Auto pre-charges on the 8 th BL8 of a CAS page		X			X				X	X	X
Performance	FIFO-DEPTH doubled							X				
Performance	Changed to emit requests faster							X				





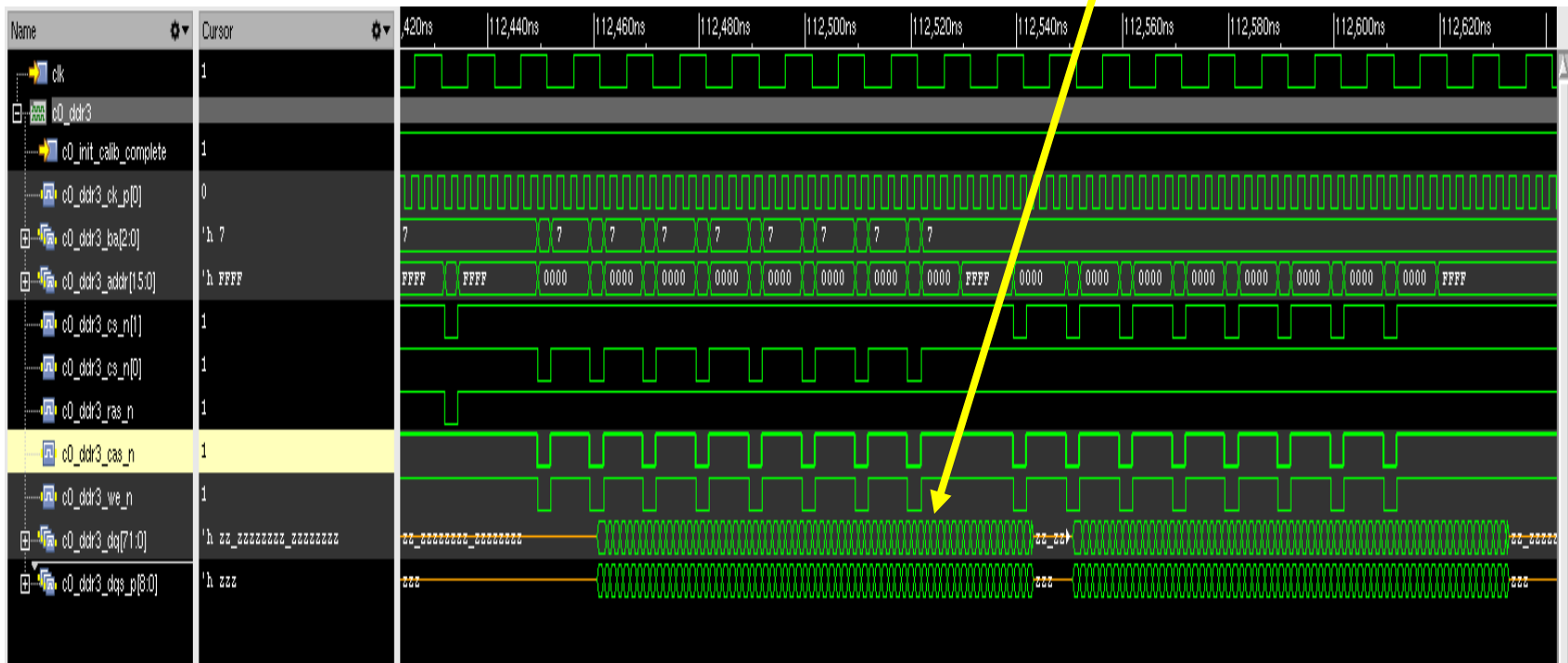
Performance

Note the Large gaps between bursts





Performance – improved bus utilization





Don't Reinvent the Wheel



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Query: size=144Mb;type=DRAMs;Synch Devices;Everspin

Help: Ex: vendor=MICRON,SAMSUNG,width=32bit;CAS Latency 5=true

Type: DRAMs;Synch Devices Vendor: -----All----- Size: min 0Bb

Class: -----All----- (classes in the above type) Data Width: --- All Widths--- Size: max 1Tb

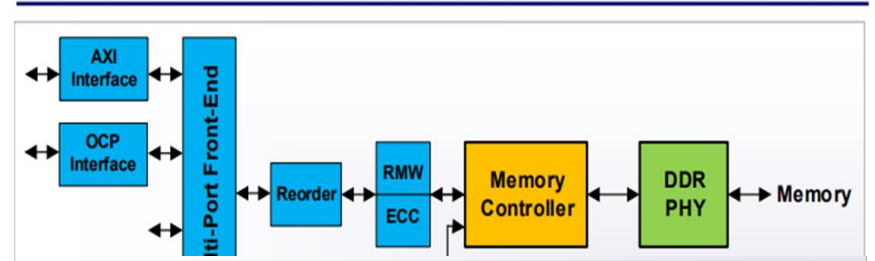
2 results

Vendor	Class	Configuration	Part Number	Downloads	MMIO/VPCAT Required	Avnet	Compare
EVERSPIN	ST_MRAM	256Mb (4M x 8 bit x 8 bank)	EMD3D256M			3,3036 / 11.30.034	<input type="button" value="Compare"/>
EVERSPIN	ST_MRAM	256Mb (2M x 16 bit x 8 bank)	ST-MRAM-256M-X16			3,3033 / 11.30.031	<input type="button" value="Compare"/>

Each item highlighted in red is available to you only under a non-disclosure agreement between Cadence and the part's vendor.

There are 6 more parts available under NDA. Please contact your memory vendors or your Cadence AE for more information.

NORTHWEST LOGIC Memory Interface Solution Overview



Solution Includes:

- Memory Controller Cores
 - Supports HBM2, GDDR6, DDR4/3, LPDDR4/3 and MRAM
 - 64 banks and 16 deep command queue support

Key Features:

- Complete Solution
 - Full featured and modular solution enables IP to be configured to exact customer requirements





Adapting Controllers for STT-MRAM

Summary

- Timing and page size changes needed for ST-DDR3
 - Performance optimization in Xilinx MIG DDR3 with sequencing, FIFO depth and address ordering
- Power Up and Power Down simplified
 - Persistent user data in memory needs to be accounted for
- Resources are available
 - Xilinx MIG support and design guide
 - ASIC design support from Cadence and Northwest Logic

