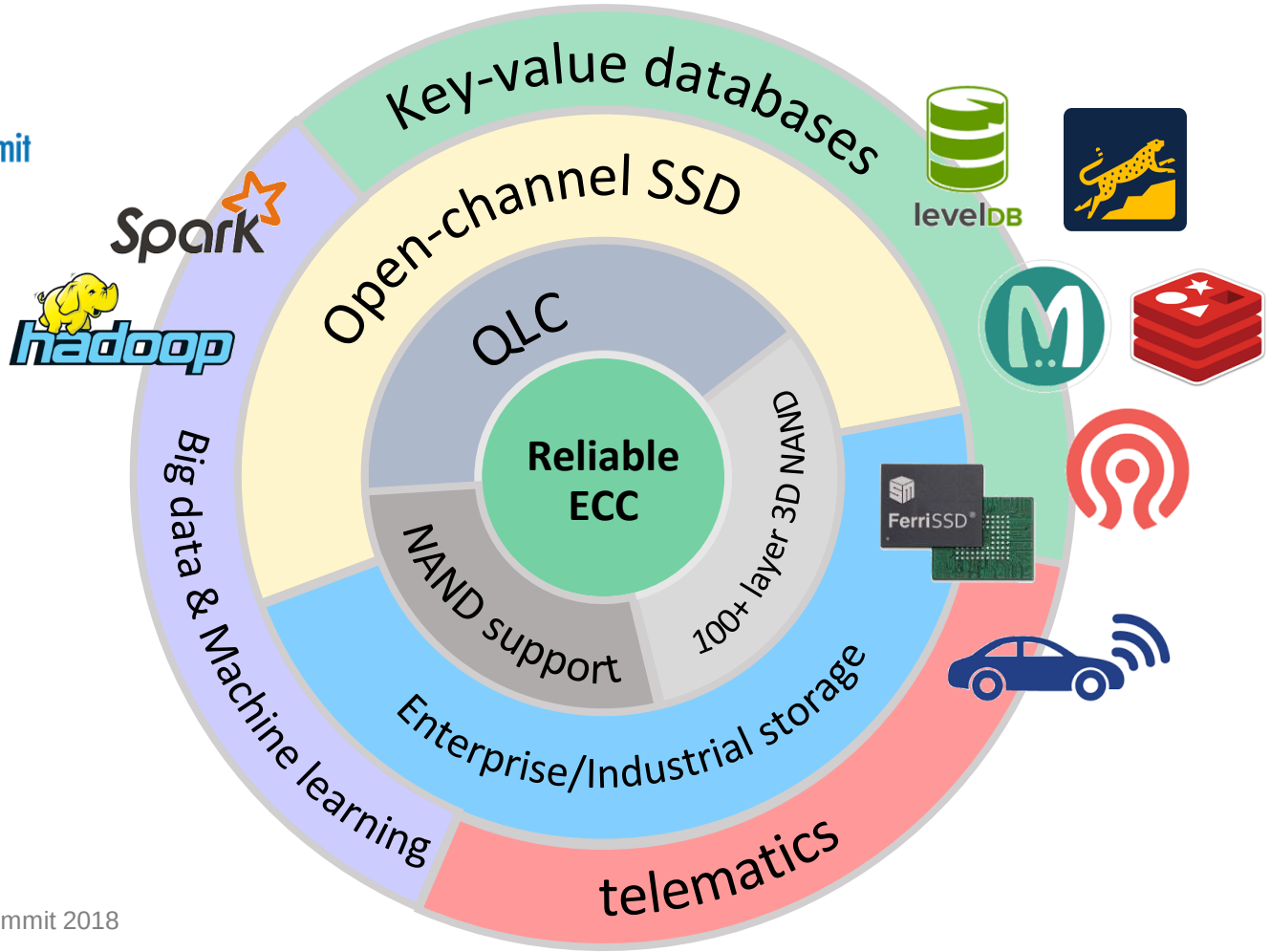
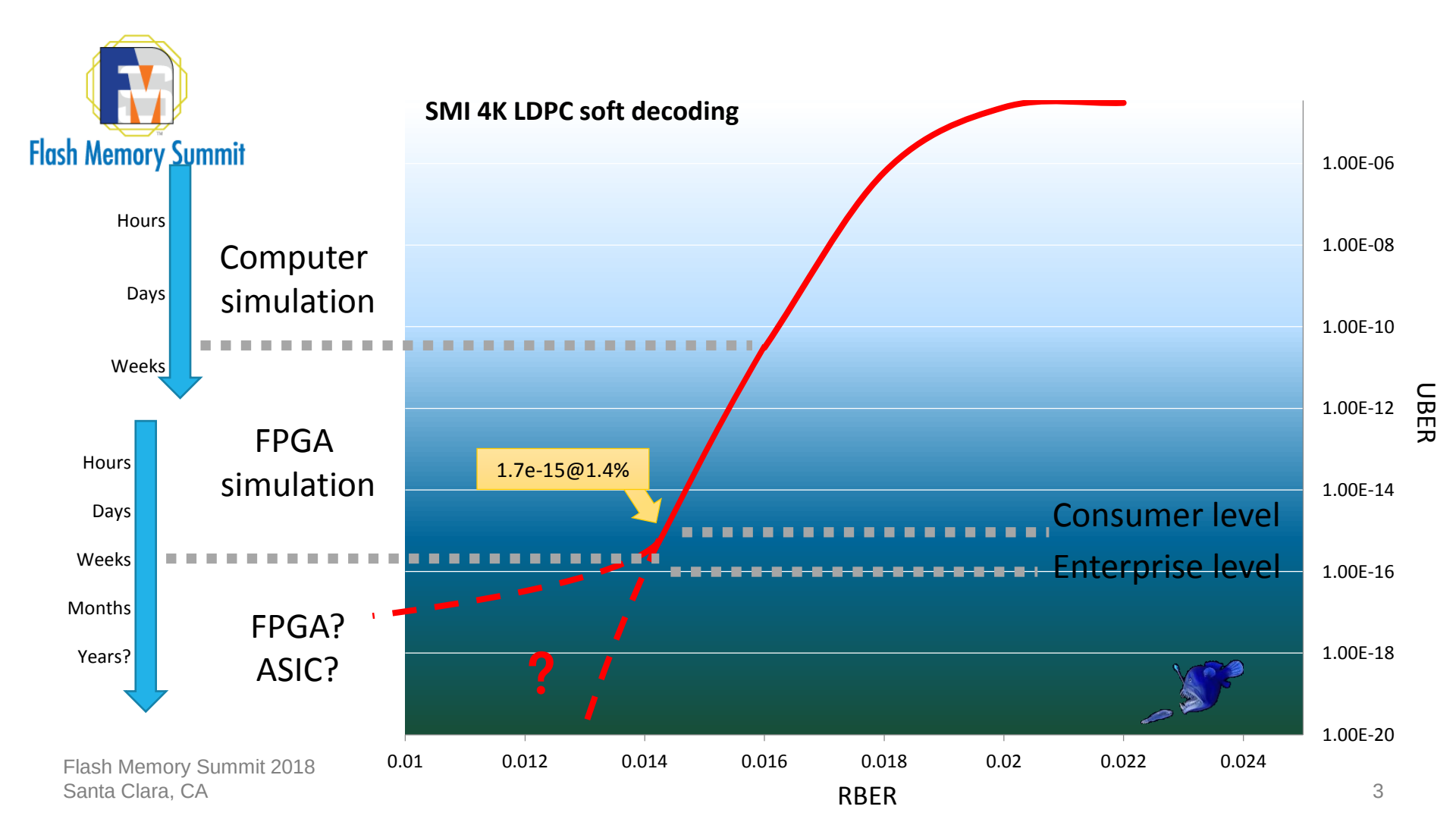
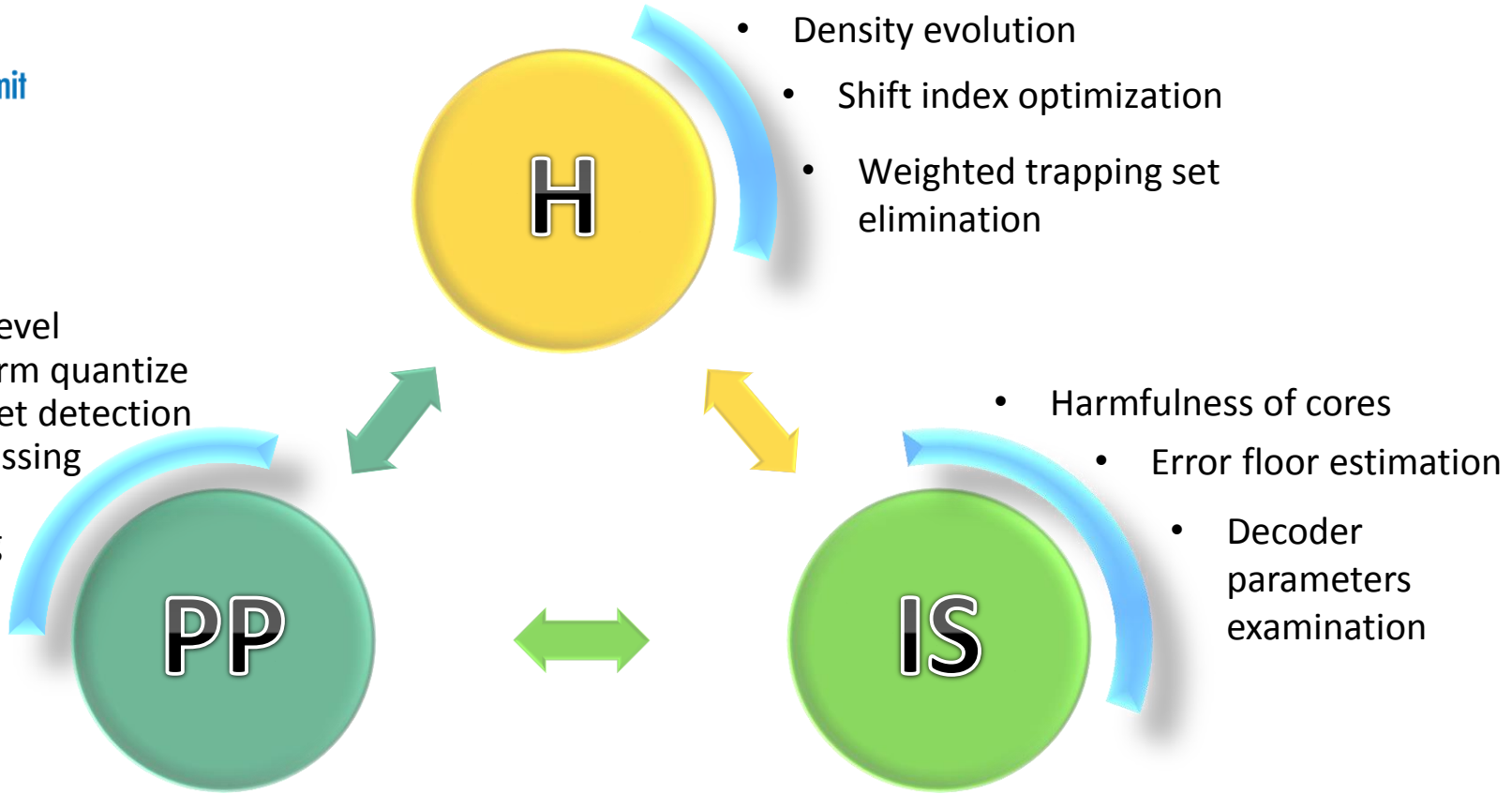
LDPC codes expand enterprise-level reliability

Dr. Shiuan-Hao Kuo

ECC team


Key-value databases
Open-channel SSD
QLC
Reliable ECC
NAND support
100+ layer 3D NAND
Big data & Machine learning
Enterprise/Industrial storage
telematics
Spark
hadoop
levelDB
FerriSSD

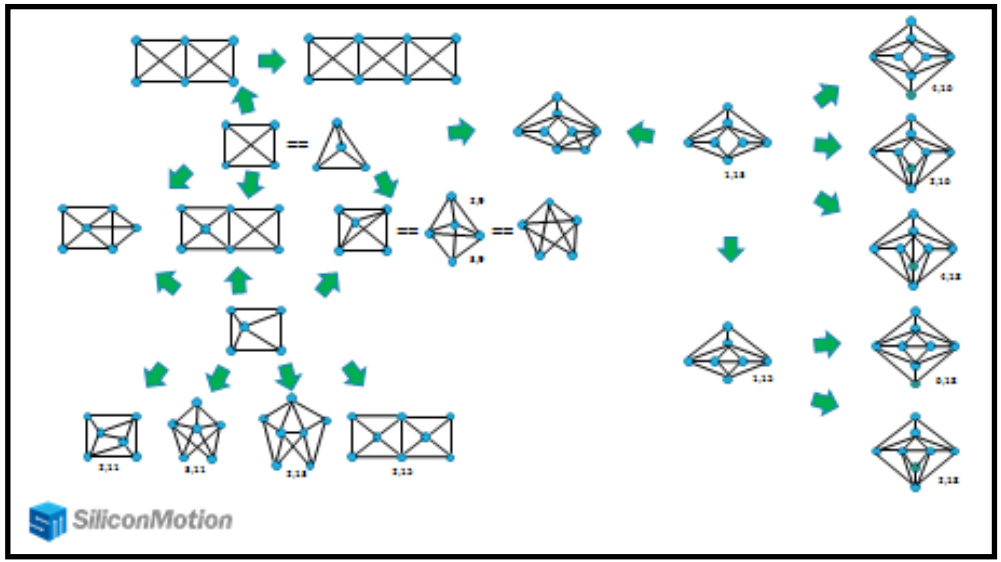

Flash Memory Summit
Hours
Days
Weeks
Computer simulation
Hours
Days
Weeks
Months
Years?
FPGA simulation
FPGA?
ASIC?
SMI 4K LDPC soft decoding
1.7e-15@1.4%
Consumer level
Enterprise level
?
1.00E-06
1.00E-08
1.00E-10
1.00E-12
1.00E-14
1.00E-16
1.00E-18
1.00E-20
UBER
0.01
0.012
0.014
0.016
0.018
0.02
0.022
0.024
RBER


H
Density evolution
Shift index optimization
Weighted trapping set elimination
PP
Quantize level
Non-uniform quantize
Trapping set detection
Post processing
Post- post processing
IS
Harmfulness of cores
Error floor estimation
Decoder parameters examination

Code design

- What is a good LDPC code
  - Sharp waterfall.
  - Low error floor.
- Design criterions
  - A good asymptotic performance.
  - No cycle 4 is allowed.
  - Minimize the count of cycle 6.
  - A feasible encoding algorithm.
  - Anything else?

Harmful trapping sets !



➢ Shiuan-Hao Kuo, Zhen-U Liu and Jeff Yang, “On practical LDPC code construction for NAND flash applications”, Information Theory Workshop (**ITW**), Nov. 2017.

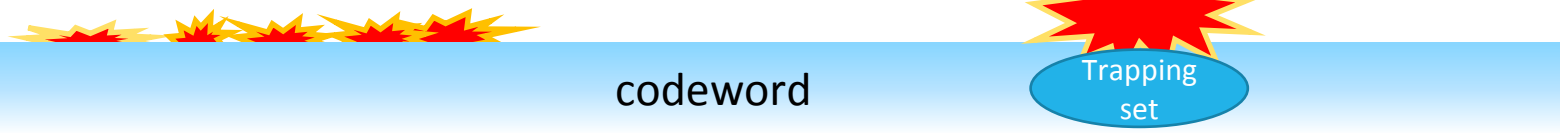
Importance Sampling

IS

- How to proof error floor beyond 10^{-16} UBER
  - FPGA / ASIC simulation – time consuming / huge cost.
  - High reliability error (on FPGA)– bombard the codeword.
  - Importance sampling (computer / FPGA) – missile attack.

High reliability error test

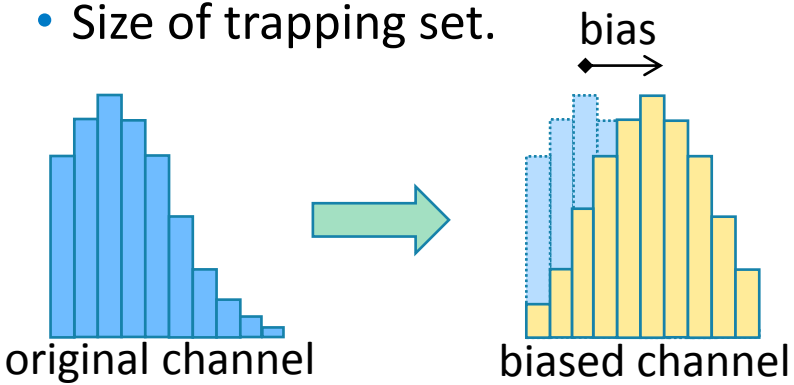
Importance sampling

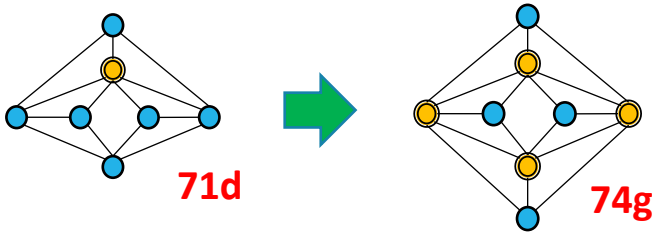


Importance Sampling

IS

- having samples generated from a different distribution.
- Add biased noise to the position of trapping set cores.
- Trapping set inheritance.
- Size of trapping set.



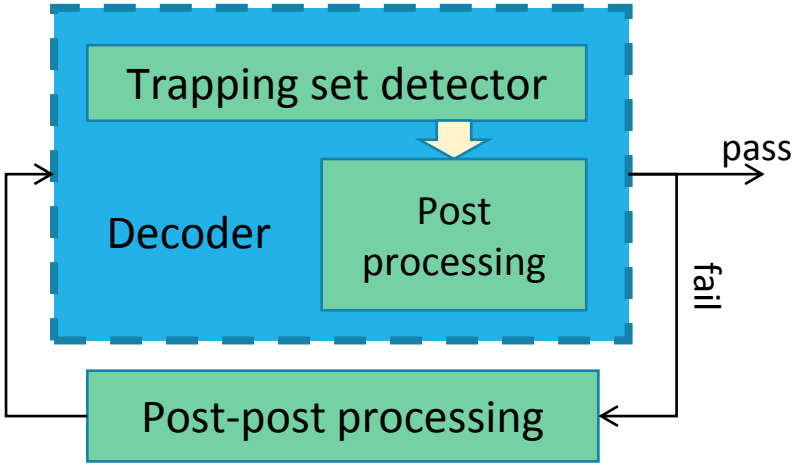


- RBER 1%, 8 variable node
- Size of CPM is *p*.
- Harmful factor *h*.
- Weighted FER ≈ $hxpx10^{-16}$

Post processing

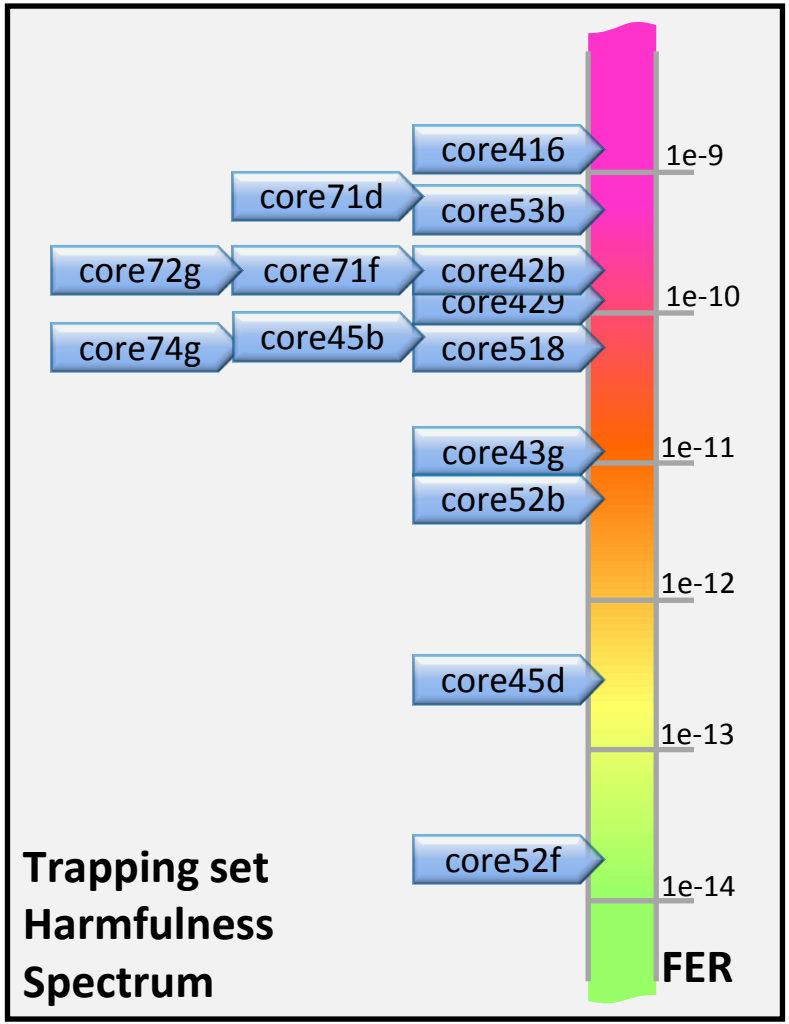
PP

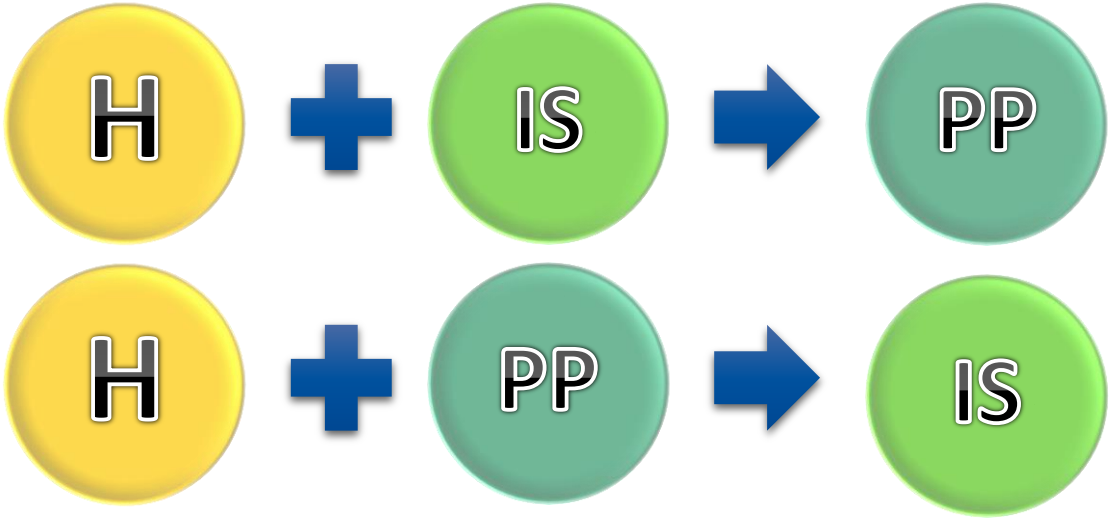
- Methods to dynamically break trapping sets during decoding.
  - Trapping set detection
    - Detection criterion
  - Post processing
    - Variable node
    - Check equation
  - Post-post processing
    - LLR table…etc.



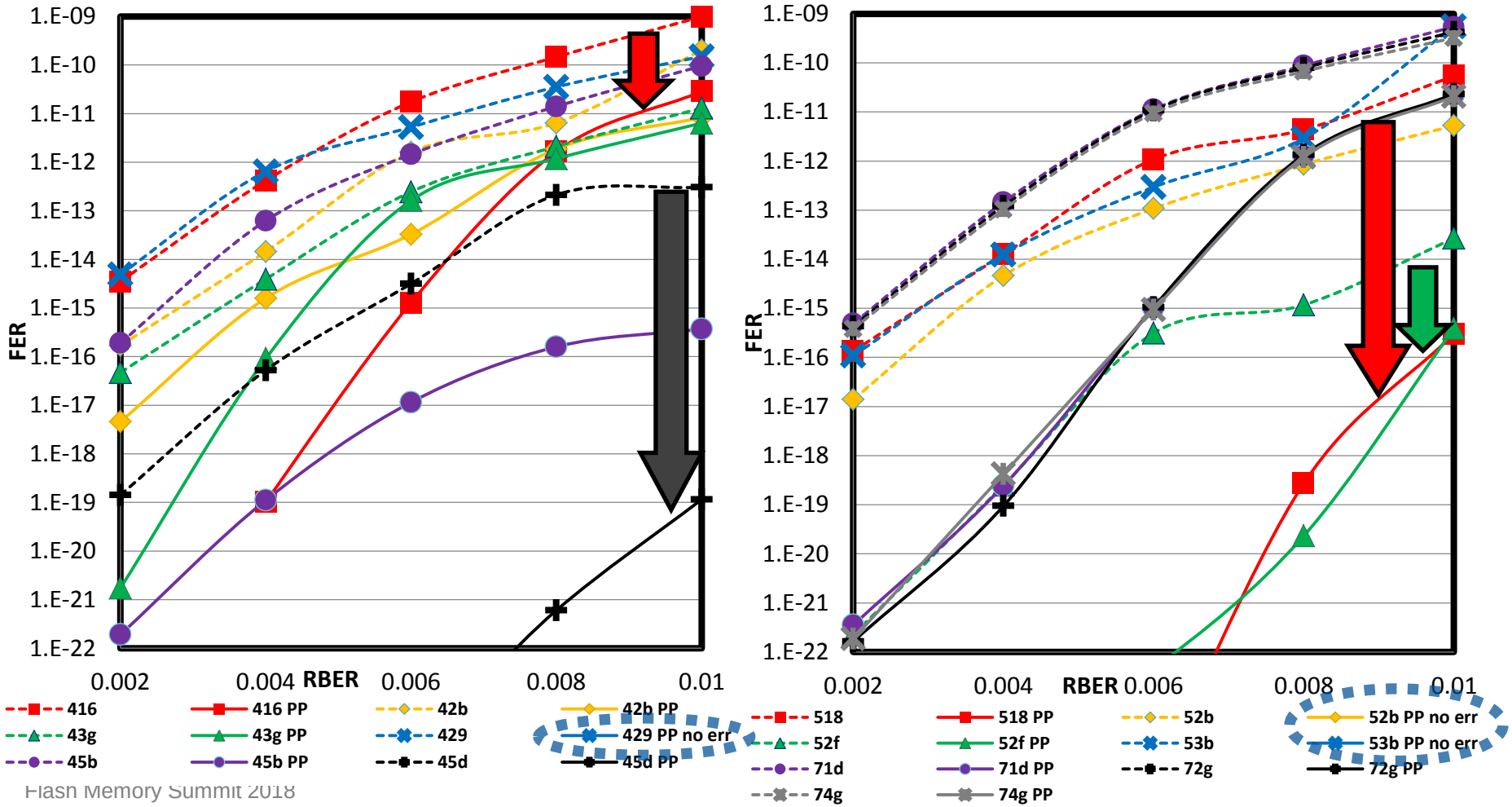
- Tuning decoder
  - Range of values, (non-uniform) quantization level, decoder status indicator … etc.

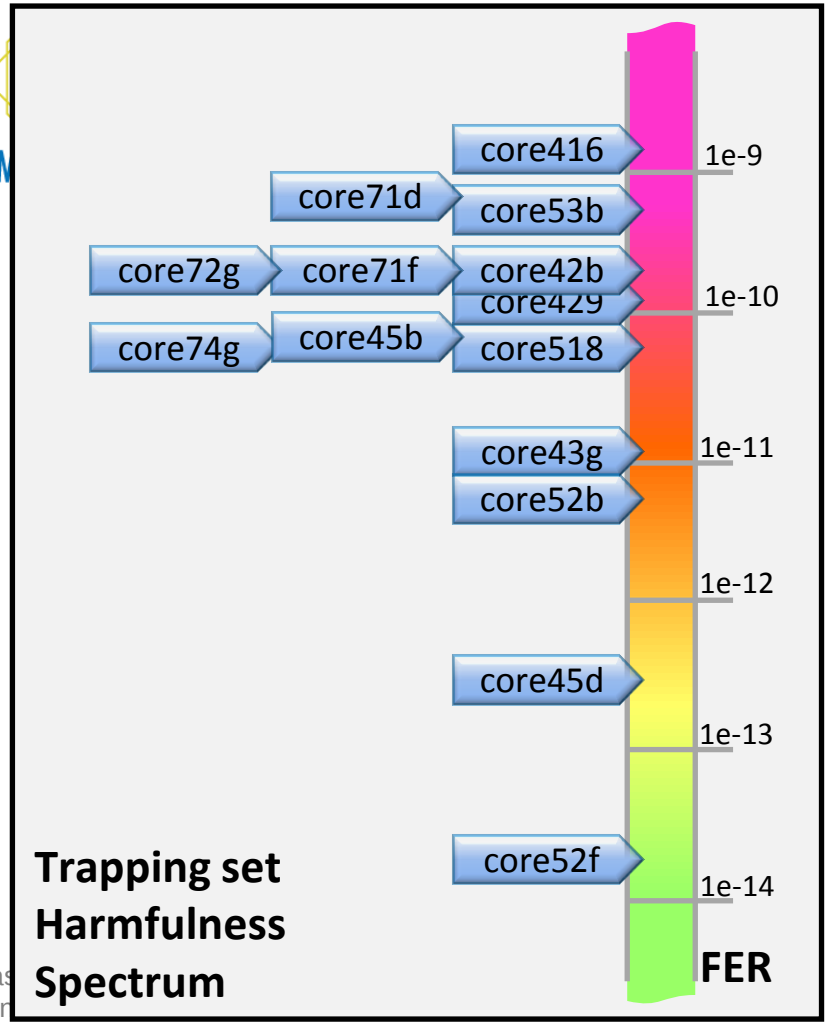
- Construct multiple LDPC codes.
  - BASE matrix
  - Girth and small cycles
- Detect and categorize trapping sets.
  - HRE
  - Topology
- Harmfulness – maximum possible error floor by importance sampling.

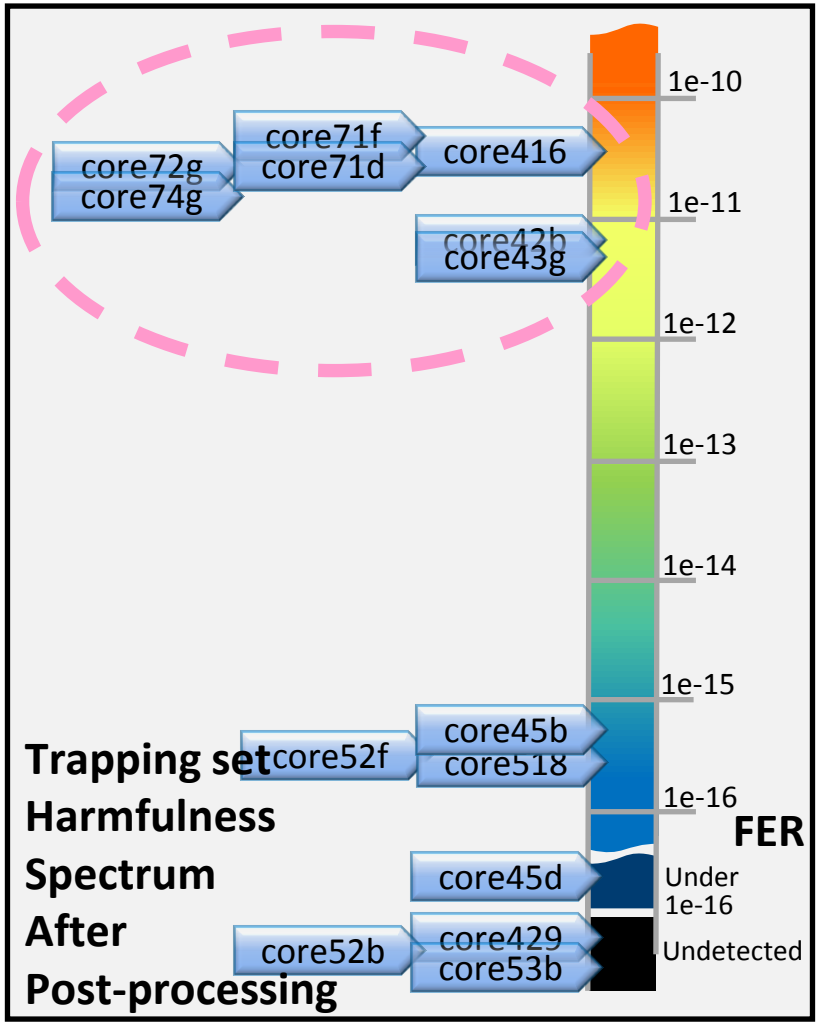


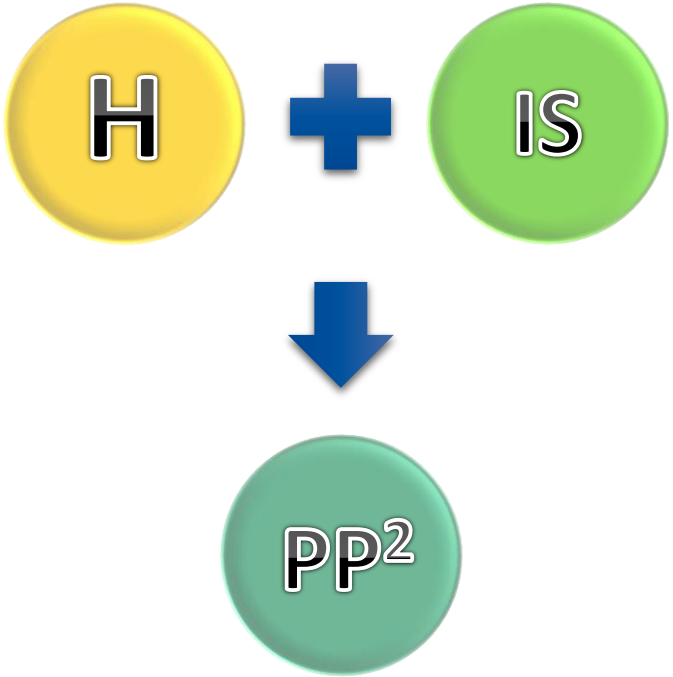


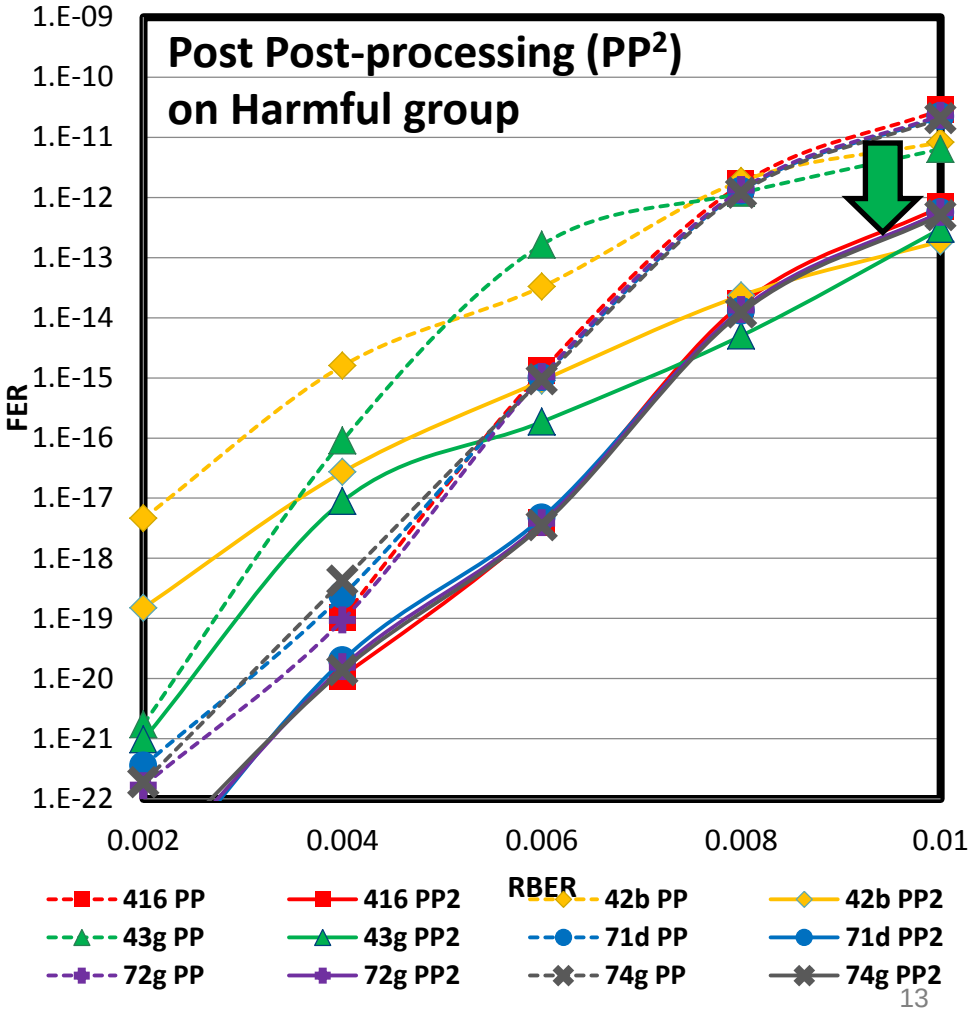
- LDPC codes and their list of harmful trapping set
- Decoder algorithm & Post Processing
  - Trapping set detection
  - Trapping set elimination
- Harmfulness after post processing.


1.E-09
1.E-10
1.E-11
1.E-12
1.E-13
1.E-14
1.E-15
1.E-16
1.E-17
1.E-18
1.E-19
1.E-20
1.E-21
1.E-22
FER
0.002
0.004
0.006
0.008
0.01
RBER
416
416 PP
42b
42b PP
43g
43g PP
429
429 PP no err
45b
45b PP
45d
45d PP
518
518 PP
52b
52b PP no err
52f
52f PP
53b
53b PP no err
71d
71d PP
72g
72g PP
74g
74g PP

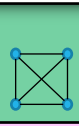
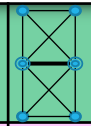
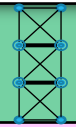
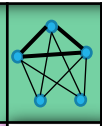
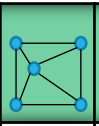
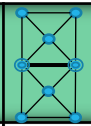
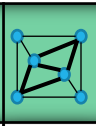
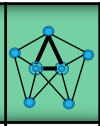
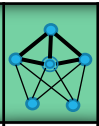
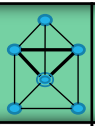
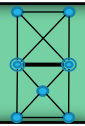
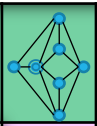
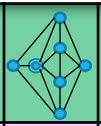
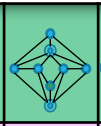
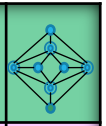

core416
core71d
core53b
core72g
core71f
core42b
core74g
core45b
core518
core43g
core52b
core45d
core52f
1e-9
1e-10
1e-11
1e-12
1e-13
1e-14
FER
Trapping set Harmfulness Spectrum

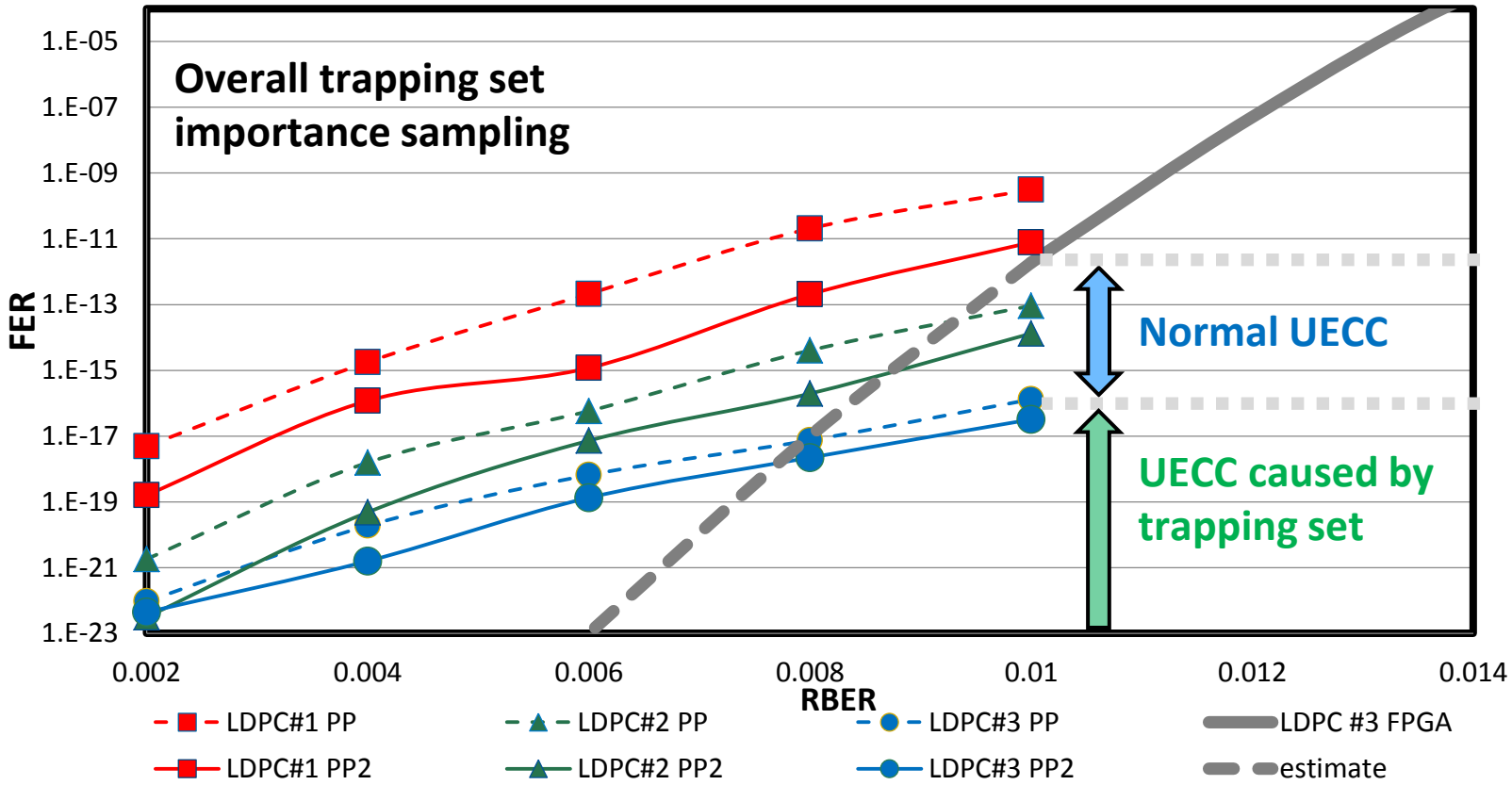

core72g
core74g
core71f
core71d
core416
core43g
core52f
core45b
core518
core45d
core52b
core53b
1e-10
1e-11
1e-12
1e-13
1e-14
1e-15
1e-16
FER
Under 1e-16
Undetected
Trapping set Harmfulness Spectrum After Post-processing


H
IS
PP2


Post Post-processing (PP2) on Harmful group
FER
1.E-09
1.E-10
1.E-11
1.E-12
1.E-13
1.E-14
1.E-15
1.E-16
1.E-17
1.E-18
1.E-19
1.E-20
1.E-21
1.E-22
0.002
0.004
0.006
0.008
0.01
RBER
416 PP
416 PP2
42b PP
42b PP2
43g PP
43g PP2
71d PP
71d PP2
72g PP
72g PP2
74g PP
74g PP2

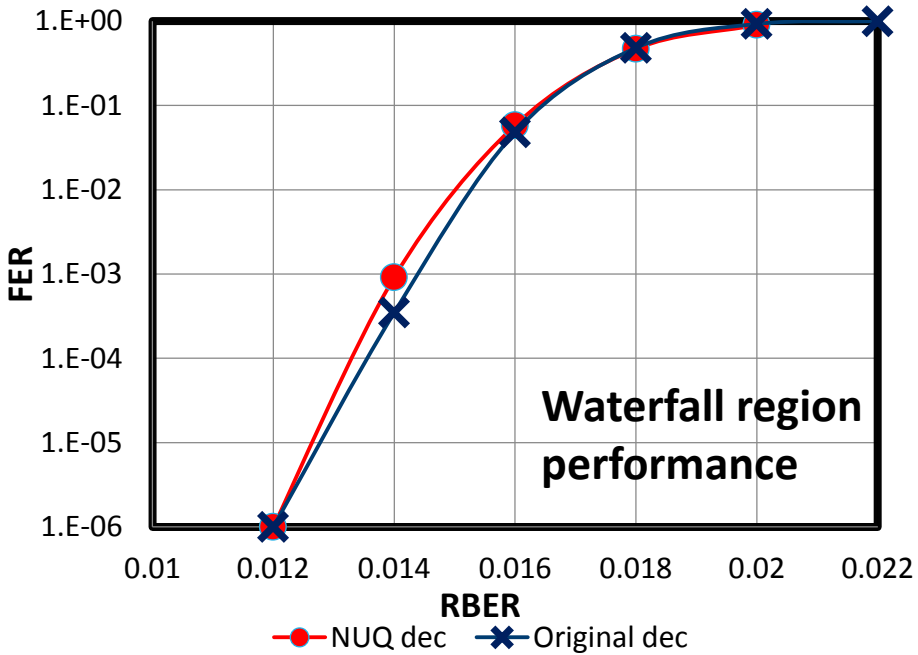
- Reduce / eliminate harmful trapping sets during code construction

ETS core	 416	 42b	 43g	 429	 518	 52f	 52b	 52d	 53b	 45b	 45d	 71d	 71f	 72g	 74g
LDPC#1	167	17	3		201	6					10	178	27	21	10
LDPC#2												113		14	8
LDPC#3	54	1			75										


Overall trapping set
importance sampling
Normal UECC
UECC caused by
trapping set
FER
1.E-05
1.E-07
1.E-09
1.E-11
1.E-13
1.E-15
1.E-17
1.E-19
1.E-21
1.E-23
0.002
0.004
0.006
0.008
0.01
0.012
0.014
RBER
LDPC#1 PP
LDPC#2 PP
LDPC#3 PP
LDPC #3 FPGA
LDPC#1 PP2
LDPC#2 PP2
LDPC#3 PP2
estimate

Algorithm verification

- Example: Non-uniform quantization



LDPC #3, ETS Core416 RBER 0.01 / biased RBER 0.99		Original decoder	
		Pass	Fail, FER
NUQ decoder	Pass		4.57176e-18 undetectable
	Fail, FER	1.30449e-09 2.10987e-15	undetectable

LDPC #3, ETS Core518 RBER 0.01 / biased RBER 0.99		Original decoder	
		Pass	Fail, FER
NUQ decoder	Pass		2.06629e-19 undetectable
	Fail, FER	7.25905e-11 4.11553e-16	undetectable

Summary

- LDPC construction
- Decoder algorithm design
- Verification method

Error floor	MLC support	TLC support	QLC support
SMI 1K LDPC code	$<10^{-11}$ FER ($\approx 10^{-15}$ UBER)	$<10^{-16}$ FER ($\approx 10^{-20}$ UBER)	Undetectable
SMI 2K LDPC code	$<10^{-13}$ FER ($\approx 10^{-17}$ UBER)	Undetectable	Undetectable
SMI 4K LDPC code	$<10^{-14}$ FER ($\approx 10^{-18}$ UBER)	Undetectable	Undetectable

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Thanks for your attention!