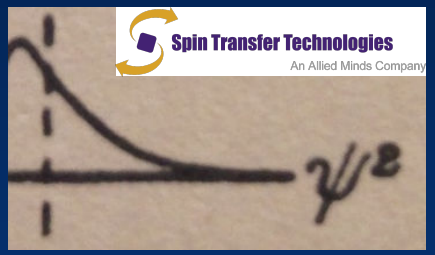
Flash Memory Summit



Breaking Through "Impenetrable" Barriers

The Key to the Evolution of Solid State Memory

A Pictorial Approach

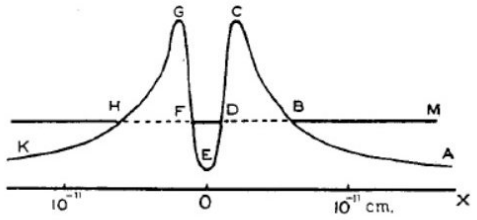
Andrew J. Walker PhD

The Link between α-particles, 3-D NAND and MRAM? - Quantum Tunneling

Flash Memory Summit

SEPTEMBER 22, 1928] NATURE

Wave Mechanics and Radioactive Disintegration

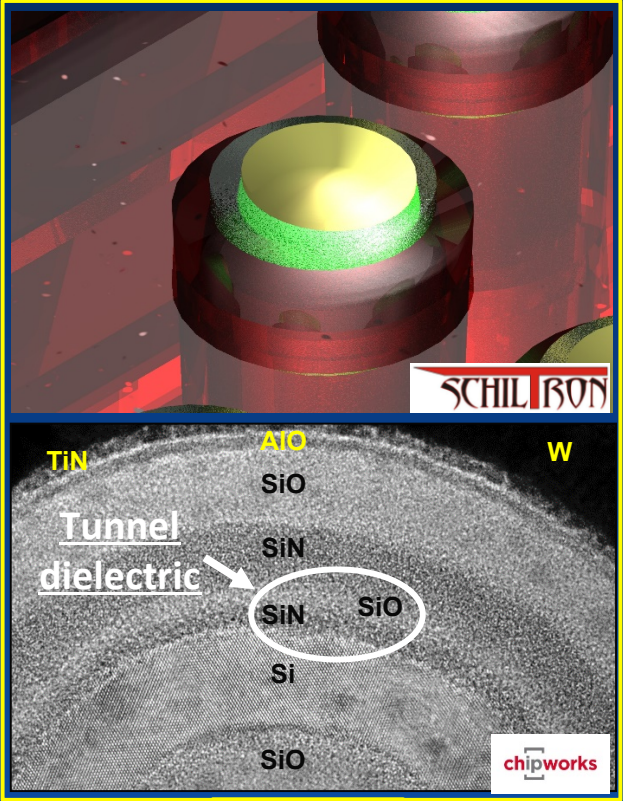


Much has been written of the explosive violence with which the α-particle is hurled from its place in the nucleus. But from the process pictured above, one would rather say that the α-particle slips away almost unnoticed.

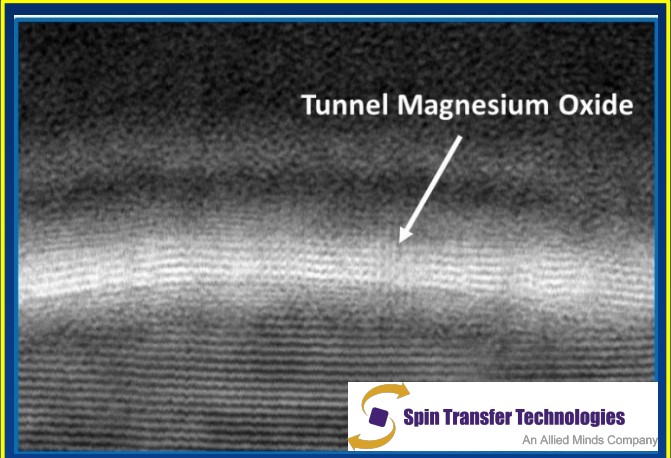
RONALD W. GURNEY.
EDW. U. CONDON.

Palmer Physical Laboratory,
Princeton University,
July 30.

α-particles



3-D NAND



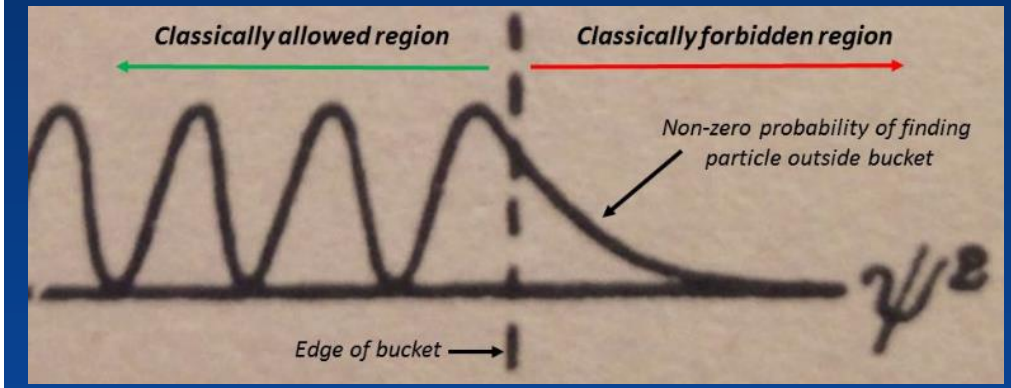
Free layer	*CoFeB*
Tunnel barrier	*MgO*
Reference layer	*CoPt*

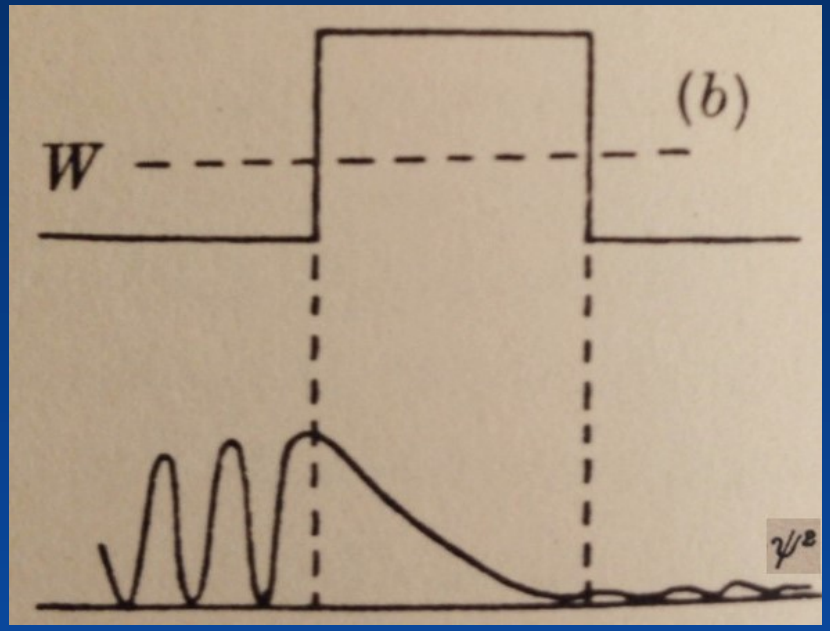
STT-MRAM

Contents

Flash Memory Summit

What is Tunneling?





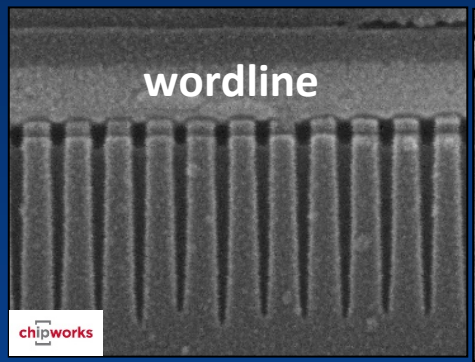
***Elementary Quantum Mechanics*, R.W. Gurney, 2nd ed., Cambridge University Press, 1940**

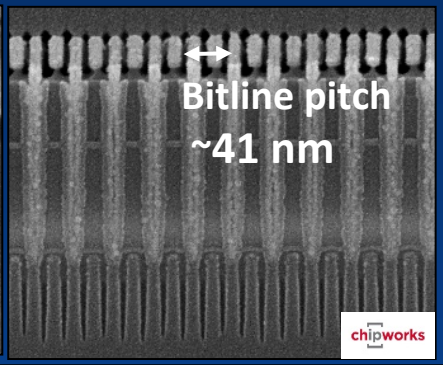
Tunneling in Solid State Memories

- ***2-D NAND***
  - Charge tunneling to and from a Floating Gate
- ***3-D NAND***
  - Charge tunneling to and from:
    - Silicon Nitride (Samsung, Toshiba, WD-SanDisk, Hynix)
    - Floating gate (Intel, Micron)
- ***Classic SONOS***
  - Charge tunneling to and from silicon nitride
- ***STT-MRAM***
  - Electron tunneling between magnetic metals

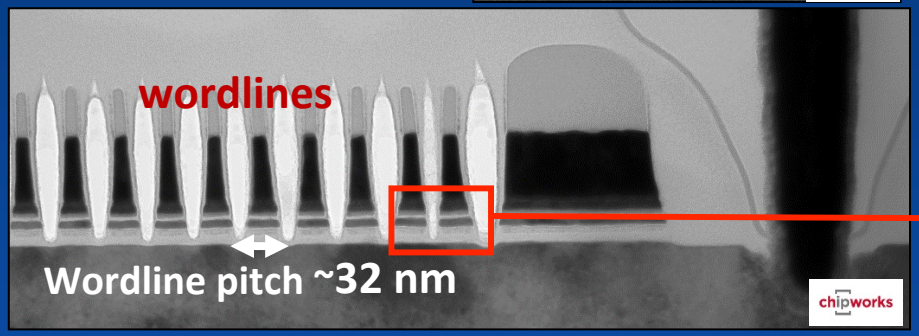
Flash Memory Summit

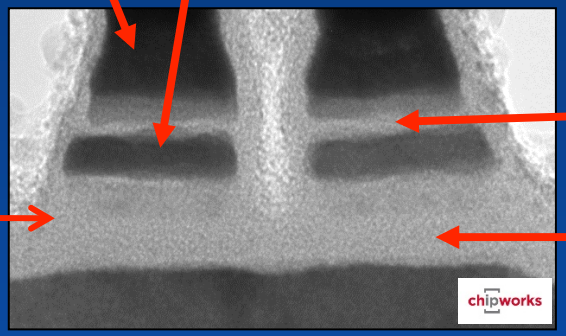
2-D NAND





128 Gbit 16 nm 2-D NAND from Intel/Micron



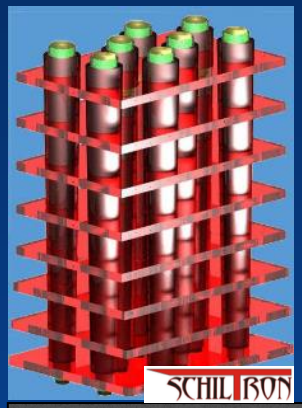


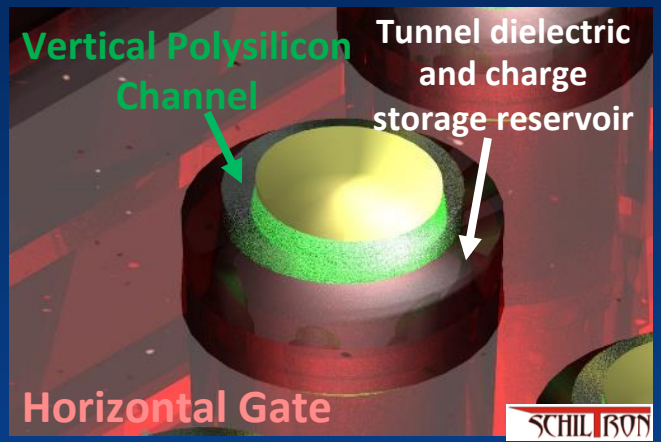
Dielectrics between gates

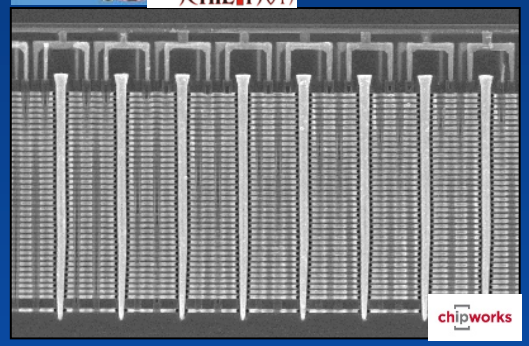
Tunnel oxide (~7 nm)

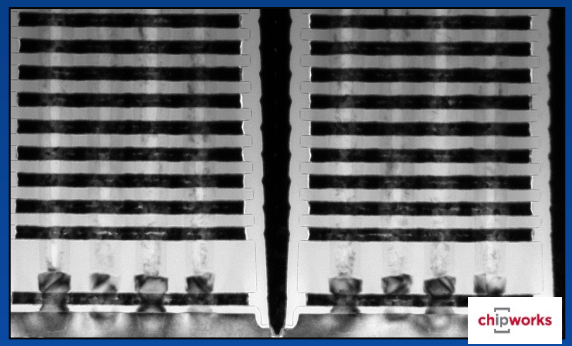
3-D NAND

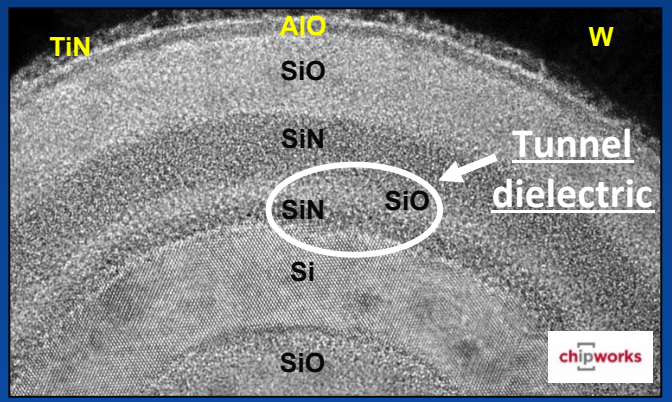
Flash Memory Summit





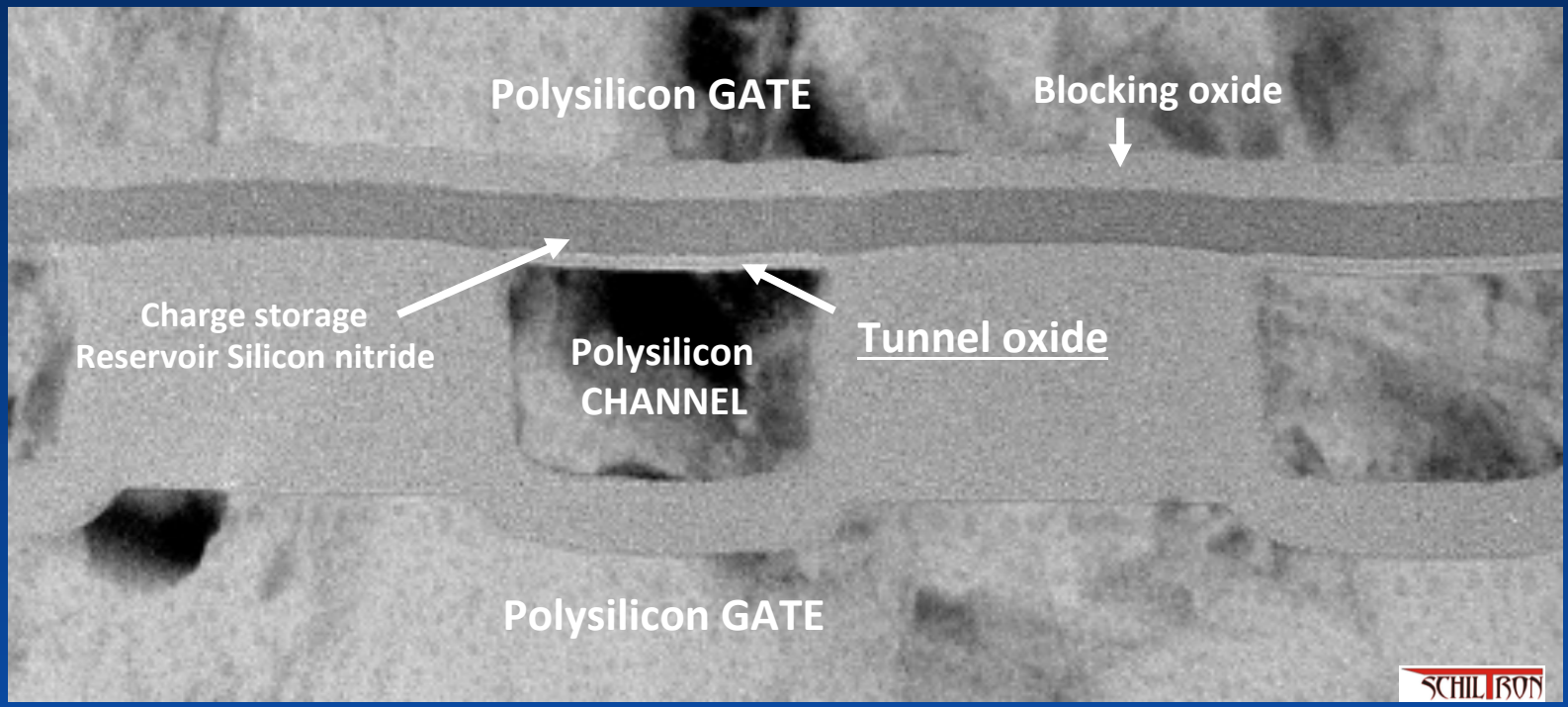






86 Gbit V-NAND from Samsung

Classic SONOS



A.J. Walker, IEEE Trans. Elect. Dev., vol.56, Nov.2009

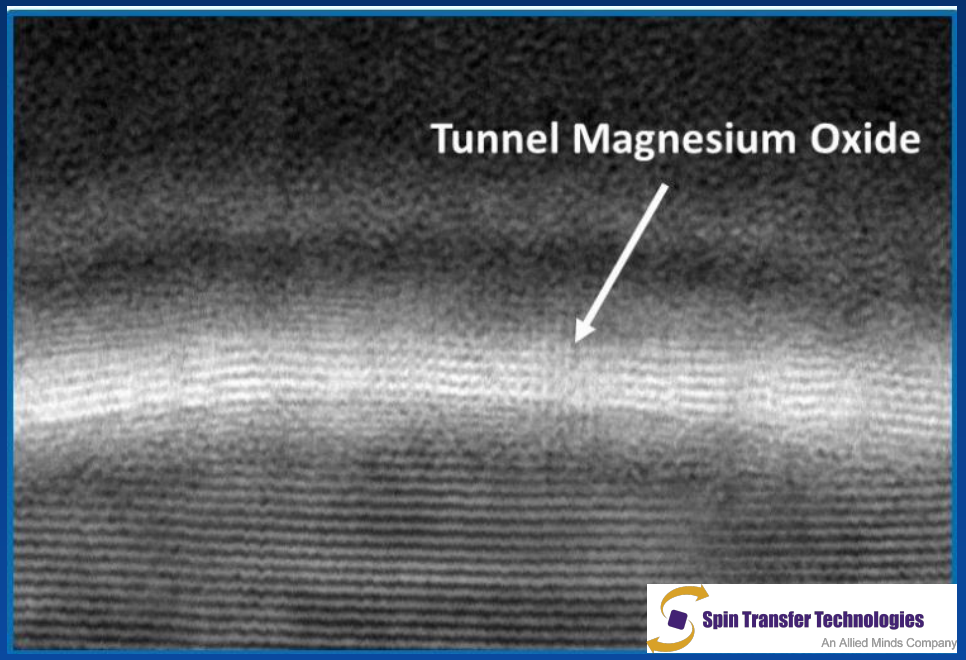
STT-MRAM

Low resistance P-state Logical "0"

Free layer	↑	*CoFeB*
Tunnel barrier		*MgO*
Reference layer	↑	*CoPt*

High resistance AP-state Logical "1"

Free layer	↓	*CoFeB*
Tunnel barrier		*MgO*
Reference layer	↑	*CoPt*



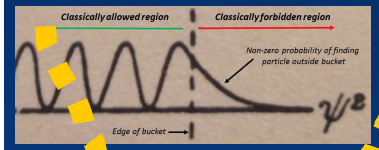
Tunneling Damage

- ***Rule of Thumb:***
  - Tunneling creates more damage in thicker tunnel dielectrics
- ***What is thick and what is thin?***
  - >/~ 3.5nm is THICK (2-D and 3-D NAND)
  - </~ 3.5nm is THIN (Classic SONOS and STT-MRAM)
- ***What is damage and what are the consequences?***
  - Charge trapping:
    - Threshold voltage shifts (in MOS-based memories – NAND and Classic SONOS)
    - Shifts in Current-Voltage characteristics
  - Stress induced damage:
    - Limited retention (in MOS-based memories – NAND and Classic SONOS
    - Wear out and breakdown

The Golden Thread of Tunneling

- From Fundamental Physics to Technological Innovation (1)

Flash Memory Summit



Electron Emission in Intense Electric Fields.

By R. H. Fowler, F.R.S., and Dr. L. Nordheim.

(Received March 31, 1928.)

Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character, Volume 119, Issue 781 (May 1, 1928), 173-181.

In order to study the emission through the potential energy surface of fig. 1 we have only to solve the wave equations (4) (5)

Fowler-Nordheim

FUNDAMENTAL PHYSICS 1928

MOSFET 1960

United States Patent Office 3,102,230 Patented Aug. 27, 1963

Aug. 27, 1963 DAWON KAHNG 3,102,230

FIELD CONTROLLED SEMICONDUCTOR DEVICE

Filed May 31, 1960

FIG. 1A

Kahng

CHARGE TRAP 1967-68

11.4 THE VARIABLE THRESHOLD TRANSISTOR, A NEW ELECTRICALLY-ALTERABLE, NON-DESTRUCTIVE READ-ONLY STORAGE DEVICE, H. A. R. Wegener, A. J. Lincoln, H. C. Pao, M. R. O'Connell, and R. E. Oleksiak, Sperry Rand Research Center, Sudbury, Mass.: H. Lawrence, Sperry Semiconductor, Norwalk, Conn.

A memory element has been developed that has the structure of a typical silicon planar p-channel enhancement insulated-gate field-effect transistor ... stored by setting the threshold voltage of the ... value. Interrogation is accomplished by applying a ... to the threshold voltage extremes. Current will flow ... the recorded threshold voltage is less negative ... voltage; none will flow if the recorded threshold ... A high (negative) threshold voltage is written by ... or higher for a duration of 1 msec or less between gate and substrate. A low threshold voltage is similarly obtained with positive 50 v pulse. The persistence of stored information has been demonstrated for periods of at least several months.

The storage mechanism will be discussed and experimental data that describe the write-in, read-out, and storage characteristics of this device will be presented. The results of its application in various experimental circuits, including a one-by-four electrically-alterable read-only memory, will be given in conclusion.

Wegener et al.

United States Patent Office 3,206,670 Patented Sept. 14, 1965

Sept. 14, 1965 M. M. ATALLA 3,206,670

FOR DEVICES HAVING DIELECTRIC COATINGS

Filed March 8, 1960

FIG. 5

Atalla

24.3 MONOS MEMORY ELEMENT, B. V. Keshavan and H. C. Lin, Westinghouse Electric Corporation, Integrated Circuit Division, Linthicum, Md.

The use of metal-nitride-oxide-semiconductor structure as a storage element was reported by Szedon ... the 1967 Device Research Conference. When such a structure is used as p-channel enhancement mode device, a positive gate voltage exceeding a certain critical value changes the device into depletion mode. Later when a negative gate voltage of the ... of this critical voltage is applied, the device changes back to enhancement ... explained as electron tunneling from the ... the traps in the nitride with a ... semiconductor with negative gate bias. ... element.

Keshavan & Lin

A Floating Gate and Its Application to Memory Devices

By D. KAHNG and S. M. SZE

(Manuscript received May 16, 1967)

When the emission is Fowler-Nordheim tunneling type, then the current density, j, has the form

$$j = C_1 E^2 \exp(-E_0/E), \quad (2a)$$

In conclusion it has been demonstrated that the controlled field emission through a buried "floating" gate may be capacitively induced by ... the outer gate electrode. This combination can therefore, be used as a memory device, with holding time as long as the dielectric relaxation time of the gate structure and with continuous nondestructive read-out capability. There seems to be no inherent reason why read-in read-out cannot be performed in a very short time, say in the nanosecond range or even shorter.

Kahng & Sze*

FLOATING GATE 1967

JOURNAL OF APPLIED PHYSICS VOLUME 40, NUMBER 8 JULY 1969

Charge Transport and Storage in Metal–Nitride–Oxide–Silicon (MNOS) Structures*

D. Frohman-Bentchkovsky and M. Lenzlinger

Fairchild Semiconductor, Research and Development Laboratory, 4001 Miranda Avenue, Palo Alto, California 94304

(Received 19 February 1969; in ... 31 March 1969)

Frohman-Bentchkovsky & Lenzlinger

EEPROM 1978

United States Patent [19] Harari [11] 4,115,914 [45] Sep. 26, 1978

ELECTRICALLY ERASABLE NON-VOLATILE SEMICONDUCTOR MEMORY

Inventor: Eliyahou Harari, Irvine, Calif.

Assignee: Hughes Aircraft Company, Culver City, Calif.

Appl. No.: 770,346

Filed: Feb. 22, 1977

Harari*

JOURNAL OF APPLIED PHYSICS VOLUME 40, NUMBER 1 JANUARY 1969

Fowler-Nordheim Tunneling into Thermally Grown SiO_2

M. Lenzlinger and E. H. Snow

Fairchild Semiconductor Research and Development Laboratory, Palo Alto, California 94304

(Received 20 September 1968)

CONCLUSION

It has been shown that the current through thermally grown silicon dioxide is electrode limited. All essential functional dependencies of the Fowler-Nordheim emission theory have been observed. Two discrepancies remain: The absolute value of the currents is low by up to one order of magnitude; this is probably related to the initial current drift. Second, the value of the effective mass m^* necessary to fit the temperature dependence is incompatible with the slope of the Fowler-Nordheim plot; this has not been satisfactorily explained. These results are believed to provide the most complete experimental examination of the Fowler-Nordheim emission theory reported to date.

Lenzlinger & Snow

A NEW FLASH E²PROM CELL USING TRIPLE POLYSILICON TECHNOLOGY

FUJIO MASUOKA, MASAMICHI ASANO, HIROSHI IWAHASHI, TEISUKE KOMURO and SHINICHI TANAKA

INTEGRATED CIRCUIT DIV. TOSHIBA CORP. KOMUKAI 1, SAIWAIKU, KAWASAKI 210 JAPAN

Control gate

Floating gate

Selection transistor

— IEDM 84

Masuoka et al.

FLASH 1984

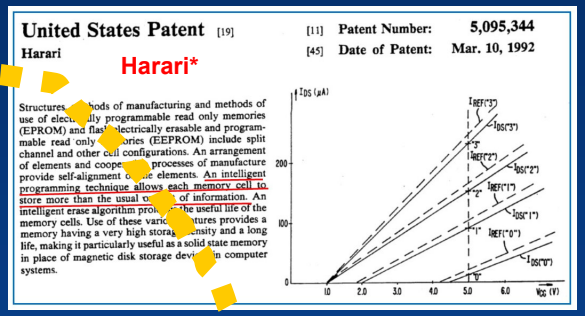
* FMS Lifetime Achievement Recipients

The Golden Thread of Tunneling

From Fundamental Physics to Technological Innovation (2)

Flash Memory Summit

MULTI-BIT
1992



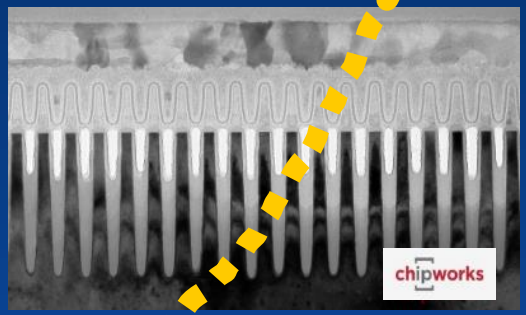
United States Patent [19]
Harari

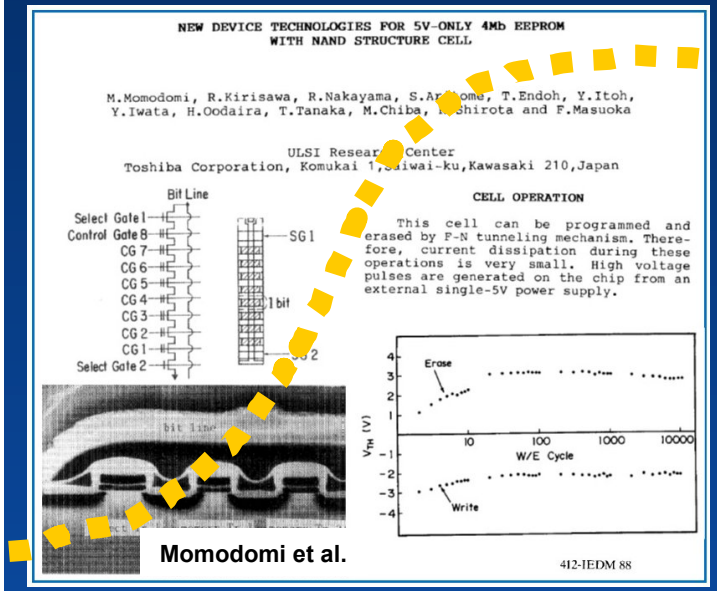
[11] Patent Number: 5,095,344
[45] Date of Patent: Mar. 10, 1992

Harari*

Structures and methods of manufacturing and methods of use of electrically programmable read only memories (EPROM) and flash electrically erasable and programmable read only memories (EEPROM) include split channel and other cell configurations. An arrangement of elements and cooperative processes of manufacture provide self-alignment of the elements. An intelligent programming technique allows each memory cell to store more than the usual one bit of information. An intelligent erase algorithm prolongs the useful life of the memory cells. Use of these various features provides a memory having a very high storage density and a long life, making it particularly useful as a solid state memory in place of magnetic disk storage devices in computer systems.

LIMIT of 2-D NAND FLASH
~2016





NEW DEVICE TECHNOLOGIES FOR 5V-ONLY 4Mb EEPROM WITH NAND STRUCTURE CELL

M.Momodomi, R.Kirisawa, R.Nakayama, S.Aritome, T.Endoh, Y.Itoh, Y.Iwata, H.Oodaira, T.Tanaka, M.Chiba, F.Shirota and F.Masuoka

ULSI Research Center
Toshiba Corporation, Komukai 1, Saiwai-ku, Kawasaki 210, Japan

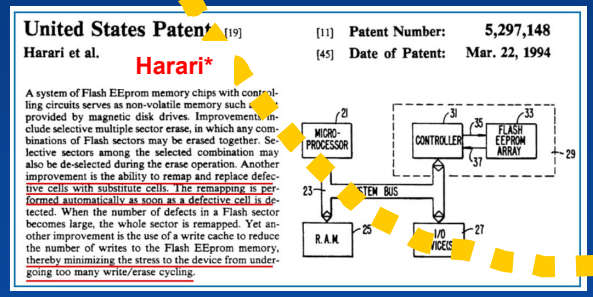
CELL OPERATION

This cell can be programmed and erased by F-N tunneling mechanism. Therefore, current dissipation during these operations is very small. High voltage pulses are generated on the chip from an external single-5V power supply.

412-IEDM 88

Momodomi et al.

NAND FLASH
1988



United States Patent [19]
Harari et al.

[11] Patent Number: 5,297,148
[45] Date of Patent: Mar. 22, 1994

Harari*

A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEprom memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.

SYSTEM FLASH
1994

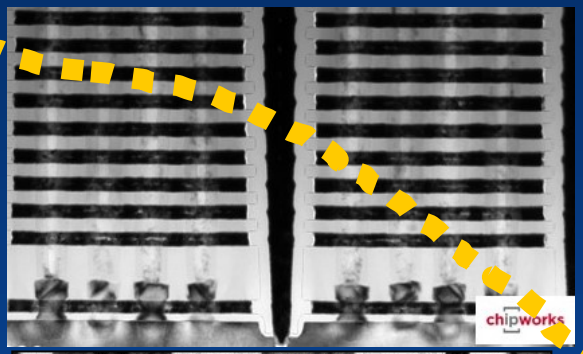
* FMS Lifetime Achievement Recipient

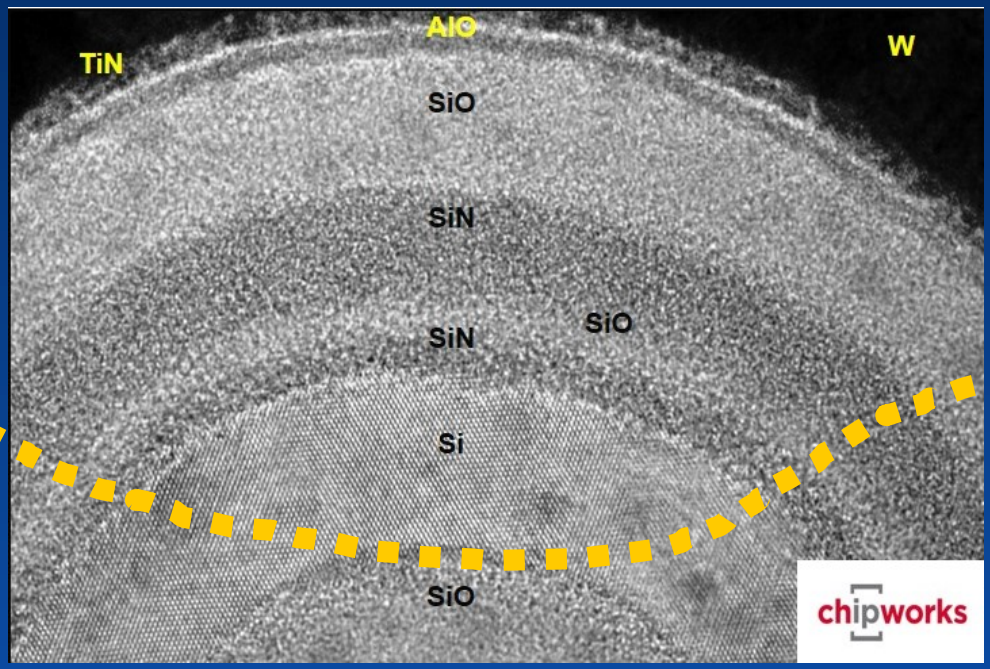
The Golden Thread of Tunneling

From Fundamental Physics to Technological Innovation (3)

Flash Memory Summit

Rise of 3-D NAND FLASH
> 2013





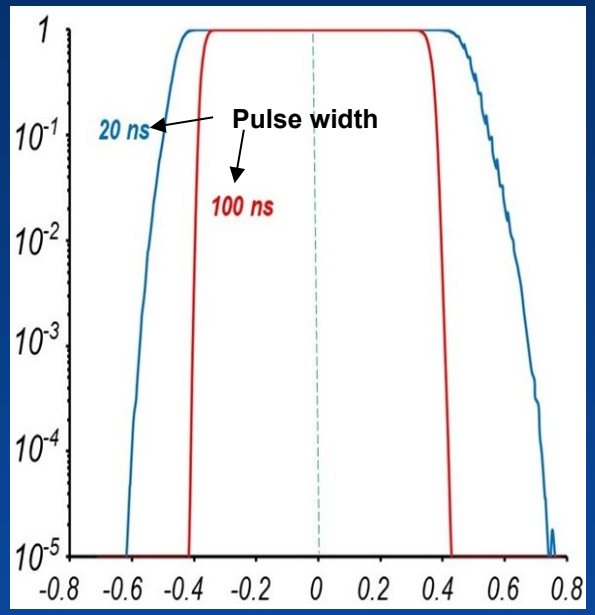
The Golden Thread Continues:
STT-MRAM: A Unique Tunneling Conundrum

Magnetic Tunnel Junction (MTJ)

Free layer	*CoFeB*
Tunnel barrier	*MgO*
Reference layer	*CoPt*

- ***Low Write Error Rate needs large tunnel current***
  - *Limits endurance due to oxide wear out mechanism*
- ***High endurance with low Write Error Rate needs reduced tunnel current***
  - *Make Free Layer magnetically less "stiff"*
  - *Reduce MTJ area*
  - *Use special design techniques (see "**The Engine**" presentation)*

The Stochastic "Top Hat"

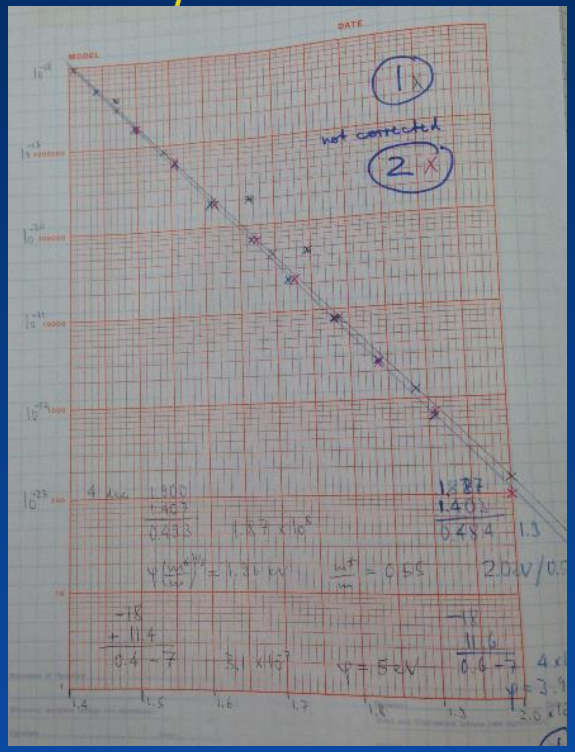


Spin Transfer Technologies
An Allied Minds Company

Tunneling Conclusions

- A long and illustrious history
- The foundation of many solid state memory technologies
- Creates damage and must be monitored
  - Circuits and systems can take advantage of the physics knowledge
- Continues to grow in importance:
  - 3-D NAND evolution
  - STT-MRAM
  - Other 3-D solid state memory approaches

Tunneling in Silicon Valley
Fairchild 1967-68



Lab Notebook #764
Martin Lenzlinger

Type ② characteristics seem to be temperature independent. (40)
fit a Fowler-Nordheim plot, resulting in reasonable values
for the $Si-SiO_2$ and $Al-SiO_2$ barrier height.
Conclusion: The current through the oxide is limited
by the tunneling injection.

Signature M. Lenzlinger Date Nov. 1, 67
Read and Understood (obtain two signatures):

DATE: January 25, 1968

LIST: xxx

R&D - D. Forsythe
A. Grove
T. Klein
G. Moore
R. Seeds
E. Snow
L. Vadasz

M.V - H. Blume
J. Kelley
P. Mogensen
G. Vashel
M. Wilder

Acknowledgements

- Eli Harari – Founder of SanDisk
- Dick James – Chipworks/TechInsights
- Malcolm Longair – University of Cambridge
- Thomas Boone – Spin Transfer Technologies
- Shustek Center at The Computer History Museum
- Cambridge University Press