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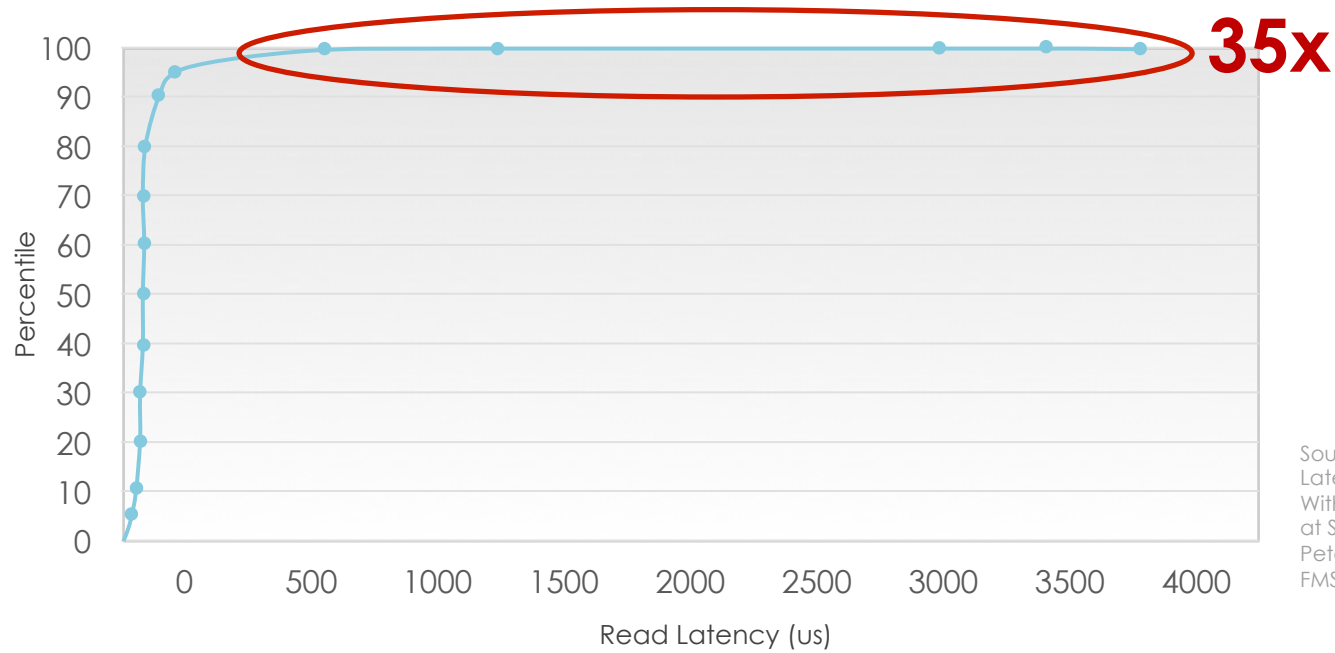
Data Persistence at Speed

Fast MRAM Write Buffers Make I/O Determinism Practical

Rizwan Ahmed
Everspin

IO Determinism is a Major Pain Point for Hyperscalers
Read Latency Challenge in Mixed Work Load

90% Random 4K Read, 10% 4K Write Latency Distribution

35x

Source: "Solving Latency Challenge With NVM Express SSDs at Scale" - Chris Peterson, Facebook. FMS 2017

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Current SSD Challenges That Can Be Addressed by STT-MRAM

Limited buffer size causes poor performance specifically QOS

Capacitors take too much board space limiting SSD capacity

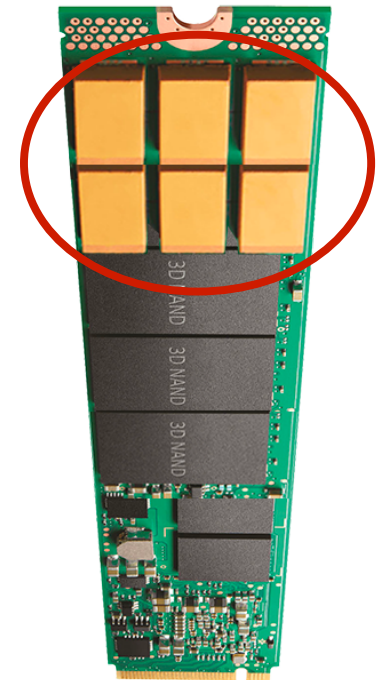**Capacitors are leading cause of drive failures**

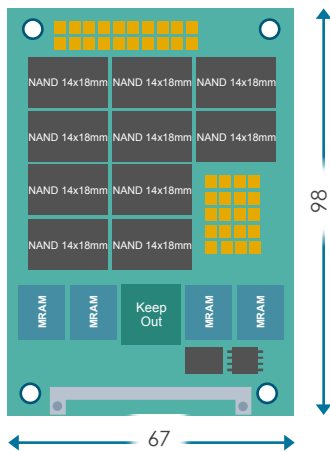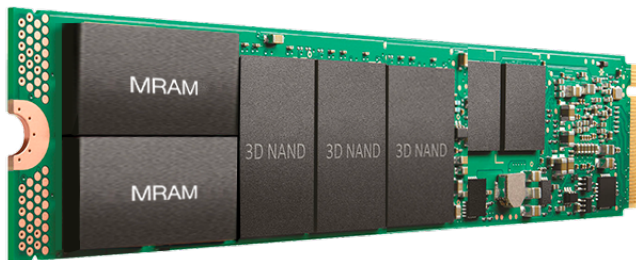**In 3D TLC, sequential read performance can be impacted if buffer size is small**

Longer time to market— PFail test is rigorous

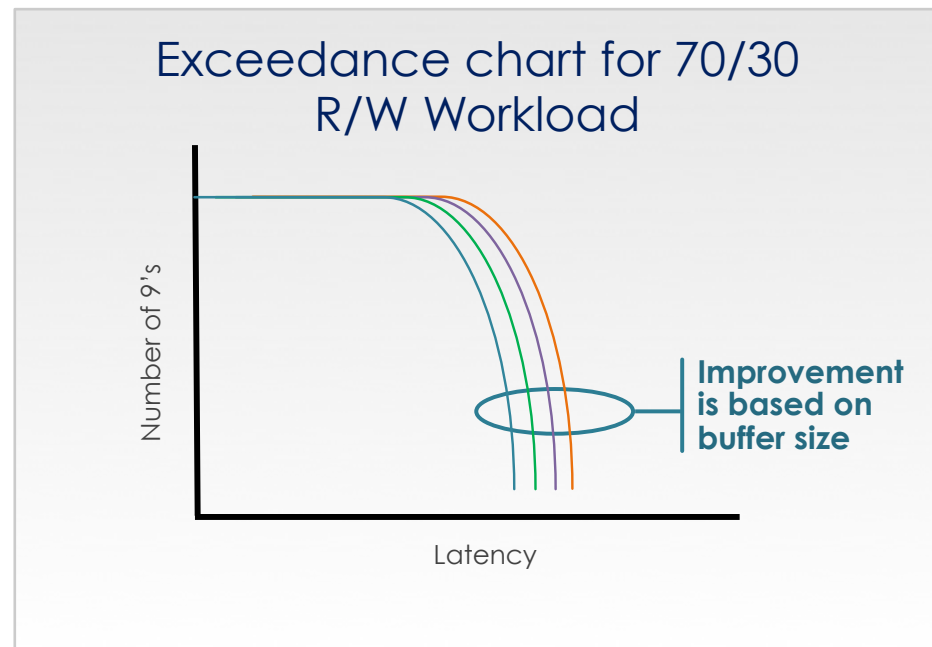**Customers want more streams for better performance & write amplification**

MRAM Enables Bigger Write Buffer

- Capacitors limit write buffer size

- Only 4-20MB write buffer size in typical enterprise SSDs

- STT-MRAM can provide 64MB or more write buffer size

- Up to 2 STT-MRAMs placement for M.2

- Up to 4 STT-MRAMs placement for U.2

Significant QOS Improvement Using STT-MRAM

- Mixed workload QoS is critical performance metric

- Host Reads are blocked by
  - Host writes
  - Garbage collection
  - Erase operations

- Bigger write buffer absorbs more writes

- Significant QOS improvement expected as a function of MRAM buffer size

Exceedance chart for 70/30 R/W Workload

Number of 9's

Latency

Improvement is based on buffer size

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Capacitors are Leading Cause of Drive Failures
STT-MRAM Improves Product Reliability

- Capacitors are #1 cause of drive failure

- Redundant caps needed to meet product life spec

- STT-MRAM eliminates the need for capacitors

- MRAM has higher temperature operating range (0c-85c)

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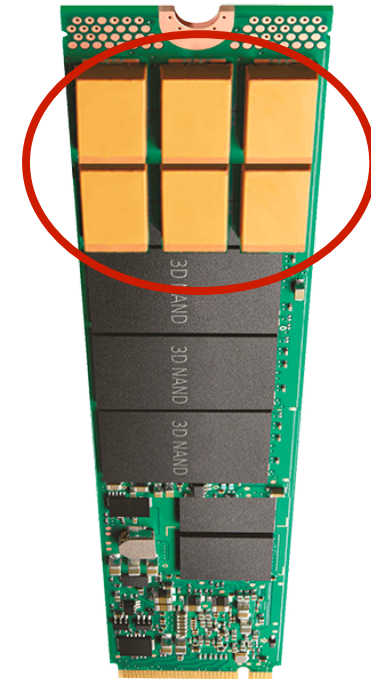
STT-MRAM Enables Higher SSD Capacity
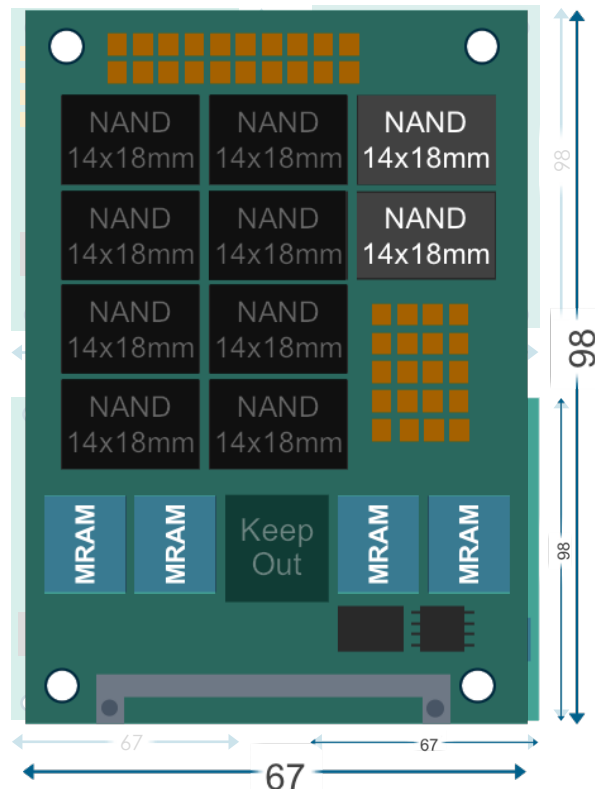
- Capacitors take up lot of board space

- Optimize board layout by removing capacitors

- Up to 4 additional NAND placements possible

- Up to 25% additional SSD capacity possible

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Faster Time to Market Using STT-MRAM
Study by Ohio State University and HP labs on "Robustness of SSD under Power Fault"

- Complicated code for managing power fail scenarios

- Lots of corner cases to validate

- Simplifying power fail code leveraging MRAM

- Leads to faster product qualification

Understanding the Robustness of SSDs under Power Fault

Mai Zheng[†]   Joseph Tucek*   Feng Qin[†]   Mark Lillibridge*
† The Ohio State University   * HP Labs

Abstract

Modern storage technology (SSDs, No-SQL databases, commoditized RAID hardware, etc.) bring new reliability challenges to the already complicated storage stack. Among other things, the behavior of these new components during power faults—which happen relatively frequently in data centers—is an important yet mostly ignored issue in this dependability-critical area.

This paper considers the behavior of SSDs[1] under fault. Specifically, we consider how commercially available SSDs behave when power is cut unexpectedly during operation. As SSDs are replacing spinning disk as the non-volatile component of computer systems, the extent to which they are actually non-volatile is of interest. Although loss of power seems like an easy fault to prevent, recent experience [18, 13, 16, 4] shows that a simple loss of power is still a distressingly frequent occurrence even

- Tested 15 drives from 5 different vendors
- 13 drives failed for power fault

Source: https://www.usenix.org/system/files/conference/fast13/fast13-final80.pdf

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STT-MRAM Improves Sequential Read Performance in 3D NAND

- 2D NAND to 3D NAND transition requires bigger buffer size

  - Upper & lower page programed together

- Data layout on NAND is not optimal with current buffer size

  - Sequential LBAs are written to upper and lower page

 - 2 NAND reads are needed to complete one host command
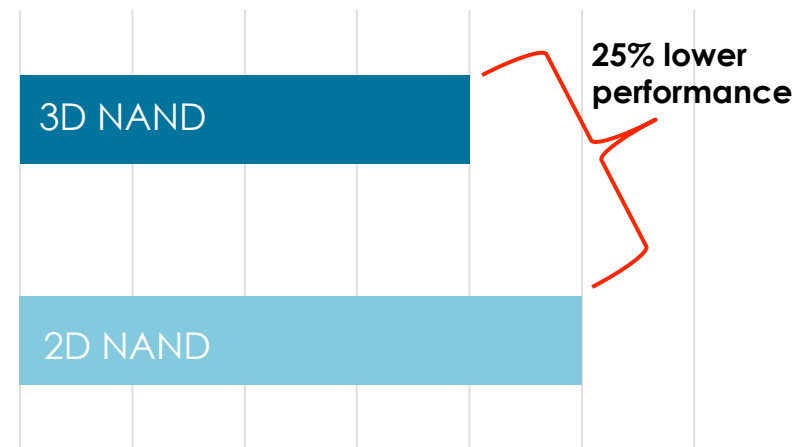
- Bigger NAND die capacity will continue to increase buffer size requirement

- 25-30% Sequential read improvement possible with optimal write buffer size

Sequential Read Performance (MB/s)

25% lower performance

3D NAND

2D NAND

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STT-MRAM Enables Higher Number of Streams Improving Performance & Write Amplification

- NVMe streams provide significant performance improvement

- Number of streams is limited by buffer size due to RAID/XOR operations

- Bigger buffer size can support more streams, resulting in better performance and WA
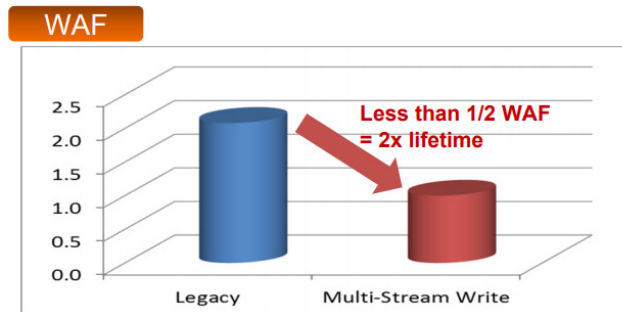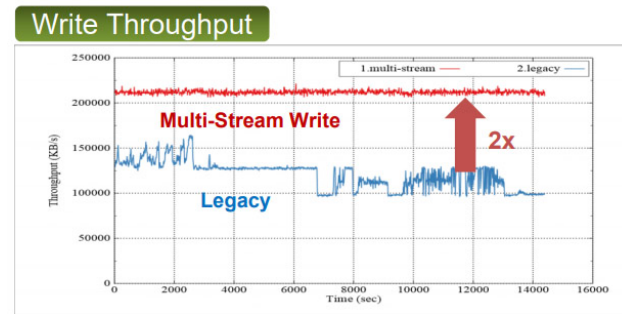
Source: "Multi-Stream Write SSD" - Changho Choi, Samsung. FMS 2016

IBM® Selected Everspin MRAM to Power Their FlashCore® Modules

Now Shipping in the IBM FlashSystem® 9100 Array

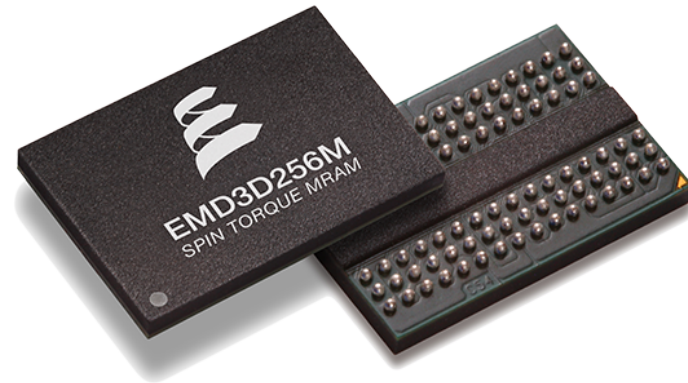https://developer.ibm.com/storage/2018/08/06/new-form-factor-ibm-flashcore/

SSDs with STT-MRAM will have:

Better QoS & seq. read performance

More reliable design

Higher capacity

Faster time to market

Available now

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Thank you.

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