

Testing Dual-Port NVMe SSD

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- What is Dual-Port NVMe?
- Dual-Port Functionality in NVMe
- Form Factors for Dual-Port NVMe
- Advantages of Dual-Port NVMe
- NVMe Dual-Port vs. SAS Dual-Port
- Testing Dual-Port NVMe



What is Dual-Port NVMe?

- Traditionally single x4 device is split into two x2 devices
 - Port A and Port B
- Methods to access the device:
 - Either Port A or Port B
 - Both Ports simultaneously
- Supported form factors:
 - U.2 (SFF-8639)



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Enterprise PCIe Pin Out

I							X	ΥL							
						L F									
Drive	Usage	Signal Description	Name	Mating	Pin #	Υ		-1		Pin #	Mating	Name	Signal Description	Usage	Drive
		Ground	GND	2nd	S1	- 9	- IP			E7	3rd	RefClk0+	ePCIe Primary RefClk +	ePCle	input
	CACICATA	SAS/SATA/SATAO O THE	SOT+ (A+)	2rd	62		- Ib			E8	3rd	RefClk0-	ePCIe Primary RefClk -	ePCle	input
input	SASTSATA	SAS/SATA/SATAE UTX+	301+ (A+)	Siu	32		10		Þ	E9	2nd	GND	Ground		
input	SAS+SATA	SAS/SATA/SATAe 0 Tx -	SOT- (A-)	3rd	S3	9	- IP	• •	Þ	E10	3rd	PETp0	ePCIe 0 Transmit +	ePCle	input
		Ground	CNID	204	64	- di	- Ib	. 41	Þ	E11	3rd	PETn0	ePCIe 0 Transmit -	ePCle	input
		Ground	GIND	2110			- IL	. 41	Þ	E12	2nd	GND	Ground		
output	SAS+SATA	SAS/SATA/SATAe 0 Rcv -	SOR- (B-)	3rd	S 5	9	18	' =	P	E13	3rd	PERnO	ePCIe 0 Receive -	ePCle	output
	CACLCATA	SAS/SATA/SATAS O Pout	50R+ (R+)	2rd	66		. Ib	• 9I	P	E14	3rd	PERpO	ePCIe 0 Receive +	ePCle	output
output	SASTSATA	SAS/SATA/SATAE U KCV +	30((+ (B+)	Siu	30		- IL		E	E15	2nd	GND	Ground		
		Ground	GND	2nd	S7					E16	3rd	RSVD	Reserved		
input	Dual Port	ePCIe RefClk + (port B)	RefClk1+	3rd	E1	-		- 11		S8	2nd	GND	Ground		
input	Dual Port	ePCle RefClk – (port B)	RefClk1-	3rd	E2	4	Þ	- 31			3rd	S1T+	SAS/SATAe 1 Transmit +	SAS+SATAe	input
input	ePCIe opt	3.3V for SM bus	3.3Vaux	3rd	E3	4	•	- 31		510	3rd	511-	SAS/SATAe 1 Transmit -	SAS+SATAe	input
input	Dual Port	ePCIe Reset (port B)	ePERst1#	3rd	E4	9	•			511	2nd	GND	Ground	CACICATA	-
input	ePCle	ePCIe Reset (port A)	ePERst0#	3rd	E5	9	•		E	<u>512</u>	3rd	51R-	SAS/SATAC 1 Receive -	SAS+SATAe	output
		Reserved	RSVD	3rd	E6					515	Jod	CND	SAS/SATAE I Receive +	SASTSATAC	output
input	SATAe	Reserved(WAKE#/OBFF),	RSVD(Wake#)	2	01	ď			6	514 E17	2110	RSVD	Recepted		
input	+SAS4	SASAct2	/SASAct2	Siu			- 10			F18	2nd	GND	Ground		
Bi-Dir	SATAe	SATAe Client /SAS reset	sPCIeRst/SAS	3rd	P2	4	- IP	' 41	Þ	F19	3rd	PFTn1/S2T+	ePCIe 1 /SAS 2 Transmit +	ePCIe+SAS4	input
							. Ib	•	Þ	E20	3rd	PETn1/S2T-	ePCIe 1 /SAS 2 Transmit -	ePCIe+SAS4	input
input	SATAe	Reserved (DevSLP#)	RSVD(DevSLP#)	2nd	P3		- IL	. 41	Þ	E21	2nd	GND	Ground		
output	SATAe +	Interface Detect	IfDet#	1st	P4	- 4	- IP	' 41	Þ	E22	3rd	PERn1/S2R-	ePCIe 1 /SAS 2 Receive -	ePCIe+SAS4	output
	ePCle	(Was GND-precharge)				- d	. Ib	9	P	E23	3rd	PERp1/S2R+	ePCIe 1 /SAS 2 Receive +	ePCIe+SAS4	output
	all			2nd	P5		- IL	. 9	P	E24	2nd	GND	Ground		
	all	Ground	GND	2nd	PG	- 4	- IF	• •	P	E25	3rd	PETp2/S3T+	ePCIe2 / SAS 3 Transmit +	ePCIe+SAS4	input
	an			2110					E	E26	3rd	PETn2/S3T-	ePCIe2 / SAS 3 Transmit -	ePCIe+SAS4	input
NC	SAS+SATA	Precharge		2nd	P7		- IL			E27	2nd	GND	Ground		
NC	SAS+SATA		5 V	3rd	P8	- 4	- IP	' 1		E28	3rd	PERn2/S3R-	ePCIe 2 / SAS 3 Receive -	ePCIe+SAS4	output
		SATA, SATAe, SAS only					- IÞ			E29	3rd	PERp2/S3R+	ePCIe 2 / SAS 3 Receive +	ePCIe+SAS4	output
NC	SAS+SATA			3rd	P9		- IL		E	E30	2nd	GND	Ground		
	all	Presence (Drive type)	PRSNT#	2nd	P10	4	- IF		E	E31	3rd	PETp3	ePCIe 3 Transmit +	ePCle	input
						- d	- IÞ			E32	3rd	PETn3	ePCle 3 Transmit -	ePCle	input
Bi-Dir	all	Activity(output)/Spinup	Activity	3rd	P11		- IL	. 41	Þ	E33	2nd	GND	Ground		
	all	Hot Plug Ground	GND	1st	P12	4	- IP	' di	Þ	E34	3rd	PERN3	ePCIe 3 Receive -	ePCle	output
							- IÞ		Þ	E35	Siu	РЕКрэ	ePCIe 3 Receive +	ercie	output
input	all	Precharge		2nd	P13		- IL	. 41	Þ	E36	200	GND	Ground	DCIa ant	Di Die
input	all		12 V	3rd	P14	- 4	- IF	' 41	Þ	E3/	2rd	SMDat	SM-Bus Clock	PCIe opt	BI-Dir Bi-Dir
input	all	All = 12V Only power for ePCIe SSD		2rd	D15	- q	- IP	9	P	E39	3rd	DualPortEn#	ePCIe 2x2 Select	Dual Port	input
mput	all	only power for er cie 550		Sru	-15										,
ePCle → Enterprise PCle (separate from SATA/SAS) SATAe → SATA Express			ſ	7	$\overline{\langle}$										
(Client PCIe- muxed on SATA/SAS signals)															
SAS4 → SAS x4															



Dual-Port Functionality in NVMe

- Dual-Port functionality can be enabled with DUALPORTEN# (E39)
- If DUALPORTEN# is left open, dual-port functionality is not enabled and device will be configured in x4
- If DUALPORTEN# is grounded, dual-port functionality is enabled and device is configured in dual x2



- Currently supported Form Factors:
 - U.2 (SFF 8639)
 - AIC
- New Form Factors:
 - EDSFF
 - NF1



Advantages of Dual-Port NVMe

- Dual Port provides failover capabilities
 - Ability to connect to two hosts simultaneously



NVMe Dual-Port vs. SAS Dual-Port

NVMe	SAS
No improvement in performance	Significant improvement in performance for read test (Read BW (simultaneous dual-port)) = 2x (non-dual port mode)
Provides failover capabilities	Provides failover capabilities
 Overall performance(NVMe PCIe Gen 3 x4): Read BW: ~3300 MB/s Read IOPS: ~800K 	 Overall performance (SAS-3) dual port mode: Read BW: ~1900 MB/s Read IOPS: ~270K Source: Toshiba
Form Factor: • U.2 (SFF 8639) • AIC	Form Factor: • U.2 (SFF 8639)

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Flash Memory Summit	ower On & Link Status of Dual-Po	ort (1/2)
• Link	Status display with Ispci	
\$ lspci \$ lspci ^	<pre>-s 0d:00.0 -vvv grep -A6 LnkCap</pre>	



• Link Status display with Advantest MPT3000 platform

~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~	
PCIe Port a Link	Status:
LinkUp L0 =	= true
LTSSM =	= 0x10, LTSSM LO
LinkWidth =	= x2
LinkSpeed =	= 8.0G
ActiveLanes =	= 00000011 (0x03)
ValidLanes =	= 00000011 (0x03)
LinkUpCount =	= 1
LinkRetrainCnt =	= 3
* * * * * * * * * * * * * * * * * * *	* * * * * * * * * * * * * * * * * * * *
* * * * * * * * * * * * * * * * * * * *	* * * * * * * * * * * * * * * * * * * *
PCTA Port h Link	Status.
LOIC LOIC D HINK	Status.
LinkUp L0 =	= true
LinkUp L0 =	= true = 0x10, LTSSM L0
LinkUp L0 = LTSSM = LinkWidth =	= true = 0x10, LTSSM_L0 = x2
LinkUp L0 = LTSSM = LinkWidth = LinkSpeed =	= true = 0x10, LTSSM_L0 = x2 = 8.0G
LinkUp L0 = LTSSM = LinkWidth = LinkSpeed = ActiveLanes =	= true = 0x10, LTSSM_L0 = x2 = 8.0G = 00000011 (0x03)
LinkUp L0 = LTSSM = LinkWidth = LinkSpeed = ActiveLanes = ValidLanes =	<pre>status. = true = 0x10, LTSSM_L0 = x2 = 8.0G = 00000011 (0x03) = 00000011 (0x03)</pre>
LinkUp L0 = LTSSM = LinkWidth = LinkSpeed = ActiveLanes = ValidLanes = LinkUpCount =	<pre>status. = true = 0x10, LTSSM_L0 = x2 = 8.0G = 00000011 (0x03) = 00000011 (0x03) = 1</pre>
LinkUp L0 = LTSSM = LinkWidth = LinkSpeed = ActiveLanes = ValidLanes = LinkUpCount = LinkRetrainCnt =	<pre>status. = true = 0x10, LTSSM_L0 = x2 = 8.0G = 00000011 (0x03) = 00000011 (0x03) = 1 = 3</pre>
LinkUp L0 = LTSSM = LinkWidth = LinkSpeed = ActiveLanes = ValidLanes = LinkUpCount = LinkRetrainCnt =	<pre>status. = true = 0x10, LTSSM_L0 = x2 = 8.0G = 00000011 (0x03) = 00000011 (0x03) = 1 = 3 ***********************************</pre>
LinkUp L0 = LTSSM = LinkWidth = LinkSpeed = ActiveLanes = ValidLanes = LinkUpCount = LinkRetrainCnt =	<pre>status. = true = 0x10, LTSSM_L0 = x2 = 8.0G = 00000011 (0x03) = 00000011 (0x03) = 1 = 3</pre>
LinkUp L0 = LTSSM = LinkWidth = LinkSpeed = ActiveLanes = ValidLanes = LinkUpCount = LinkRetrainCnt =	<pre>status. = true = 0x10, LTSSM_L0 = x2 = 8.0G = 00000011 (0x03) = 00000011 (0x03) = 1 = 3 ***********************************</pre>



Testing Dual-Port NVMe (Production Test Flow – 1/4)

- User can access one port at a particular point of time
 - Either Port A or Port B
- Complete LBA address range can be accessed from both ports



Testing Dual-Port NVMe (Production Test Flow – 2/4)





Testing Dual-Port NVMe (Production Test Flow – 3/4)

- Example Test Case:
 - Write to a particular LBA range using Port A
 - Read from the same LBA address range using Port B





Testing Dual-Port NVMe (Production Test Flow– 4/4)

- Checks if both Port A and Port B is functional
- Checks if same link rate can be negotiated on both Ports
- Part of Production Test Flow

Testing Dual-Port NVMeFlash Memory Summit (QA Test Flow – 1/4)

- User can access both ports simultaneously.
- Simultaneous Read: Both ports can access the same LBA address range
- *Simultaneous Write:* LBA address range should be exclusive to the ports.



Testing Dual-Port NVMe (QA Test Flow – 2/4)





Testing Dual-Port NVMe (QA Test Flow – 3/4)

- Example of Test Case (Simultaneous Write)
 - Write to exclusive LBA address ranges using Port A and Port B simultaneously.



Flash Memory Summit (QA Test Flow- 3/4)

- Example Test Case (Simultaneous Read)
 - Read from the same LBA address range using both Port A and Port B





- Checks if both ports can be accessed at the same time
- Checks if there is no performance degradation with simultaneous dual-port access
- Part of QA Test Flow



- Dual-port devices ensure redundancy and provides failover capability
- Provides ability to connect to two hosts simultaneously
- Used in Enterprise SSD market
- Current form factor is U.2



More Info: NVMe Dual-Port Testing

 Please visit us at Booth # 606 for to know more about NVMe Dual-Port Testing





Thanks