August 5, 2019

Welcome to the Conference/Event Overview
9:00 am – 9:15 am., Great America Meeting Room 2

Speaker: Barry Hoberman, MRAM Developer Day Conference Chair

Keynote #1 – MRAM Comes of Age as a Disruptive Technology
9:15 am – 9:55 am, Great America Meeting Room 2

Speaker: Kevin Conley, CEO, Everspin Technologies

Abstract: *MRAM is now coming into its own as a disruptive technology. With over 100 million units shipped, it has already brought unparalleled performance levels to many industrial applications over the last decade. Recent advances have led to STT-MRAM emerging as a practical technology for manufacturing. Visionary companies are using it today to create a new class of high-performance, low-latency storage systems. Demand for this technology in embedded SoC applications on leading-edge semiconductor processes has also led to major investments by foundries and manufacturing equipment companies to add it to their portfolios. Discrete STT-MRAM has recently broken the Gb density barrier, both reducing bit cost and increasing the range of applications. These are just the first steps in unlocking MRAM's disruptive potential for taking advanced computing architectures to new performance levels and meeting the need for simpler, smaller, and faster 5G-connected IoT devices.*

Keynote #2 – *New Development Tools Improve the Outlook for STT-MRAM*
9:55 am – 10:25 am, Great America Meeting Room 2

Speaker: Chang-Man Park, Director Advanced Technology, Tokyo Electron (TEL)

Abstract: *STT (Spin-Transfer Torque) MRAM offers excellent properties for a wide variety of applications, including embedded memory, cache memory, standalone memory, and storage-class memory. However, process difficulties remain in achieving the small write current, high MR ratio/low RA product, and high thermal stability required to take STT-MRAM into high-volume manufacturing. New process-vapor deposition (PVD) tools deliver much higher performance for forming complex multi-stack thin films. Process modules can be flexibly configured or added to accommodate applications at different stages from R&D to high volume production. The tools also offer great flexibility for new techniques such as perpendicular magnetization, and stability for wafer uniformity and tool marathon run performance.*

Keynote #3 – Challenges and Process Solutions for Scaling of STT MRAM
10:25 am – 10:55 am, Great America Meeting Room 2

Speaker: Mahendra Pakala, Managing Director, Memory Group, Applied Materials

Abstract: *With all major foundries offering STT MRAM technology at 40-22nm nodes, the development focus is now shifted to scaling beyond these nodes, and to enable newer applications by improving performance. Scaling typically requires reducing the RA of the MgO tunneling barrier while still maintaining the reliability of the device, as well as reducing the pitch of the bits in memory arrays with similar ppm level yields as demonstrated in current products. Some of the key issues and potential solutions, in terms of materials and process engineering of stacks, to achieve these goals are discussed.*

Plenary: State of MRAM Today – Annual Update
11:15 am – 11:45 am, Great America Meeting Room 2

Chairperson: Nilesh Gharia, CTO, Numem

Speaker: Barry Hoberman, Independent Consultant

Abstract: *MRAM is rapidly entering the marketplace with the widespread availability from Everspin of commercial 256 Mb and 1 Gb parts with initial design wins reported. Leading foundries such as TSMC, Samsung, Intel, and GlobalFoundries have announced that they will provide embedded MRAM for SoC designs. Accelerators, caches, SSDs, AI devices, and other applications have been reported. Market researchers have predicted large markets to come in enterprise storage, embedded systems including IoT, mil/aero, computer, and other applications.*

Plenary: State of MRAM Today – MRAM Technology and Market Trends
11:45 am – 12:15 pm, Great America Meeting Room 2

Chairperson: Nilesh Gharia, CTO, Numem

Speaker: Simone Bertolazzi, Engineer Analyst, Yole Developpment

Abstract: *MRAM has emerged as one of the most promising next-generation non-volatile memory technologies. In the embedded space, it holds potential for replacing eFlash (code/data storage) and SRAM (cache memory), which are facing severe challenges towards continuous improvement and miniaturization. Notably, all major foundries have been developing 28/22nm manufacturing processes with MRAM macros, and mass production of MRAM-based chips is now taking off. In this presentation, I will provide an overview of the spectrum of MRAM technologies, applications and markets. Moreover, I will discuss the latest developments in the MRAM business, highlighting the strategies and the challenges towards the establishment of a comprehensive MRAM ecosystem.*

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Track #1: MRAM Application Briefs
2:00 pm – 3:15 pm, Great America Meeting Room 1

Chairperson: Tom Coughlin, President, Coughlin Associates

Speakers:

- *Krishna Thangaraj, Memory Development Engineer, IBM, Using MRAM in High-Speed Enterprise Storage Caches*
- *Pankaj Bishnoi, Director Applications, Everspin Technologies, "Using MRAM to Enable Power Loss Protection for NVMe"*
- *Jeff Lewis, VP Business Development, Spin Memory, "Enabling the Next Generation of IoT Edge Device Using MRAM"*
- *Brent Yardley, Sr Technical Staff Member/Master Inventor, IBM Systems, "Making MRAM Work in Actual Applications"*

Abstract: *MRAM is here today. Applications reported include accelerators, caches, SSDs, mil/aero systems, IoT, and embedded systems. Many others are expected as MRAM's characteristics (high speed, long lifetime, fast writes, and low power) become better known. Brief descriptions of current or proposed applications should help designers understand how MRAM will fit into their storehouse of useful components.*

Track #2: Embedded MRAM
2:00 pm – 3:15 pm, Great America Meeting Room 3

Chair: Dave Eggleston, Principal, Intuitive Cognition Consulting

Speakers:

- *Danny Sabour, VP Marketing, Avalanche Technology, "Generic Interface for High Performance Embedded MRAM"*
- *Tetsuo Endoh, Professor, Tohoku University, "IoT and AI Applications of Embedded MRAM"*
- *Nicholas Hendrickson, Director, Numem, "A 22nm 20Mb Embedded MRAM with 5Gbps Read and 1Gbps Programming"*
- *Martin Mason, Sr. Director Leading Edge eNVM, Global Foundries, "e-MRAM Technology is Here Today for Many Embedded Applications"*

Abstract: *Embedded MRAM is a key IP block, now readily available from multiple foundries for SOC and MCU designers to incorporate into their chips. With eMRAM reliability solidly established for broad consumer and industrial markets, the industry's current focus has turned to performance enhancement of the bitcell and macros. In achieving nanosecond speed reads and writes, eMRAM enables new features in AI and IoT chips far beyond simple code storage. eMRAM IP designers are pushing the performance boundaries, and enabling new features in novel applications.*

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Track #1: MRAM Development
3:30 pm – 4:45 pm, Great America Meeting Room 1

Chairperson: Jeff Lewis, VP Business Development, Spin Memory

Speakers:

- *Andre Dais, Head of Development, Hprobe, "UltraE-Fast Testing Up to 2 Tesla of Full Stack MRAM"*
- *Suhail Zain, Sr Director Marketing, Avalanche Technology, "Developing Successful MRAM Chiplets"*
- *Tomasz Brozek, Project Leader/Fellow, PDF Solutions, "Short Loop Characterization and Tracking System for MRAM Process Development"*

Abstract: *MRAM technology has emerged to offer the benefits of low latency, high endurance, and persistence. Hardware and software designers can now realize the benefits of this technology. This session will focus on how MRAM technology is progressing to allow for more applications. We will also present the latest advances in MRAM testing, chiplets, and process development.*

Track #2: MRAM in AI/ML Applications
3:30 pm – 4:45 pm, Great America Meeting Room 3

Chairperson: Simone Bertolazzi, Engineer Analyst, Yole Developpement

Speakers:

- *Tom Coughlin, President, Coughlin Associates, "How MRAM Fits in AI Applications"*
- *Michail Tzoufras, Staff Engineer, Spin Memory, "Leveraging MTJ Stochasticity in AI Architectures"*
- *Terry Torng, Sr VP Engineering/Co-Founder, GyrFalcon Technology, "Using MRAM in Inference Engine Applications"*

Abstract: *MRAM appears to have a bright future in AI/ML applications due to its high speed for both reads and writes, low power consumption, and long lifetime. MRAM caches can support large AI models or multiple AI models, avoid the need for expensive battery backup, and provide high throughput in both training and execution phases. Models supported include neural networks, deep learning systems, and inference engines. Recent advances in reliability and power consumption are particularly promising.*

Panel on MRAM in 2024 and How We Got There
5:00 pm – 6:00 pm, Great America Meeting Room 2

Chair: Satoru Araki, Sr. Director Product/Program Management, Spin Memory

Panelists:

- *Mark Webb, President, MKW Ventures*
- *Daniel Worledge, Distinguished Research Staff Member/Sr Manager MRAM, IBM Research*
- *Terry Torng, Sr VP Engineering/Co-Founder, GyrFalcon Technology*
- *Tetsuo Endoh, Professor, Tohoku University*
- *Tom Andre, VP Engineering, Everspin Technologies*
- *Jean-Pierre Nozieres, CEO, Antaios*

Abstract: *When we look back from 2024, what will we see? Surely a large MRAM market in the hundreds of millions of dollars. We will see much larger parts than we have today and far more applications. We will also see MRAM as a standard component in the toolboxes of memory designers in a wide variety of application areas. Our look forward will be along two axes, one being applications (e.g., SRAM, AI, unified, automotive, and persistent memory) and the other being performance (e.g., retention, endurance, cost, scalability, and power consumption)*.

Networking Reception
6:00 pm – 8:00 pm, Great America Meeting Room Foyer

Join MRAM Developer Day sponsors Everspin Technologies, Global Foundries, Hprobe, Integral Solutions International, and Numem to view their product demonstrations and to network with colleagues while enjoying appetizers and beverages.