MRAM Developer Day 2019
MRAM Update

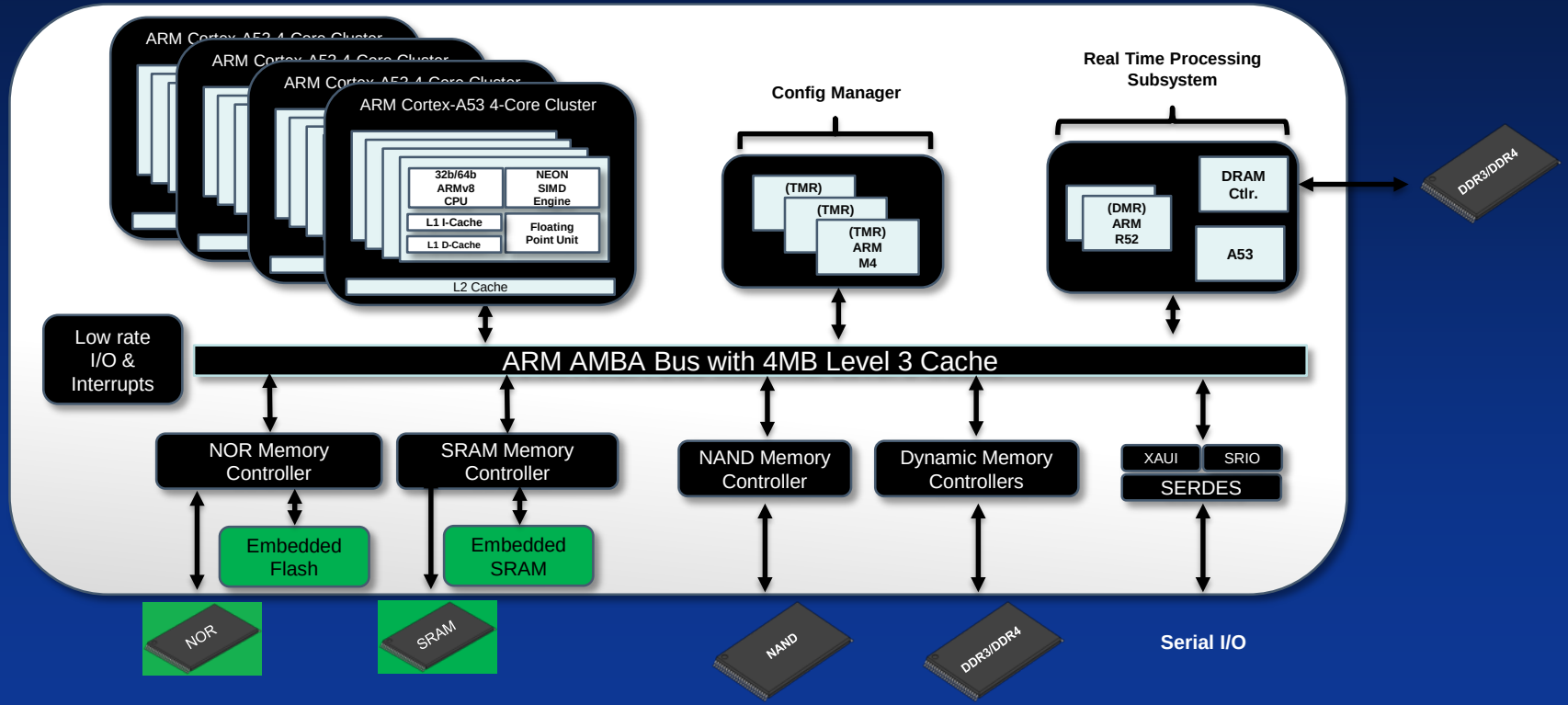
Danny Sabour
VP of Marketing & Business Development
Avalanche Technology

Generic MRAM Interface

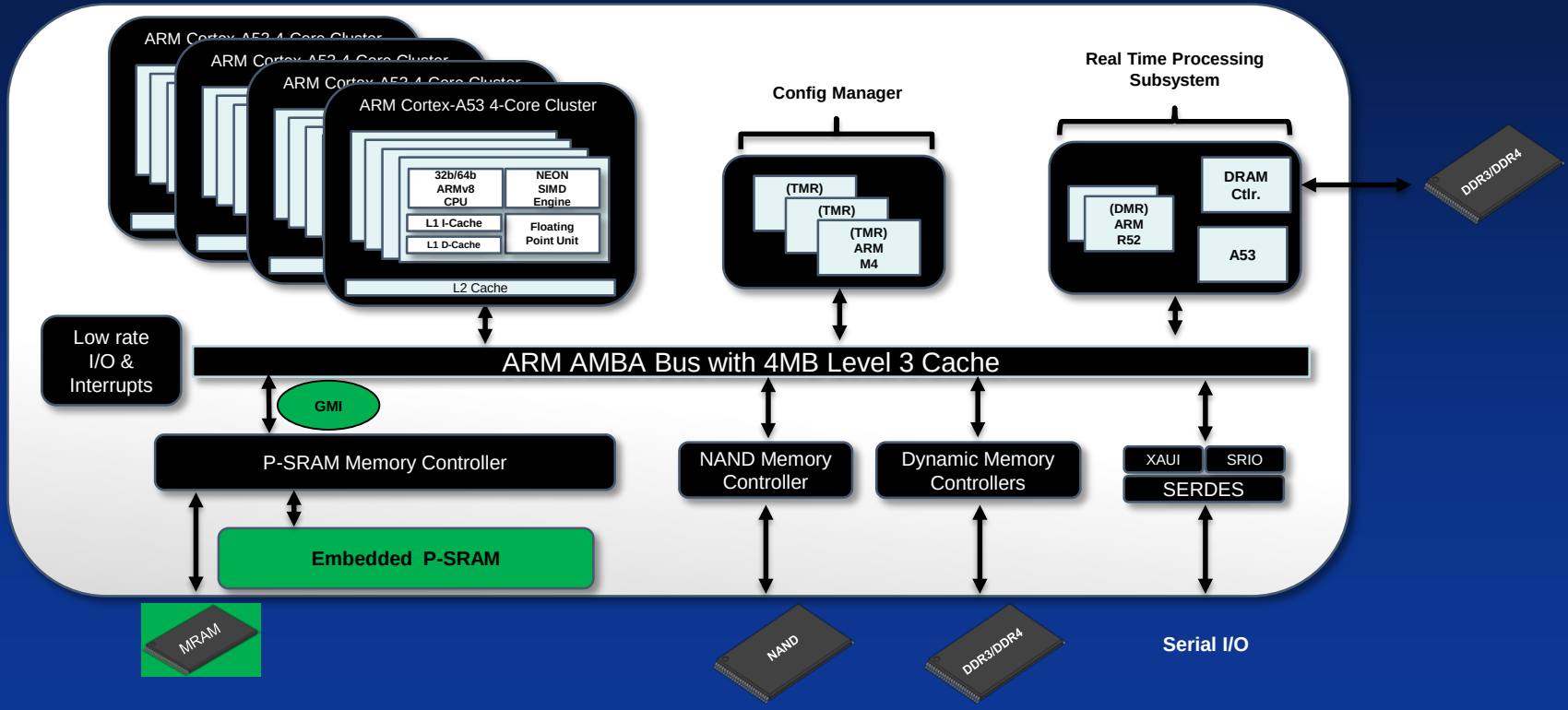
ABSTRACT: Avalanche Technology offers embedded MRAM (eMRAM) macros for embedded SRAM and embedded Flash applications in SoCs. To facilitate integration and reusability with different processes, a Generic MRAM Interface (GMI) is being proposed. GMI is a point-to-point connection and is used for accessing the MRAM resources.

This session will describe how Avalanche's GMI is one of the first steps needed for mass adoption of MRAM

High Performance Computing



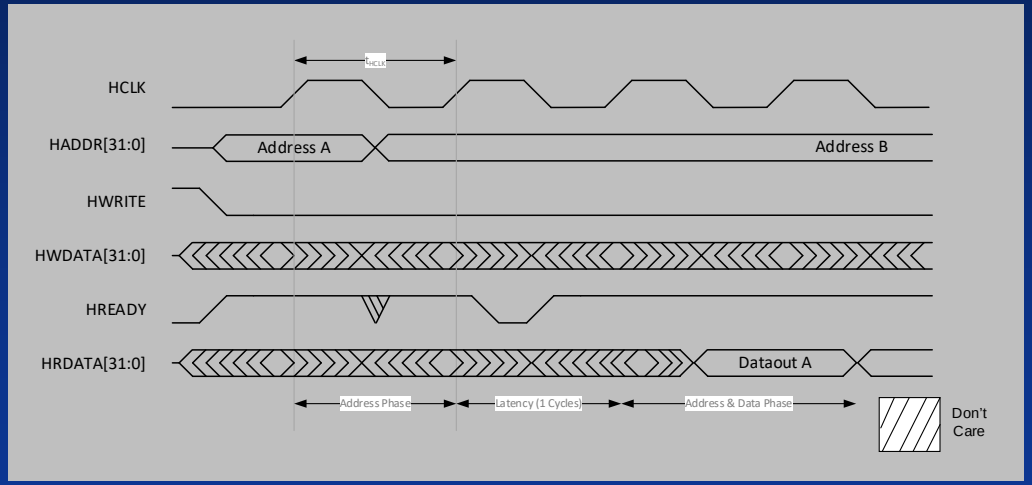
High Performance Computing with GMI

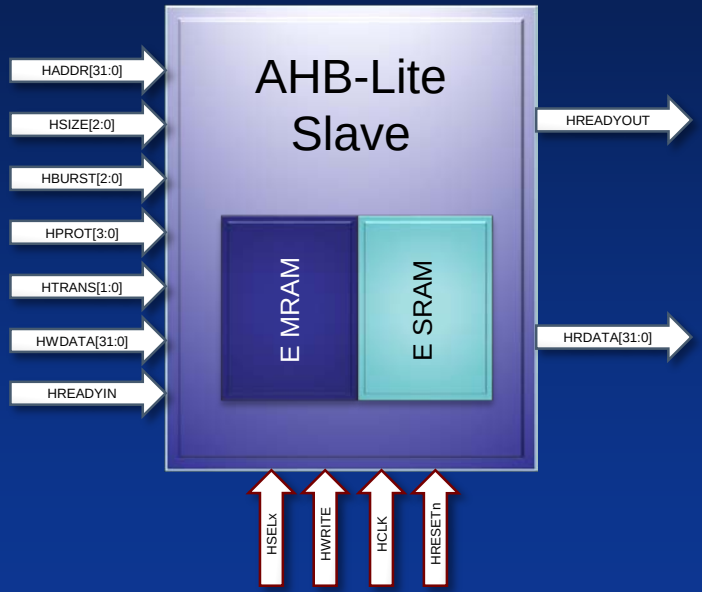


Simplifying the system : Phase 1: MRAM replaces SRAM & NOR Flash

Phase 1: Removing the Flash Ctlr.

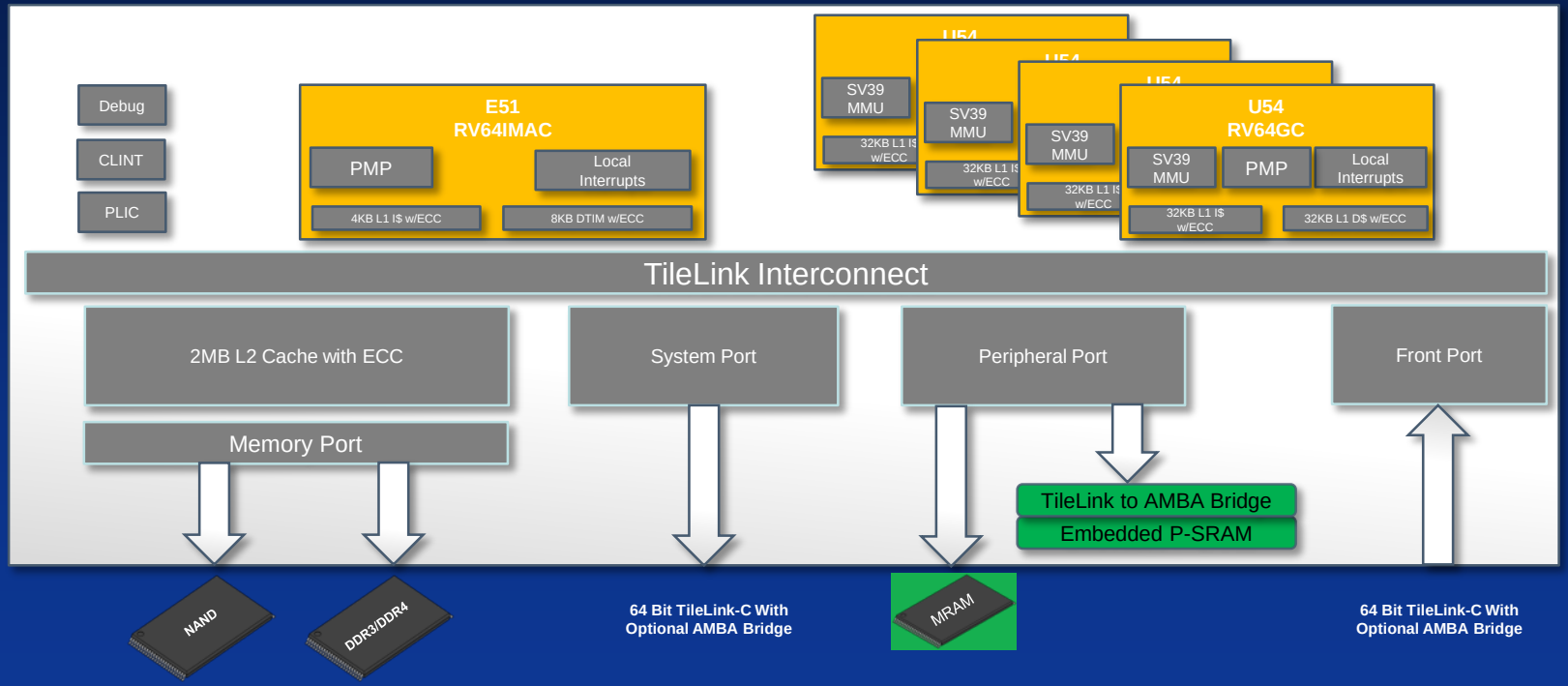
- No longer need to manage the Flash memory array
- Generic Embedded MRAM Interface (GeMI) is a point-to-point connection between a single master and a single slave MRAM
- One common block connects directly to the AMBA AHB-Lite bus





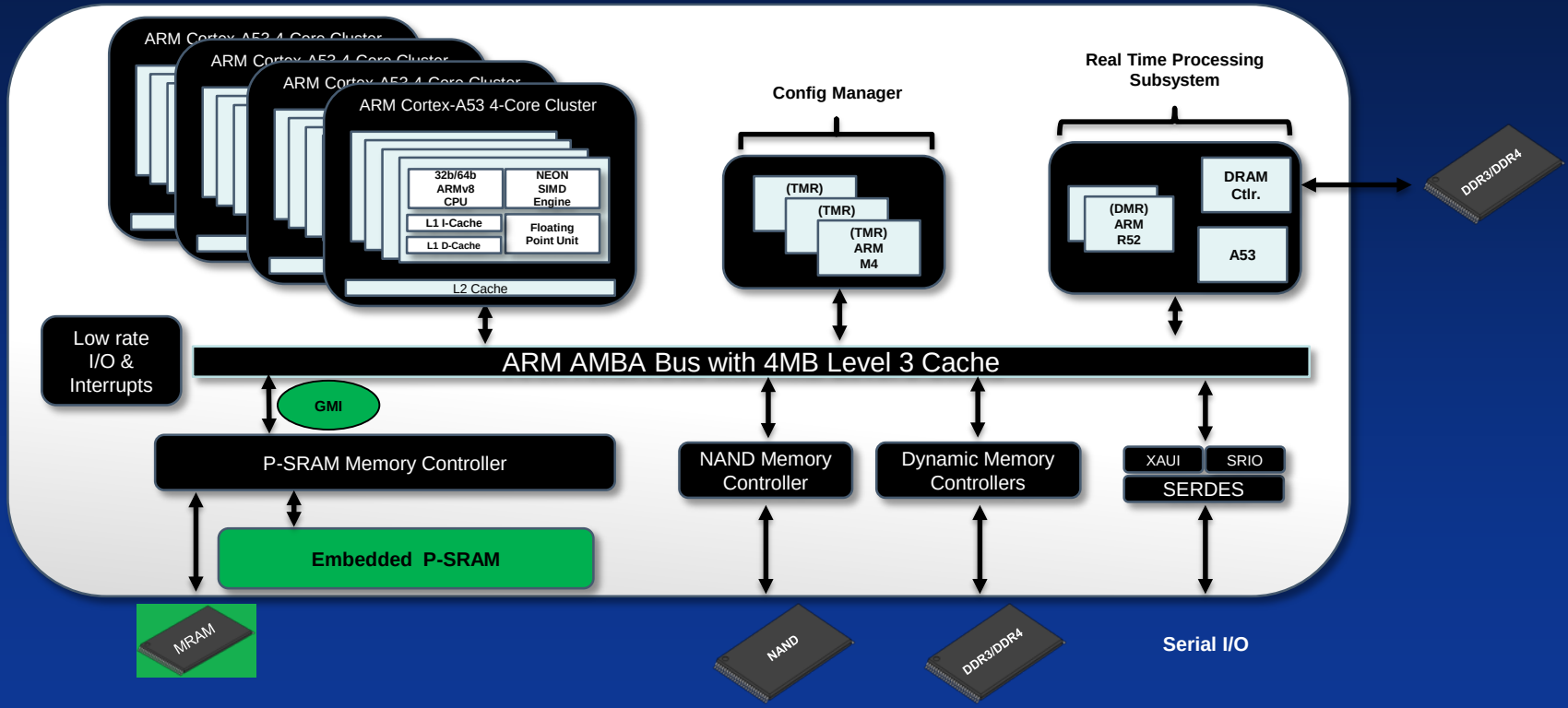
Goal: Transportability between foundries

High Performance Computing: RISC V

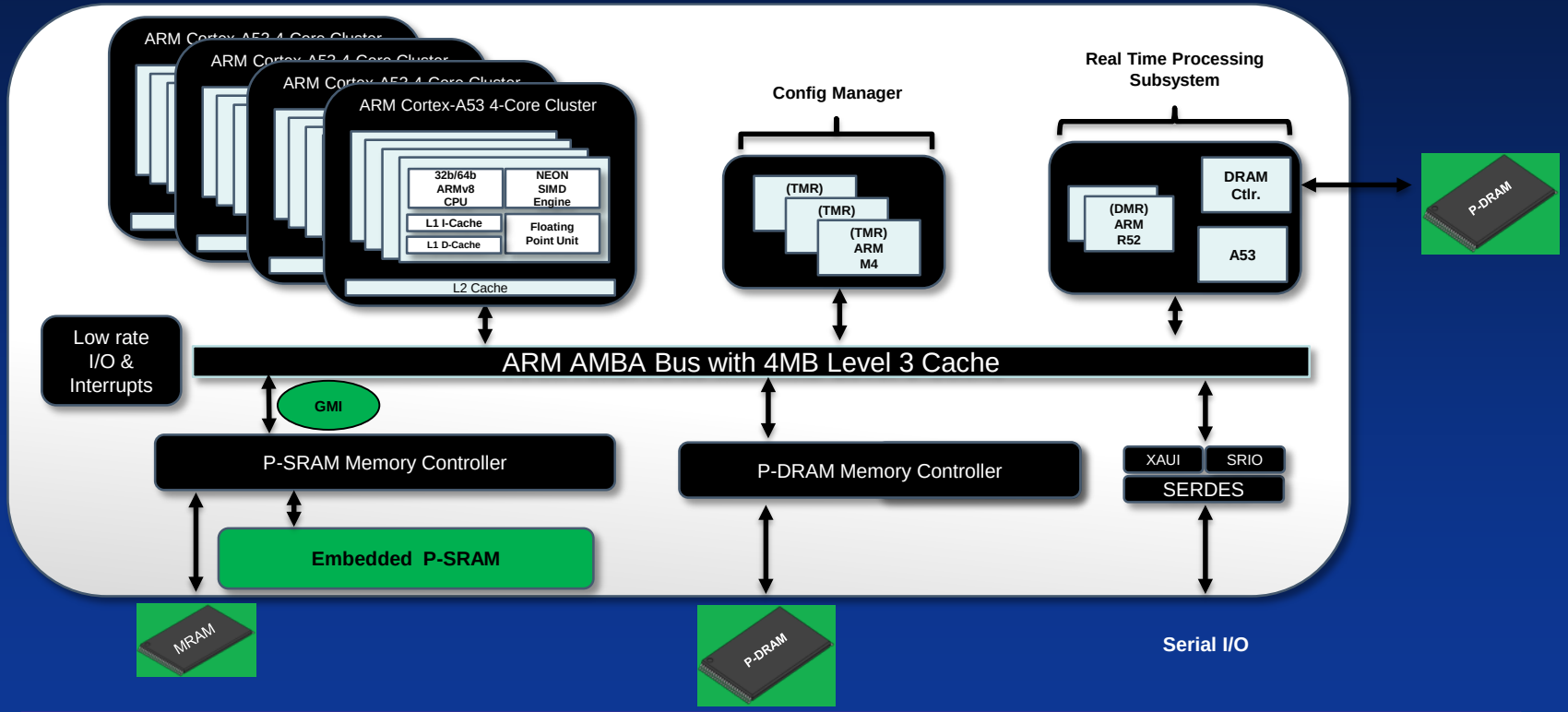


TileLink bridge to AMBA bus is the quickest way to assure interoperability

High Performance Computing



High Performance Computing



Simplifying the system : Phase 2: MRAM replaces DRAM and NAND

Mass adoption of MRAM

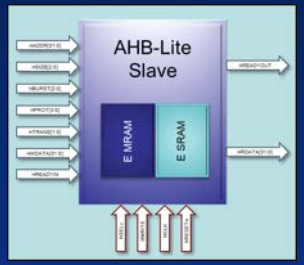
MRAM can replace SRAM and NOR Flash <u>today</u>

By 2021, MRAM can replace DRAM and NAND Flash

The phases of making it seamless for OEMs :

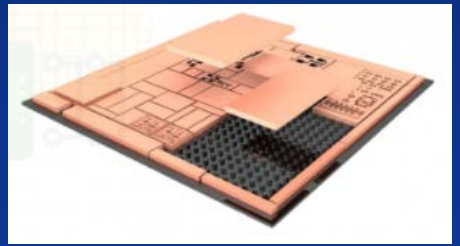
1. **Make designs that work with multiple architectures: ARM and RSIC-V (GMI)**
2. **Make designs that the community can grow on its own (Open standards)**

Samsung	Internal IP acquired from Grandis
TSMC	Internal IP developed from solution by TDK
UMC	Avalanche Technology
GF	Everspin



www.Avalanche-Technology.com/E-SRAM

3. **Make designs that work across multiple foundries:**
   - **Chiplet-based MRAM solves the transportability between foundries**



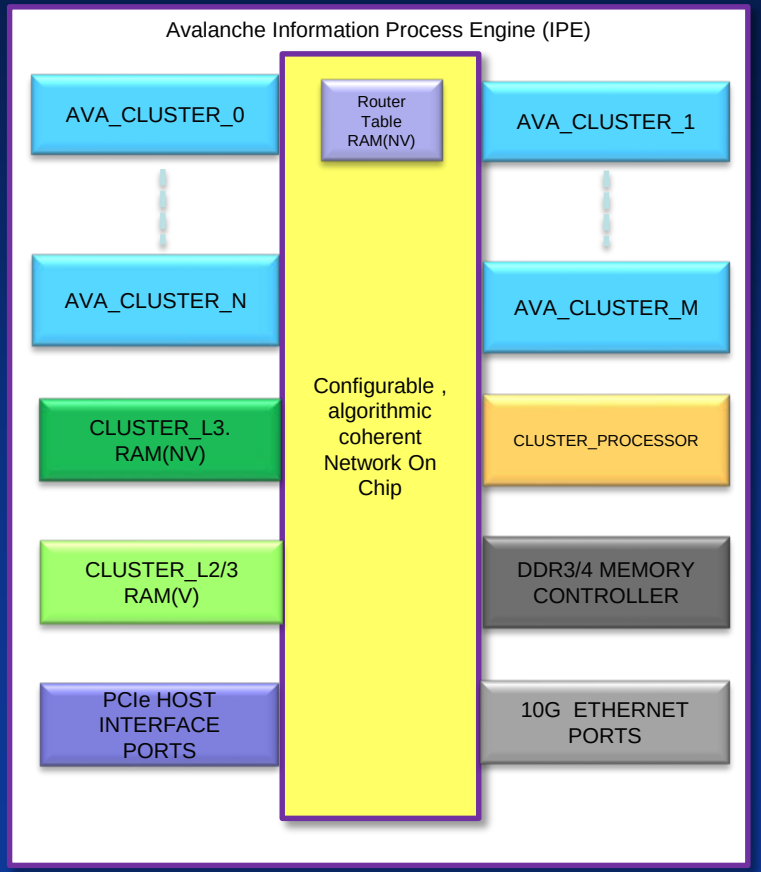
MRAM will take its rightful place in the system

MRAM DEVELOPER DAY

Application of MRAM:
Avalanche Information Processing Engine

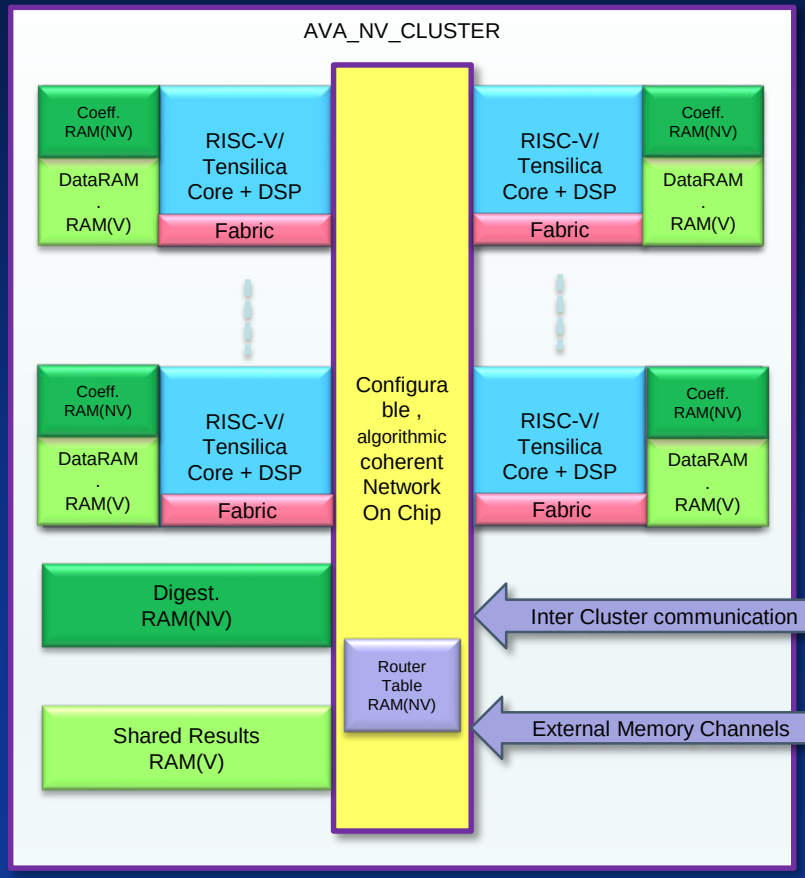
Ava Information Processing Engine

- **AVA_CLUSTER_X**
  - Hardware implementation of CNN/RNN/..
- **Cluster Processor**
  - Configures Cluster Network
  - Supports CNN Compiler
  - Tensor Flow Compiler
  - Adaptive Learning
- **External Communication Ports**
  - Scalability and distributed processing
  - Inter chiplet Communication
- **Memory Controller: DDR3/4**
- **L2/L3 Cache : Code & Data**
  - L2: SRAM (P-SRAM)
  - L3: Embedded STT-MRAM (P-SRAM)



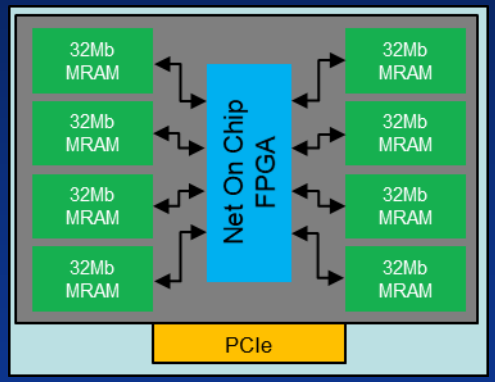
Ava_Cluster

- **Configurable Cluster Size**
  4x4; 8x8; …
- **Processing Element**
  MAC: Multiply, Accumulate, …
  State Machine
  Code and Data RAM
    Code & Coeff RAM
    Coeff is Constant
    LUT: Translation Operation
- **Single Cycle Configurable Execution**



Summary

- **Information Processing Engine using P-SRAM for Neuromorphic Computing**
  - Simpler and scalable than proposed Compute-in-Memory(CIMs)
  - Comprise of scalable Clusters
  - Low latency Network-on-chip
- **First demonstration of Key component via Chiplet**
- **Chiplets itself can be used as an AI-accelerators**
- **Advanced design for Network-on-chip**
  - For IoT Application
  - Especially for low-power mobile applications such as, AI on drones, AI on satellites, etc.



MRAM as a Chiplet or Embedded is the key ingredient of a learning IoT SoC

MRAM DEVELOPER DAY

Thank You