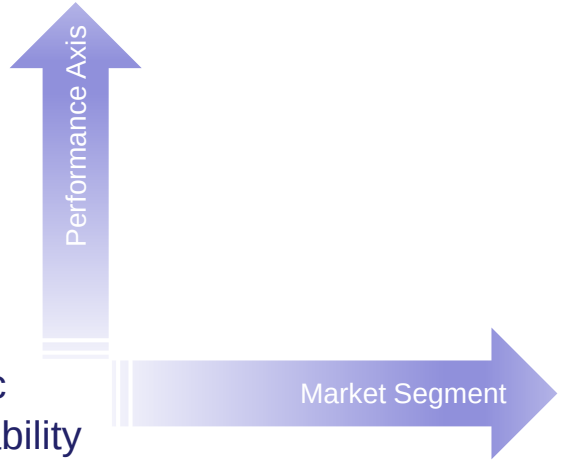
MRAM Applications – Pros/Cons

- Panel Discussion — Chair: Satoru Araki
- Goal: Discuss upcoming MRAM Applications in Two Axes: Market and Performance
- Panelists:
  - Mark Webb, President MKW Ventures
  - Daniel Worlege, Distinguished RSM, IBM Research
  - Terry Torng, Co-Founder, GyrFalcon
  - Tetsuo Endoh, Prof. Tohoku Univ
  - Tom Andre, VP Engineering, Everspin
  - Jean-Pierre Nozieres, CEO, Antaios
- Two Domains:
  - Market segments – NVM / Unified / SRAM / AI / Auto, etc
  - Performance axis – Retention / Endurance / Cost / Scalability



- What is the main Market for MRAM in 2024?
- What are the Pros/Cons in Performance?

Panelist Views 2019

		Mark	Daniel	Terry	Endoh	Tom	Jean-Pierre
Market	Target Market	▪Embedded, SOC, NOR/SRAM replacement	▪eNVM @ 105C ▪eNVM @ 125C, solder reflow ▪Mobile cache (10 ns) ▪Last level cache	▪Edge AI and IoT, AI for Robot and AI for automotive	▪e-Memory (SRAM & e-Flash replacement) ▪NV-Logic for IoT, Mobile, Car Electronics, Robot, AI	▪Entry: Storage (SSD) ▪Next: Industrial, Auto, Aerospace	▪ Immediate: IoT (battery-operated, ex. Data logging) ▪Near :Automotive / AI
Performance	Pros	▪Ability to support DRAM, NOR, SRAM applications ▪ storage in metal layers	▪eNVM @ 125C with solder reflow is doable now ▪Mobile cache at 10 ns is doable now	▪Non volatile , no leakage ▪Memory density ▪Scalability ▪Potential universal memory	<SRAM replacement> ▪ Low Power ▪ Small Cell Size <e-Flash Replacemt> ▪ Low Power ▪ Small Cell Size ▪ Better Endurance ▪ High Speed Write	▪High bandwidth non-volatile writes ▪High Endurance ▪Reliability ▪ST-DDR4 Interface	▪Fast and non volatile ▪Huge power savings at chip level
	Cons	▪Maturity in embedded applications ▪Cost/Scaling	▪Last level cache is very hard –reliable 2 ns write with low current ▪MRAM will never be SCM – no multi-bits	▪SRAM like ns Read/write speed for some application ▪SRAM like endurance or better for some application	<SRAM replacement> ▪ Endurance ▪ Write Power ▪ Cost <e-Flash Replacemt> ▪ Retention@HT ▪ Cost	▪Density < DRAM ▪Ind/Auto grades not yet avail ▪Clock Freq < DRAM	▪Endurance-speed-retention trilemma ▪Heavy ECC required ▪Limited read speed ▪STT is not RAM compatible as is
Action Needed		▪Demonstrated volume in production ▪Achieve Cell size <20 F^2	▪Develop new materials/device for reliable 2 ns write with low current	▪SRAM like performance ▪MLC MRAM ▪Next-gen MRAM, SOT, VCMA	▪Adv.Process Tech, High throughput ▪ECC Tech ▪Testing Tech	▪MTJ Scaling and Design to extend temp and improve power/perf/area	▪Achieve speed AND endurance at the same time – SOT ! ▪Improve read margin to raise read speed

2019 MRAM Markets and Applications

Mark Webb

MKW Ventures Consulting, LLC

8/5/2019

MRAM Future and Challenges

- MRAM technology is here today
  - We know what it is and what the challenges are
  - Cost, Performance, Density, Endurance, SOC integration, etc
- In past year, we have updates on multiple fronts
  - Existing companies announced 1Gbit parts, updated us on revenue and growth
  - Multiple Companies presented embedded MRAM technologies
    - IEDM/ISSCC Papers were popular. Embedded is an option to choose
  - New technologies and models and optimization
- No need to speculate on what is coming

A Tale of Two Markets

- Embedded: MRAM is ideal for market (revenue not measurable)
  - Potential to replace NOR, SRAM, DRAM applications
  - Ability to integrate (metal stacks), density (Mbit), performance (DRAM) match embedded needs well
  - Endurance work needed for full RAM replacement
  - Looks like Embedded “Universal Memory”… Why isn’t it here already?
- Discrete: Targets and Market growth uncertain (Rev <$100M today)
  - Target applications requires specific density, speed, with NVM requirement.
  - Small markets exist, but they are vulnerable to attack on all sides.
  - No measurable NAND replacement market (Too small, expensive)
  - Performance/cost/density ratio not on track to match DRAM
  - Needs to dominate Niche or have “Killer App”

Revenue Projections for MRAM

- In 2018 we predicted >$900M in Revenue by 2024
  - This will not happen
  - 2018/2019 did not breakout like we hoped/expected

	MRAM Revenue Baseline	Notes/required milestone
2020	$115M	1Gb selling for revenue in 2020, DRAM-Like performance. Multiple IP sources for foundries
2022	$217M	Multiple foundries and 1+ Memory company in volume
2024	$429M	2+ memory companies in volume

Included discrete chips (may be stacked) and revenue from licensing
Does not include embedded memory (no revenue model)

What is Needed to meet Revenue by 2024 (Forecast=$429M)

- ALL MRAM: Volume production in applications in 2020
  - These are required to allow people to commit the technology to significant products.
- Embedded: Multiple foundry support with multiple applications
  - MRAM penetration into market is measureable in 2020
  - MRAM becoming chosen technology in 2022 designs
- Discrete: Meet aggressive endurance goals, Cell size Goals, Density roadmaps and Cost
  - To have any penetration into larger markets, confidence needs to increase in delivering specs.
  - MRAM is unique enough to not allow easy “backup plans”, so high confidence is needed

- More details on MRAM vs other memories in my memory update on Tuesday
- Mark Webb, www.mkwventures.com

MRAM Developer Day

Panel Discussion

Daniel Worledge

IBM Research

Senior Manager, MRAM

Key Advances in Spin-Transfer-Torque MRAM

Device

1974

Slonczewski (IBM) invents magnetic tunnel junction.

1995

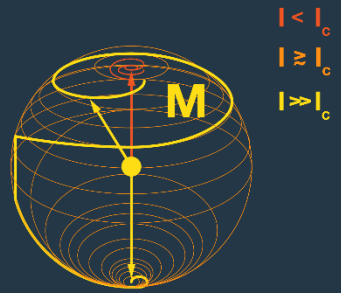
Moodera (MIT) and Miyazaki (Tohoku U.) demonstrate first room temperature magnetic tunnel junctions.

Magnetic Tunnel Junction

Write

1996

Slonczewski (IBM) invents spin-transfer-torque switching.

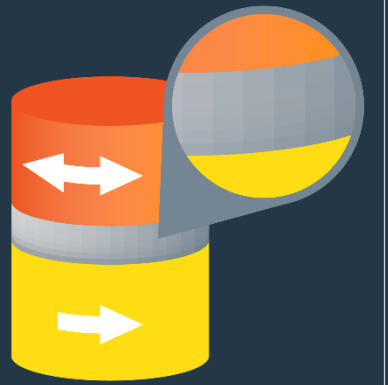


Spin Transfer Torque

Read

2004

Parkin (IBM) and Yuasa (AIST) publish discovery of high magneto-resistance in MgO tunnel junctions.

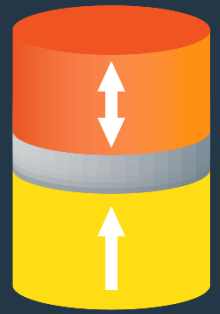


MgO Tunnel Barriers

Scaling

2010

Worledge (IBM) and Ohno (Tohoku U.) demonstrate first perpendicular CoFeB tunnel junctions.



Perpendicular Magnetization

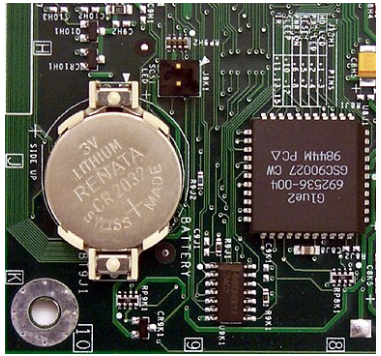
MRAM Applications

Application examples

Key requirements

Standalone

- Replace battery-backed SRAM or DRAM
- Buffer for hard disk drive
- Replace DRAM

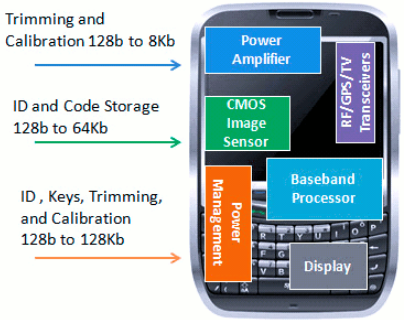


- Lower temp process is OK
- 0 C – 70 C operation
- 256 Mb – 1 Gb and up
- 30 - 70 ns read/write
- High endurance (10^{10} - 10^{15})

Embedded Non-volatile

Replace NOR eFlash to store:

- ❿ Microcontroller code
- ❿ Encryption key storage
- ❿ Trimming and calibration



- 400C process required
- -40 C – 105/125/150 C
- 1 – 64 Mb
- 30 ns read, 200 ns write
- Low endurance: 10^{6}

Mobile Cache

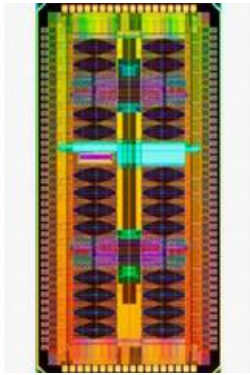
Replace SRAM for low performance & power apps

- Wearable electronics
- Co-processors
- Internet of Things

- 400C process required
- 0 C – 85 C operation
- 1 – 64 Mb
- 10 ns read/write
- High endurance (10^{12} - 10^{17})

Last Level Cache

- Fast dense memory for L3 or L4 cache
- Alternative to eDRAM



- 400C process required
- 0 C – 85 C operation
- 1 Gb and up
- 1 - 2 ns read/write
- Unlimited endurance (10^{18})

Increasing difficulty

MRAM in Edge AI and AIoT

Terry Torng

***Stealth Startup**
co-founder
Gyrfalcon Technology Inc

Core Challenge To AI: Energy Efficincy

- **Data Center Energy Use is Growing….**
- "Global data centers used roughly **3%** of total electricity in 2016, and will **double** every four years"
- Radoslav Danilak, December 15, 2017

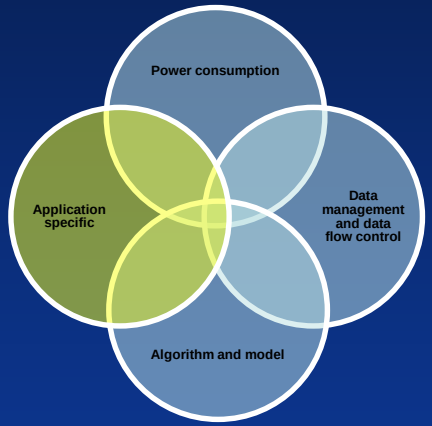
- "Global IP traffic will increase nearly threefold over the next five years, and will have increased 127-fold from 2005 to 2021."
- Bill Kleyman, Mar 09, 2018

- **Edge and IoT Devices….**
- "AI is hungry for processing power. IoT is projected to exceed 20b devices by 2020. There are currently 10b internet-connected devices, doubling to 20 billion will require massive increases to our data center infrastructure, which will massively increase our **electricity consumption**." Radoslav Danilak, December 15, 2017

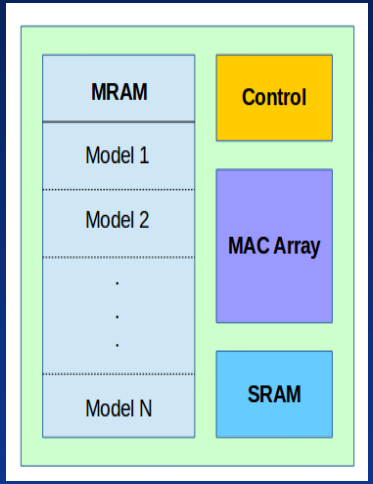
Need to make us greener…

5G is coming……

MRAM for AI



Challenges for the Edge AI



Memory : 75 to 80+ % of chip area
Memory : 67% or more leakage power

SRAM like MRAM:

1. Few ns read/write,
2. 10^{16} endurance,
3. memory density 3 : 1 or more vs SRAM.

Goal:

1. Chip size ½ of less.
2. AIoT (low duty), 60% less power consumption than SRAM only solution.
3. less than 1mw “high performance” AI accelerator for edge or AIoT

PPP (power, performance and price) Now, Next and Future

- **Hardware/software/MRAM co-design**
- Simplify circuit design
- Manufacturing friendly for foundries
  - high DR/R materials and different thermal budget processes…
- OST, SOT, voltage-controlled and MLC MRAM compatible
- Chip/wafer yield friendly

◆ What is the main segment for MRAM in 2024?

<My Position> e-Memory of Logic @ 2024

	CMOS SRAM-LLC	MTJ STT-MRAM(S)	CMOS eFlash	MTJ STT-MRAM(F)	Other NVM	
					ReRAM	PCRAM
Operation Voltage	<1.1 V	<0.5 V ☺	12 V	<0.5V ☺	> 6.5 V	> 1.8 V
Write Current	10^{-5} A	10^{-5} A	10^{-4} A	10^{-5} A ☺	10^{-4} A	10^{-4} A
Write Speed	<10ns	<10 ns	10000 ns	<200 ns ☺	50 ns	100 ns
Read Speed	<5ns	<5 ns	30 ns	<25 ns	< 5 ns	< 5 ns
Retention	Volatile	1～Several Month ☺	10Years	10Years	10Years	10Years
Endurance	10^{15}	10^{15}	$10^{3\sim4}$	$< 10^{8\sim12}$ ☺	10^{6}	$10^{9} – 10^{12}$
Cell Size	160 ~ 280F^2	12 ~ 28F^2 ☺	64 ~ 128F^2	6 ~ 14F^2 ☺	6 ~10F^2	4 ~ 19F^2
	①Low Power ②Small Cell Size		① Low Power ② High Speed Write ③ Better Endurance ④Small Cell Size			

◆ Which application / market will drive it?

<My Position> Mobile, IoT, Car Electronics, AI, Robot etc

◆ What are the challenges?

<My Position>

Improvement of MRAM Performance for each Application

For higher level cache: High Speed Write & Low Write Power
& over 10^{15} Endurance@128Mb-GbMRAM

For e-Flash of Automotive Application: Excellent Thermal Stability (Δ)

For Main Memory : Scalability & High Density Array

◆ What technological breakthrough needed?

<My Position>

1) Advanced Process Technology
including High throughput & Damage Control Technology

2) Circuit Technology including ECC Technology

3) Testing Technology for mass production

Most critical problem of MRAM is our mind.

⇒ **Tough Mind** to believe MRAM Potential

EVERSPIN TECHNOLOGIES

Data Persistence at Speed

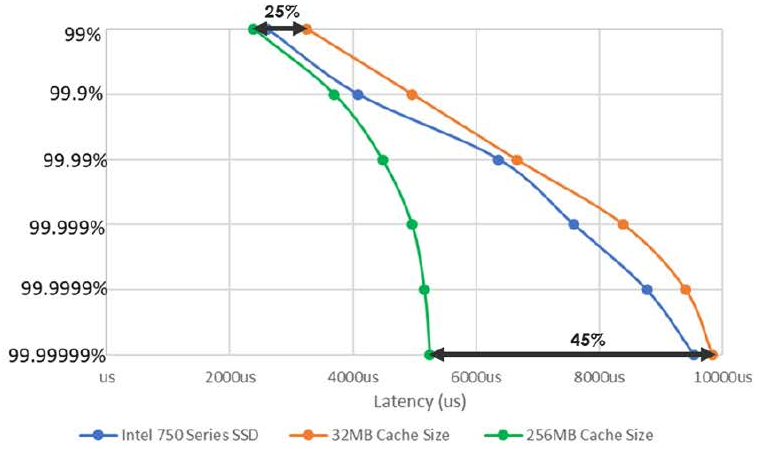
MRAM DEVELOPER DAY

MRAM Developer Day 2019
Panel: MRAM Application – Pros/Cons

Tom Andre
VP Engineering, Everspin Technologies

STT-MRAM Applications Today

Larger Buffer Improves QOS	Enable Higher Number of Streams	Simplified Architecture Eliminates Power Fail Hardening	More Physical Space For Storage Capacity	No Capacitor Liability	Optimized Interleave For Sequential Performance



QOS IMPROVEMENT

- 25% - 45% latency improvement
- Latency improvement is architecture dependent

MRAM Performance

MRAM DEVELOPER DAY

EVERSPIN TECHNOLOGIES

MR4A16B

1M x 16 MRAM

FEATURES

- +3.3 Volt power supply
- Fast 35 ns read/write cycle

EVERSPIN TECHNOLOGIES

EMD3D256M08BS1
EMD3D256M16BS1

256Mb ST-DDR3 Spin-transfer Torque MRAM

FEATURES

- Non-volatile 256Mb (32Mb x 8, 16Mb x 16) DDR3

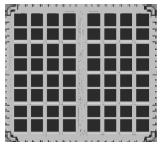
EVERSPIN TECHNOLOGIES

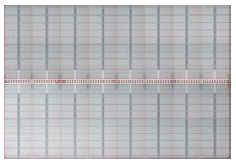
EMD4E001GAS1

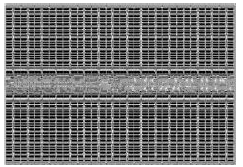
FEATURES 1Gb Non-Volatile ST-DDR4 Spin-transfer Torque MRAM

- 128Mb x8, 64Mb x16 Organization
- Supports most DDR4 features
- Page size of 1024 bits for x8, 2048 bits for x16
- VDD = VDDQ = 1.2v
- VPP = 2.5V
- Operating Temperature of 0˚C to 85 ˚C
- 667MHz clock frequency (fCK)
- On-Device Termination
- Multipurpose register READ and WRITE capability
- Per-Device addressability (PDA)
- Connectivity Test
- On-Chip DLL aligns DQ, DQS, DQS transition with CK transition
- Burst lengths of 8 addresses
- All addresses and control inputs are latched on rising edge of the clock

	16Mb Toggle	256Mb ST-DDR3	1Gb ST-DDR4
VDD / VPP	**3.3V**	**1.5V**	**1.2V / 2.5V**
Data Retention	**20 years / 85C** 2 years / 125C	**3 months / 70C**	**3 months / 70C** 10 yrs / 85C capable
Endurance	**>1e16** (>10yrs constant use)	**1e10 cycles** every page	**1e10 cycles** every page
Uniform 10yr writes per Chip	**18 PBW** (performance limit)	**320 PBW** (cycle limit)	**840 PBW** (performance limit)
Peak Bandwidth per x16 Chip	**57MB/s**	**2.67GB/s**	**2.67GB/s**







EVERSPIN TECHNOLOGIES

STT-MRAM Areas for Development

MRAM DEVELOPER DAY

	Storage / SSD	Industrial	Auto	Aerospace
Application	Non-volatile Data Buffer/Cache/PMR	Non-volatile Data logs, params	Non-volatile Data params, buffer	Non-volatile Code, Data
STT-MRAM benefit	Write Bandwidth, Endurance	Endurance, Reliability	Write BW, End, Reliability	Rad Hard, Reliability
Density	128MB - **>1GB**	8MB - 128MB	128MB – **>1GB**	8MB – 128MB
Operating Temp	0C - 85C	**-40C** – 85C	**-40C – 125C** (Grade 1) **-40C – 150C** (Grade 0)	**-40C – 125C** **-55C – 125C**
Data Retention	3 months / 70C	10 years / 85C	**Profile across temp**	**15 yrs / 105C**
Endurance	Buffer: 1e10 every page **PMR: >1e15 total**	varies by app **>1e15 total**	varies by app	varies by app
Peak Bandwidth	5GB/s - **>12GB/s**	10MB/s – 2GB/s	10MB/s – 2GB/s	<100MB/s

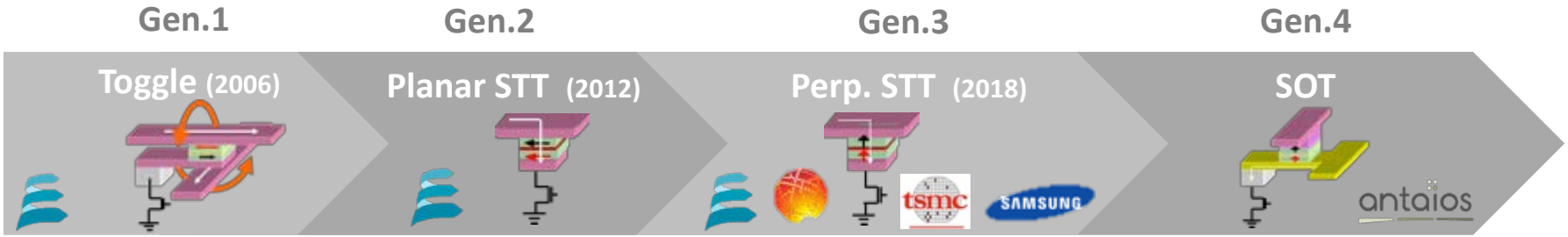
antaios

MRAM Developer Day

August 5, 2019

ANTAIOS “NEXT-GEN” SOT MRAM

Mission Statement : Jointly develop and license SOT (technology and IPs)
as the **next-generation MRAM** that solves STT shortcomings



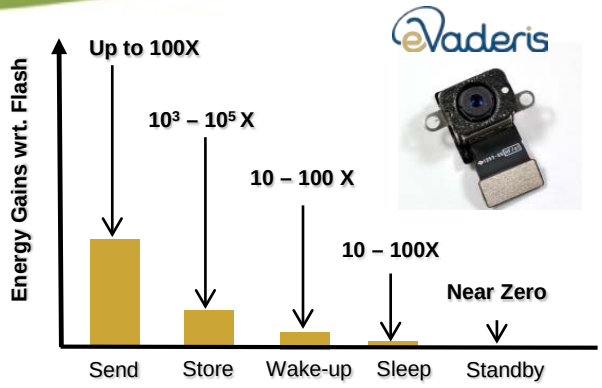
Endurance-Retention-Speed tradeoff
→ **Limited to e-NVM applications**

Infinite endurance / High intrinsic speed
= Fully RAM compatible
(enables Cache applications)

PERFORMANCES PROS & CONS (STT)

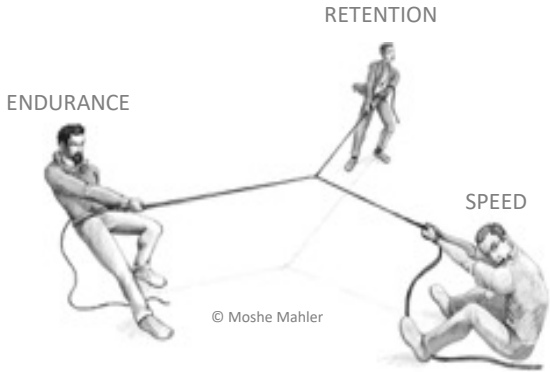
Pros

- Fast and low (write) power, beats eFlash hands down
  - ➢ Huge power savings at chip level (+ endurance)
- Fast and non volatile
  - ➢ Zero standby power, zero leakage, unlike SRAM



Cons (STT)

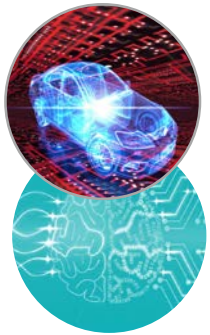
- STT not RAM compatible
  - o Endurance / speed / retention trilemna
  - o Low read window = limited read speed
  - o Heavy ECC needed (cost, performance limitations)



MRAM APPLICATIONS (STT)

“Low Hanging Fruit” Market : IoT

- In particular for those applications involving large amounts of data for which power and endurance are key (ex. Data logging, audio/video monitoring)



Other “near-ready” markets

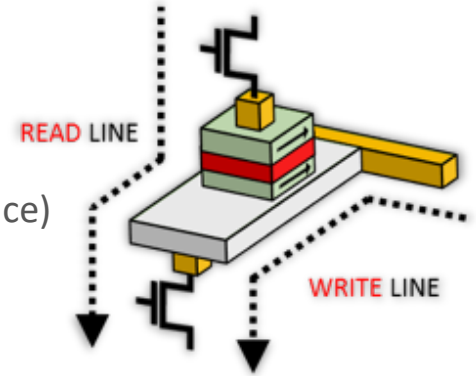
- **Automotive** - Provided the temperature/reliability specs are met
- **AI chips** - Killer benefits of MRAM (can hold data during compute)
  STT good enough as-is, but SOT should be even better

STT is excellent for NVM (e-Flash) replacement, but full benefit of MRAM migration will be achieved when cache (e-SRAM) is addressed as well

ACTIONS NEEDED (AS NEXT STEP)

To unleash full potential of embedded MRAM …

- **Improve device towards RAM requirements**
  - Need speed AND endurance at the same time
    - STT won't do it - Need something new
    - SOT is the only solution (fast write & infinite endurance)
  - Improve read margin to raise (read) speed
    - By materials (TMR increase)
    - By design (device and chip level)



To address standalone market …

- **Achieve high capacities (>Gb)**
  - Control of BER, distribution (tails), …
  - Dedicated memory process / architecture for high density (low F2)