MRAM HAS LANDED!

The Era of Gigabit Universal Memory Begins

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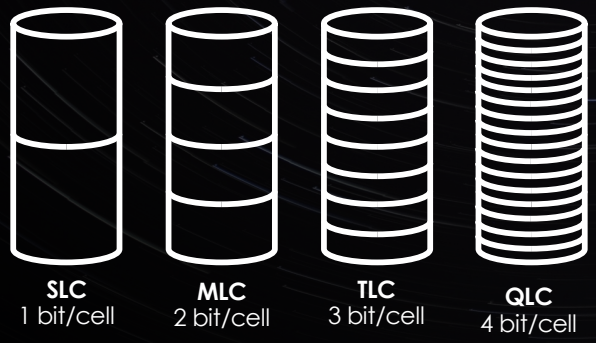
MRAM Developer Day, August 6, 2019

Forward-Looking Statements

This presentation contains "forward-looking statements" that involve risks, uncertainties and assumptions. If the risks or uncertainties materialize or the assumptions prove incorrect, our results may differ materially from those expressed or implied by such forward-looking statements. All statements other than statements of historical fact could be deemed forward-looking statements, including, but not limited to: any estimates of addressable market size and our ability to capture that market, market trends and market opportunities, customer growth, product availability, technology developments, or other future events; any statements about historical results that may suggest future trends for our business; any statements regarding our plans, strategies or objectives with respect to future operations or business performance; any statements regarding future economic conditions; and any statements of assumptions underlying any of the foregoing. These statements are based on estimates and information available to us at the time of this presentation and are not guarantees of future performance. Actual results could differ materially from our current expectations as a result of many factors, including, but not limited to: market adoption of our products; our limited operating history; our ability to raise capital; our history of losses; our rate of growth; our ability to predict customer demand for our existing and future products; our ability to hire, retain and motivate employees; the effects of competition, including price competition; technological, regulatory and legal developments; and developments in the economy and financial markets. We assume no obligation, and do not intend, to update these forward-looking statements, except as required by law.

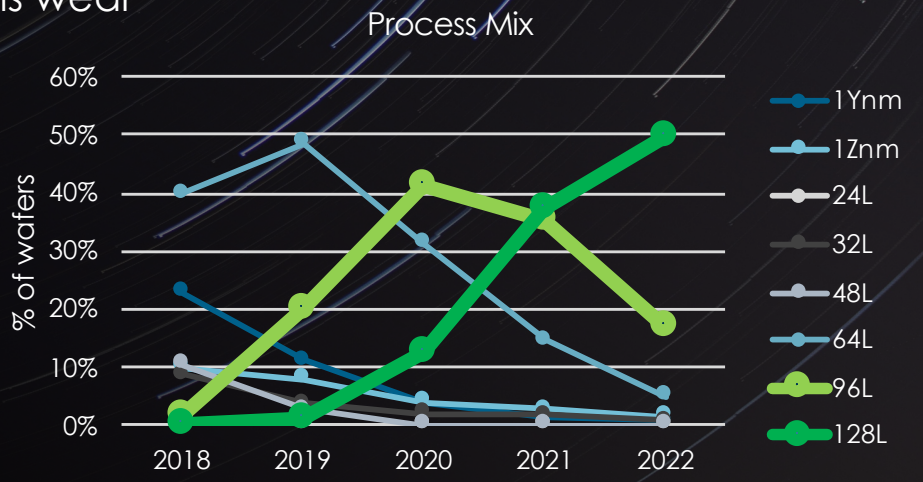
We have watched NAND Flash establish ever higher densities
but larger blocks and bits/cell bring higher latency and lower endurance



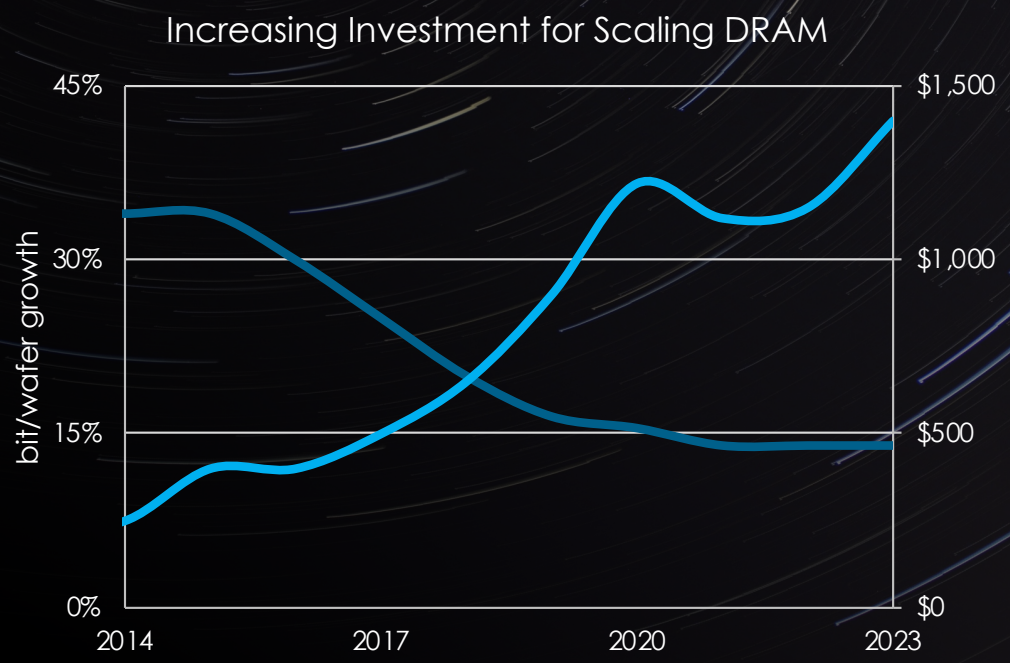
More bits/cell require more time to read and program

Tighter distributions harder to maintain as flash cells wear

More layers mean larger blocks of data to manage (more time to perform garbage collection)



We have watched DRAM bring increasing density and performance
but bit cost benefits are slowing



Only MRAM Demonstrates The Promise of Universal Memory

PERSISTENCE

Maintains memory contents without requiring power

PERFORMANCE

SRAM & DRAM-like performance with low latency

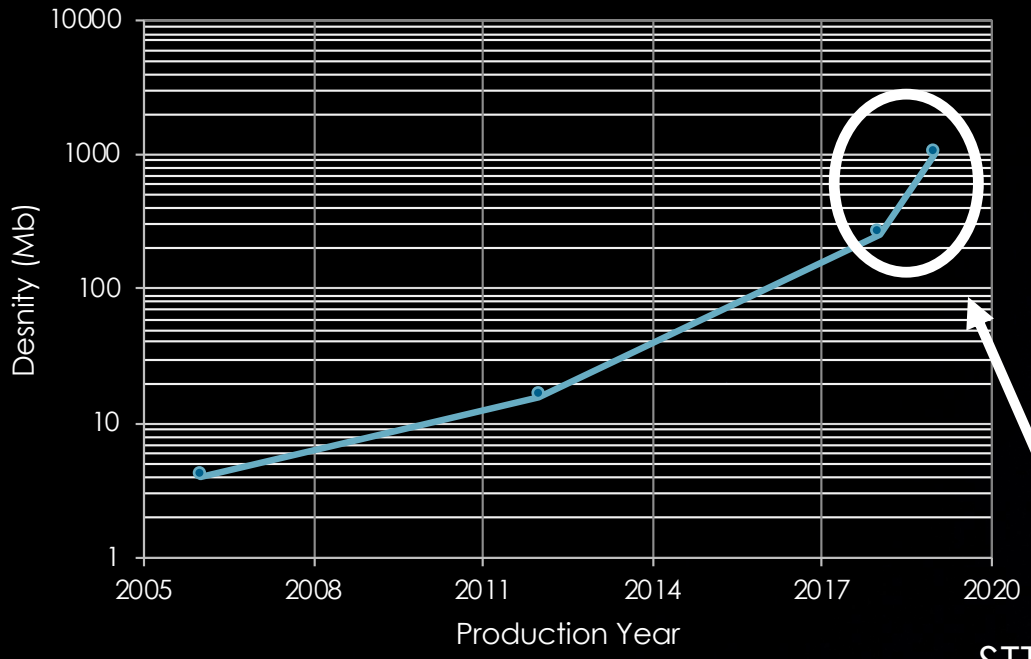
ENDURANCE

Superior durability supports memory workloads without sophisticated management

RELIABILITY

Best-in-class robustness designed and tested for extreme conditions

MRAM Technology Entering The Gigabit Era:
More than just density

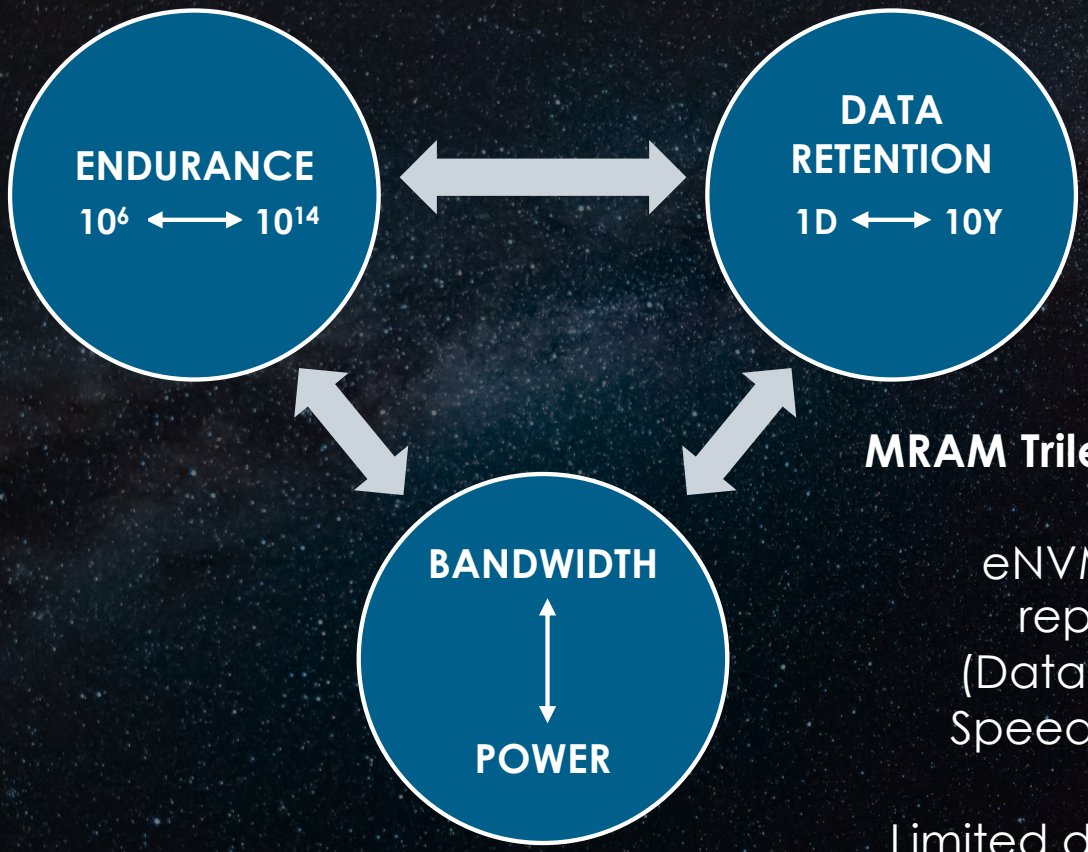


1Gb Progress over 256Mb

80X the data retention:
10 years @ 85C

STT Enabling New Density Path

What about the MRAM Trilemma?

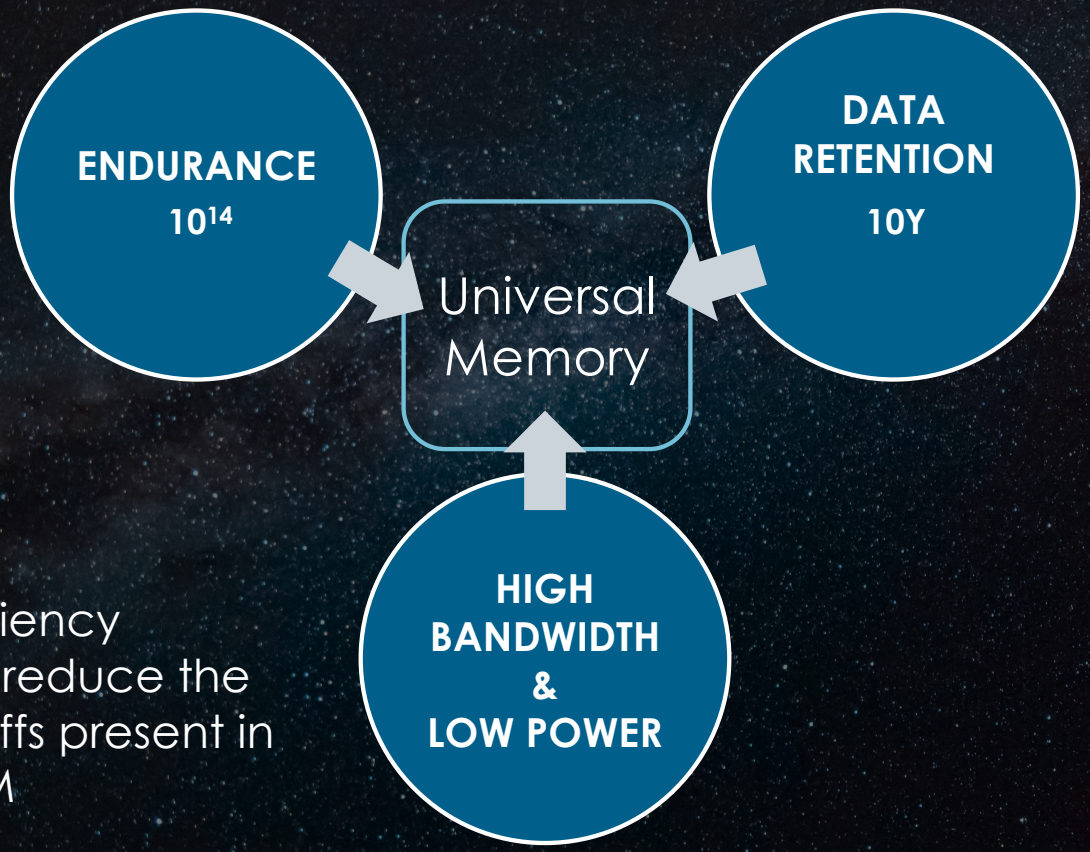


MRAM Trilemma Examples:

eNVM or eSRAM replacement (Data Retention or Speed/Endurance)

Limited density vs. DRAM

Overcoming the MRAM Trilemma



Memory Cell Efficiency improvement will reduce the degree of tradeoffs present in today's STT-MRAM

The State Of Advanced MRAM Manufacturing

Several equipment suppliers have 300mm production tools

Magnetic Materials Deposition

TEL™ TOKYO ELECTRON

Canon CANON ANELVA

APPLIED MATERIALS®

Etch

HITACHI Inspire the Next

Lam® RESEARCH

APPLIED MATERIALS®

Logic Fabrication Progress

STT-MRAM enters mass production industry-wide

GLOBAL FOUNDRIES

Producing 40nm and 28nm Discrete STT-MRAM (for Everspin)
22nm FDX embedded production expected 2019

tsmc

22nm ULP Production 2019

SAMSUNG

22nm FD-SOI Production 2019

intel

22nm FinFET Production Ready 2019

UMC

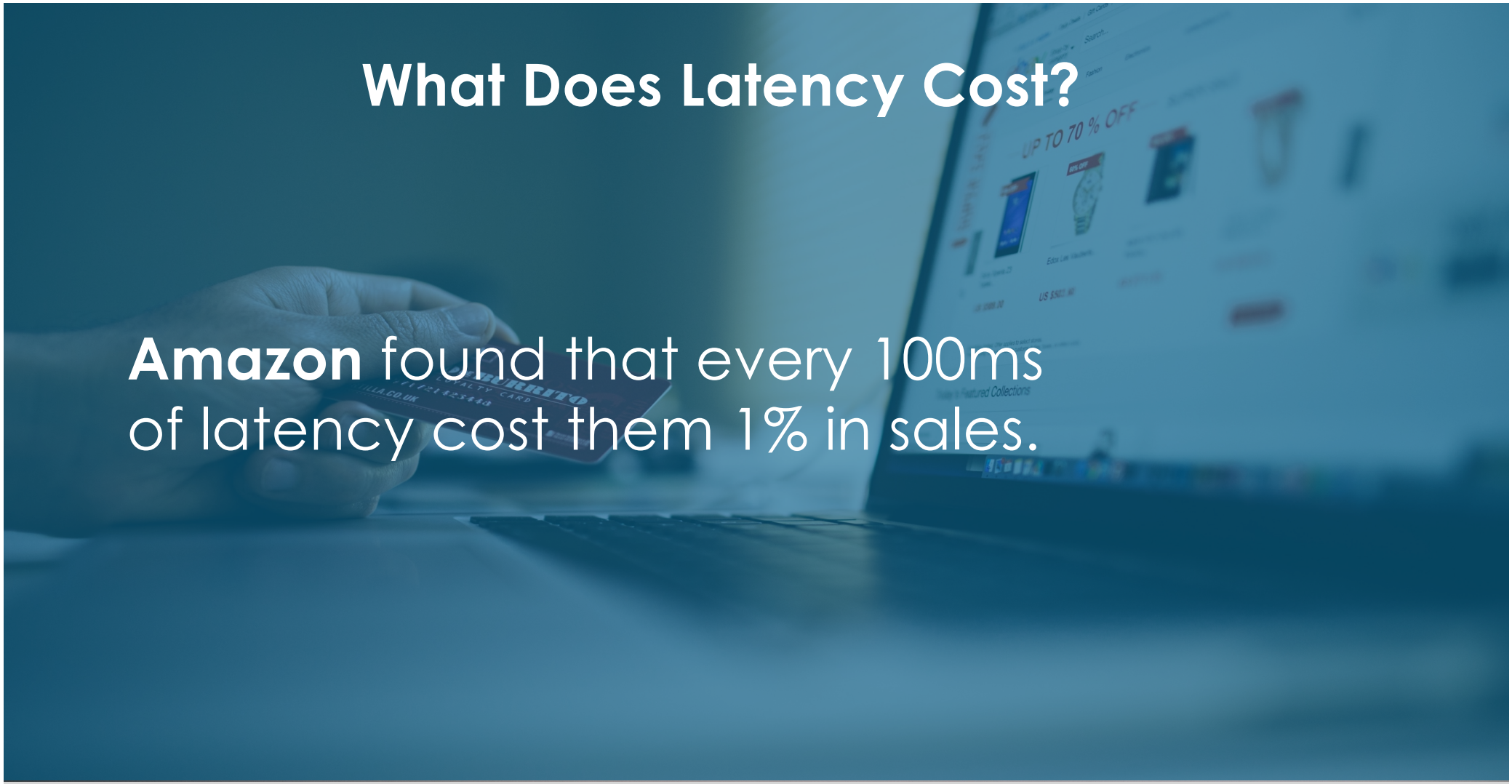
MRAM Partnership Announced

Others still to come

STT-MRAM Is Making Tracks In Addressing Data Center Latency

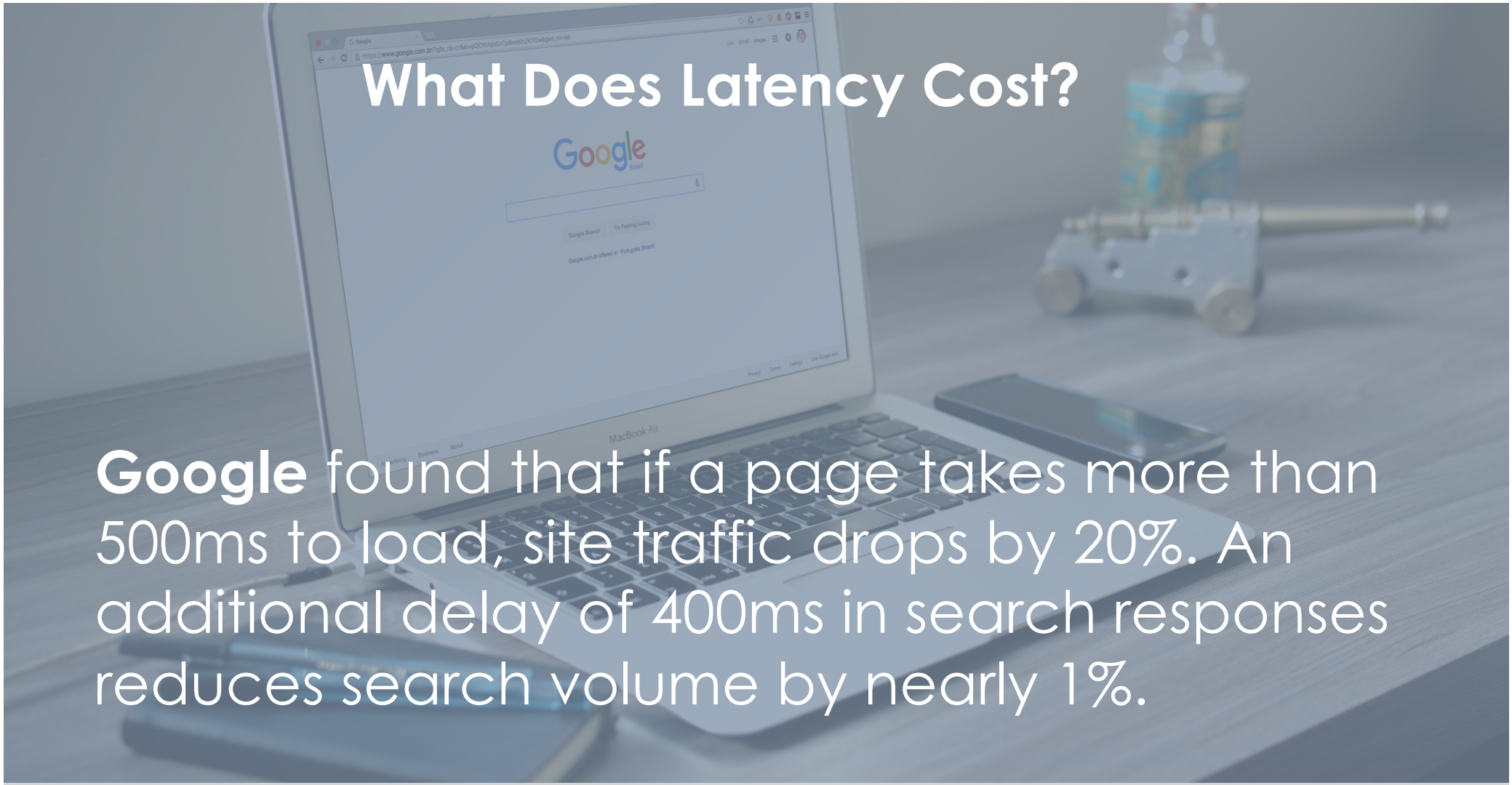
One small step for this revolutionary technology…

What Does Latency Cost?



Amazon found that every 100ms of latency cost them 1% in sales.

What Does Latency Cost?

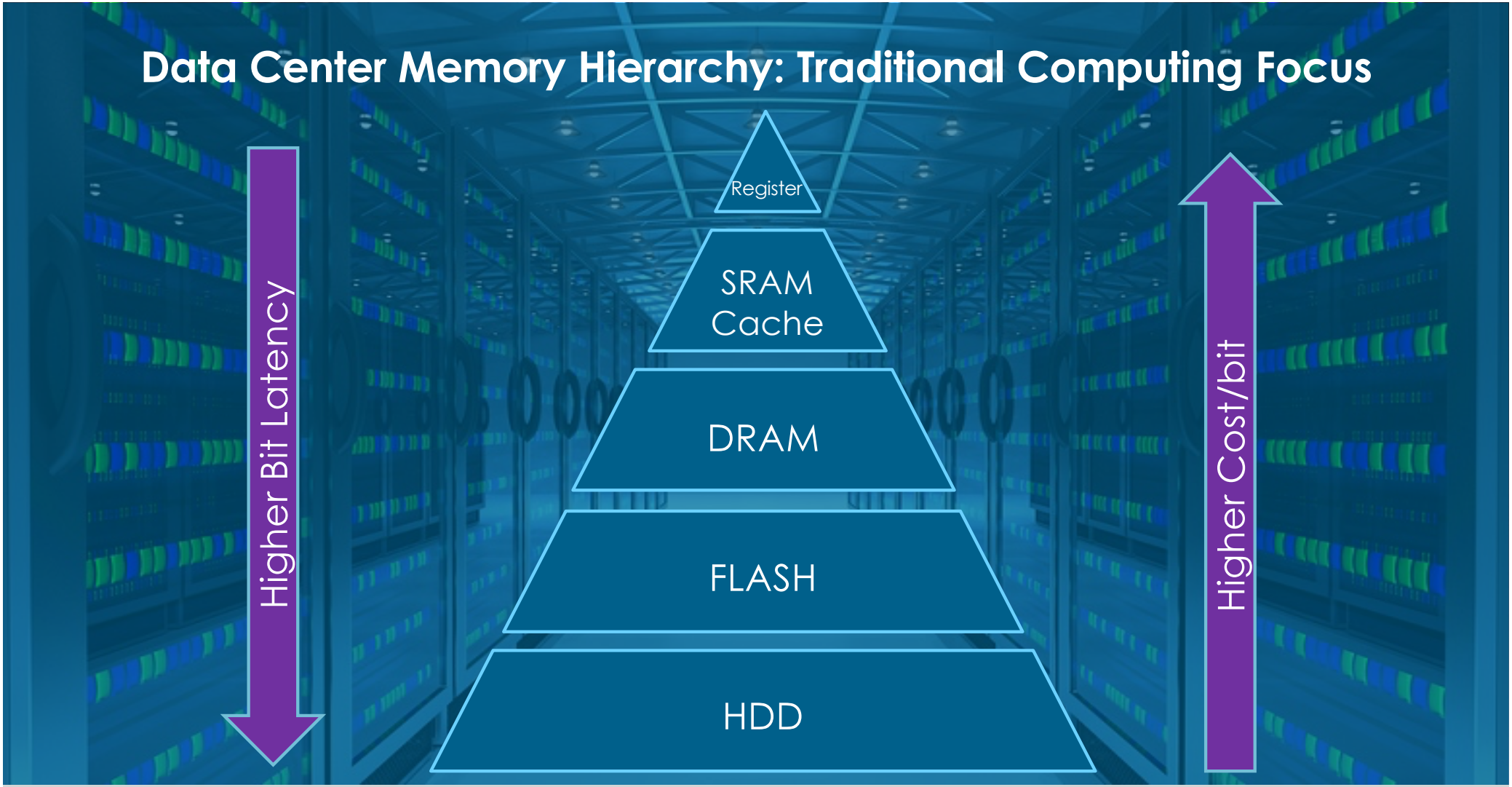


Google found that if a page takes more than 500ms to load, site traffic drops by 20%. An additional delay of 400ms in search responses reduces search volume by nearly 1%.

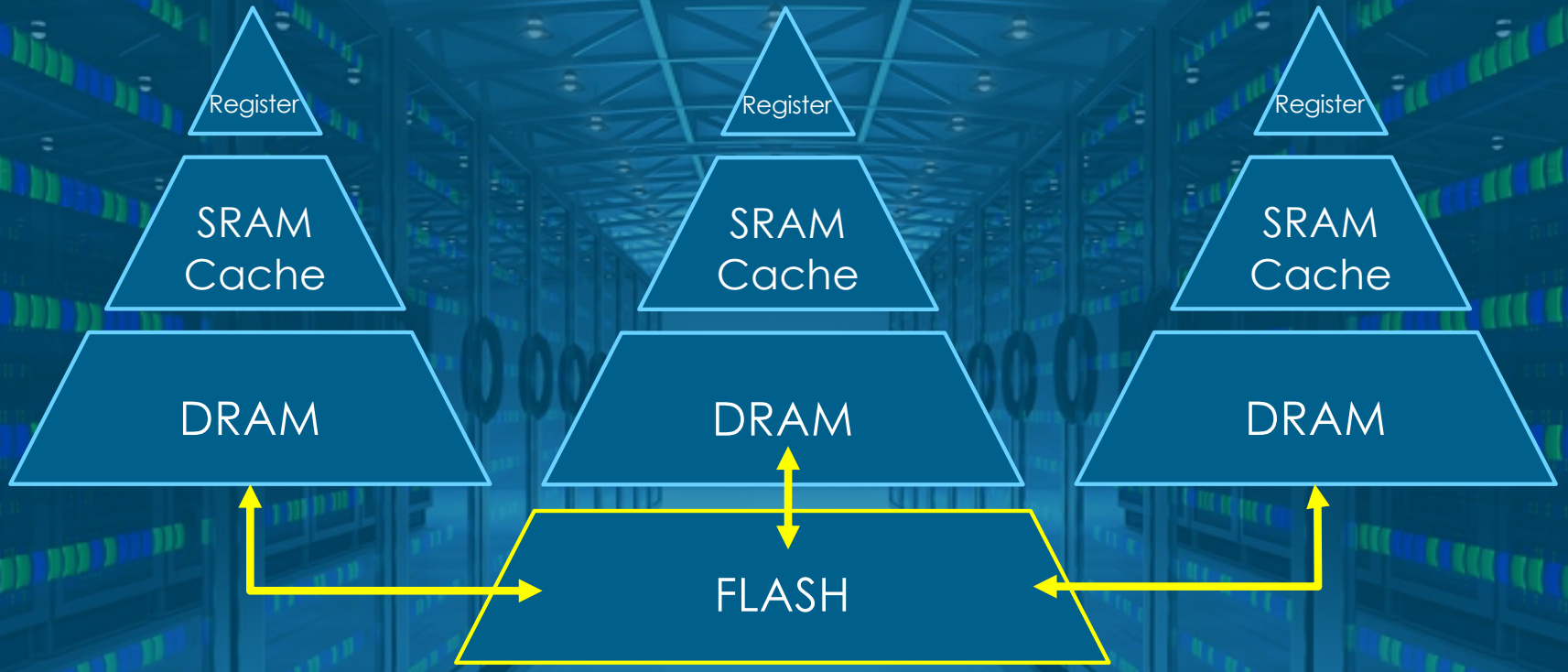
What Does Latency Cost?

A brokerage firm could lose as much as $4 million in revenue per ms if its **electronic trading platform** was only 5ms behind the competition. A 1ms advantage in latency can be worth upwards of $100 million per year.

Data Center Memory Hierarchy: Traditional Computing Focus



Flash Storage Disaggregation Puts Flash Latency Central

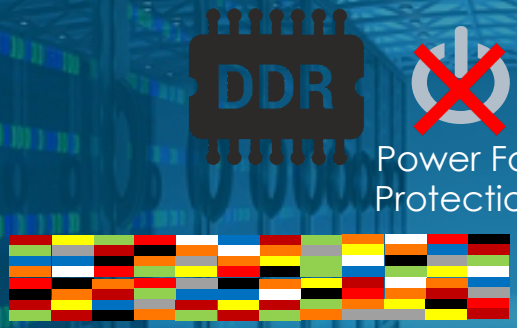


Flash Arrays subject to thousands of dissociated VMs further fragmenting workloads

Storage Bandwidth vs. Latency
In SSD Architecture

Non-Volatile Write Buffer

MLC NAND Flash



SATA3

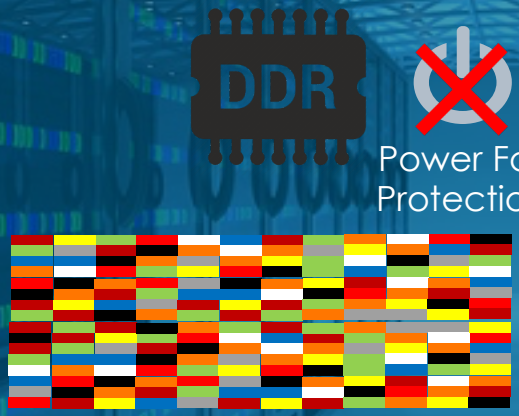
4 CH

Storage Bandwidth vs. Latency
In SSD Architecture

Non-Volatile Write Buffer

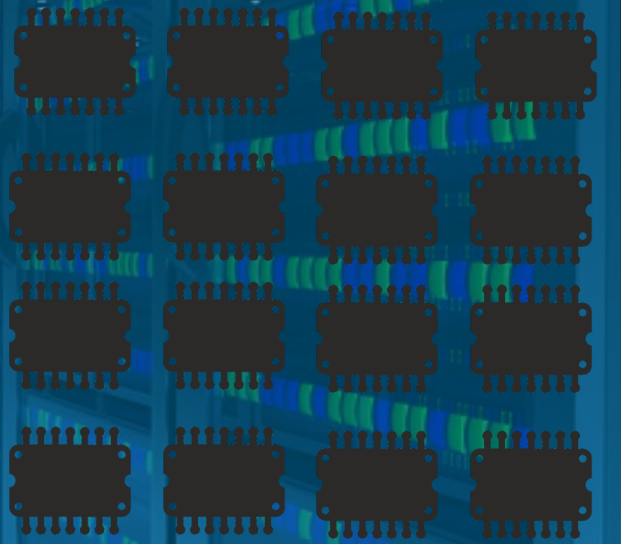
3D TLC NAND Flash

PCI Gen2



Power Fail Protection

8 CH



- Bigger Buffers
- More Capacitors

- Bigger, Slower Blocks
- Lower Endurance

Storage Bandwidth vs. Latency
In SSD Architecture

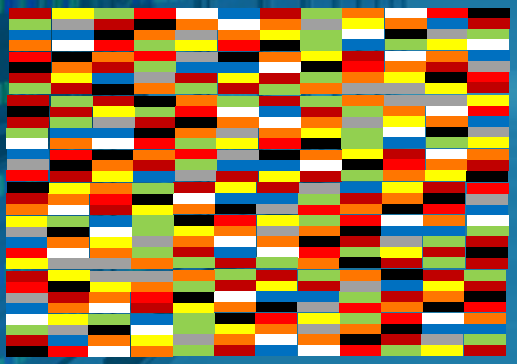
Non-Volatile Write Buffer

3D QLC NAND Flash

PCI Gen3 NVMe

Power Fail Protection

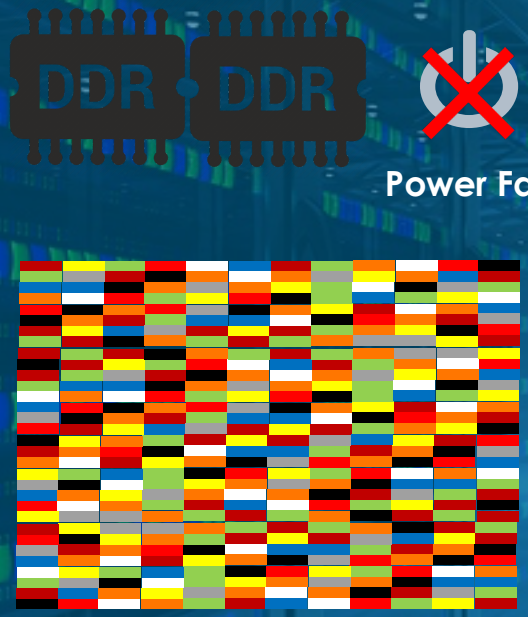
16-32 CH



Power Fail Capacitors limit buffer size and threaten reliability

- Even Bigger, Slower Blocks
- Even Lower Endurance

MRAM Addresses Latency Challenge

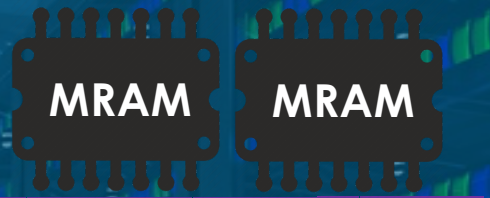


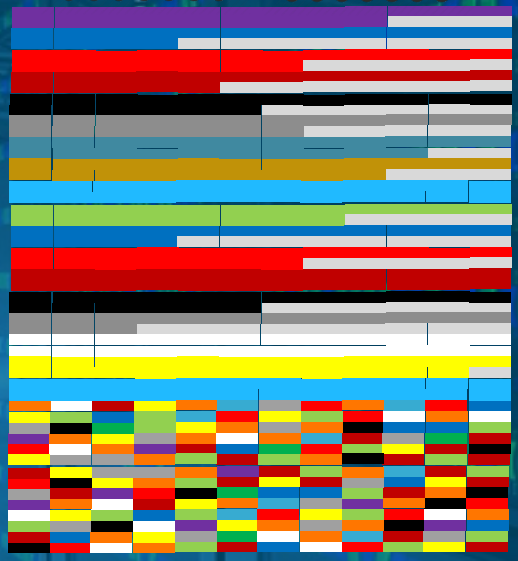
Power Fail

Non-Volatile Write Buffer Redesign

MRAM Enables More:

NVMe Sets
I/O Streams
Zoned Name Spaces



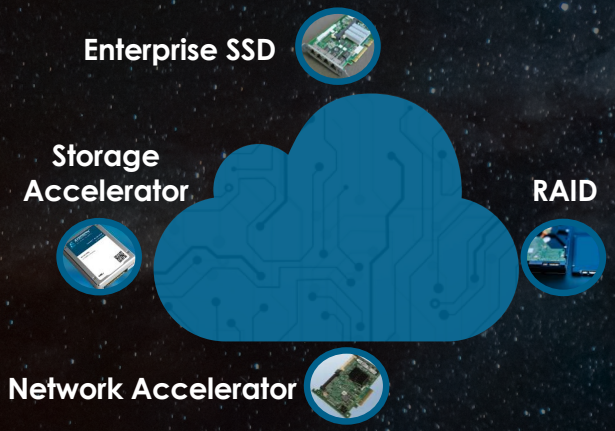


- 2-3X Drive Life
- Improved 6-9s Latency QOS
- No Caps: higher reliability & more Flash Capacity

5G Opens A Universe of MRAM Applications

Core

175 Zettabytes of data by 2025

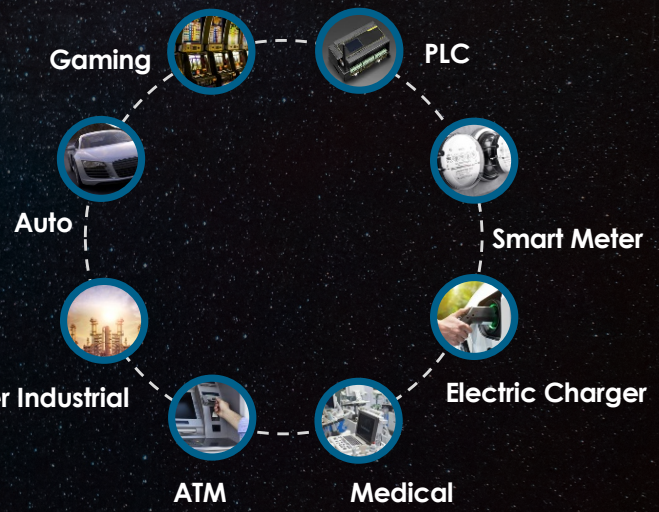


Edge

By 2025 75% of enterprise data will be created and processed outside the Datacenter

End Points

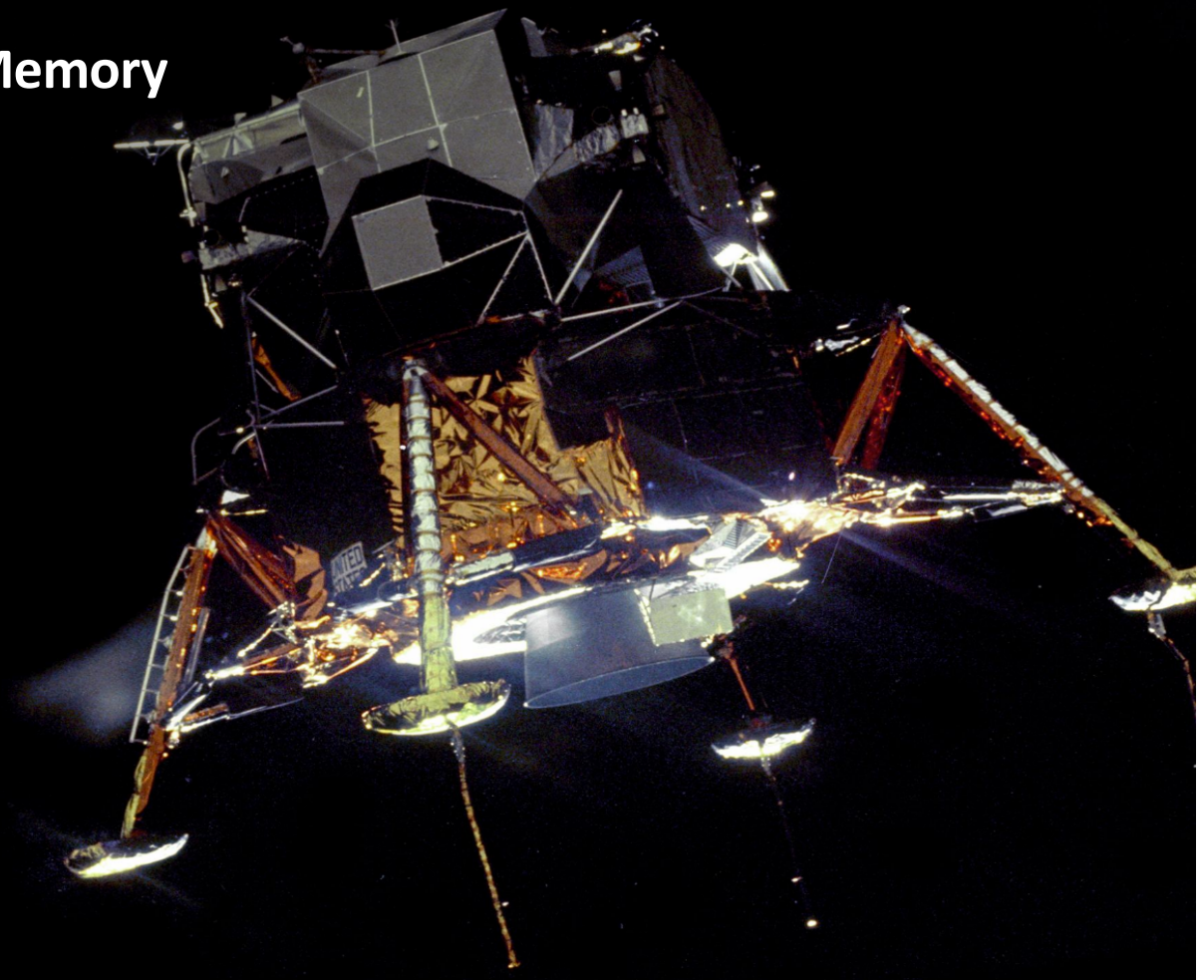
27B Networked Devices by 2021 Producing 79 ZB



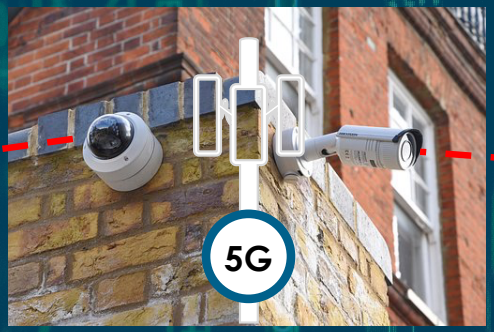
STT-MRAM Takes On Universal Memory Challenge of 5G

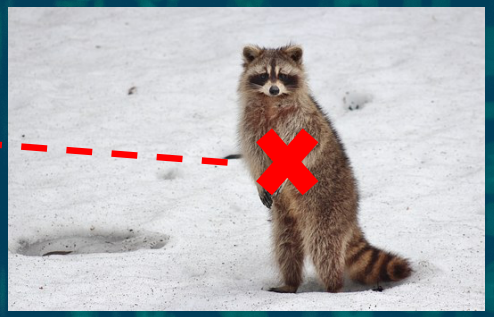
Bringing a simpler, low power solution to the challenge of ”always connected”

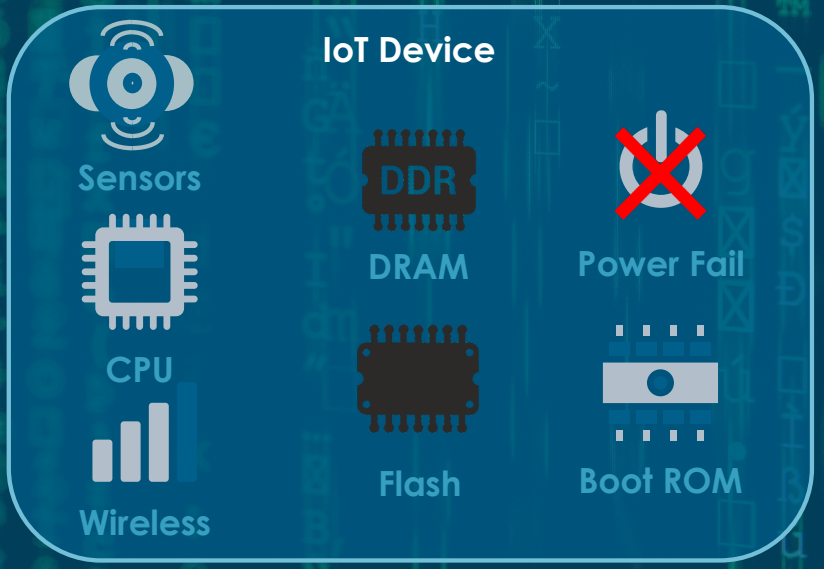
…One giant leap in the pursuit of Universal Memory



IoT Memory Requirements Changing

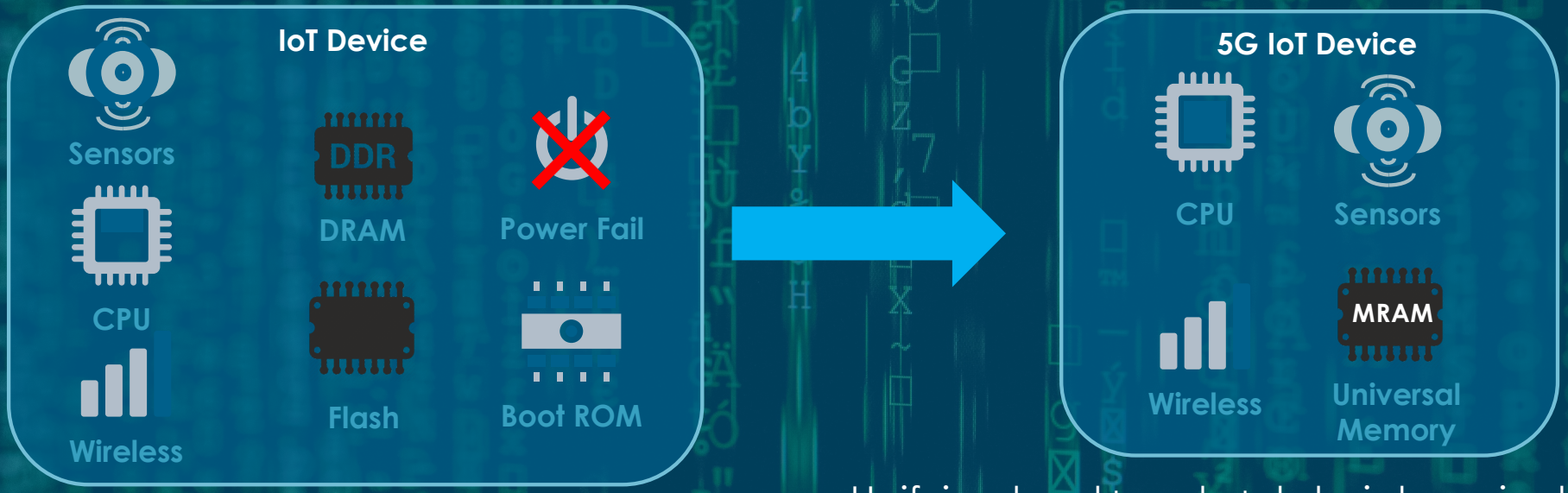






- Complexity High
- Data At Risk
- Slow System Init
- Power Inefficient

Compute Disruption – The Move to Universal Memory



- Complexity High
- Data At Risk
- Slow System Init
- Power Inefficient

- Unifying boot+code+data into a single memory greatly simplifies design
- Simpler design is easier to secure
- Data memory is inherently non-volatile – never at risk
- System can sleep with memory power off

Can STT-MRAM go where no memory has gone before?

5-Year STT-MRAM Prediction:

DRAM-like Capacity
Fast Random Access
No Endurance Limit
10 years Data Retention
Automotive Operating Temperature

STT-MRAM Is On The Path to True Universal Memory

Did we mention MRAM is naturally resistant to radiation in space?