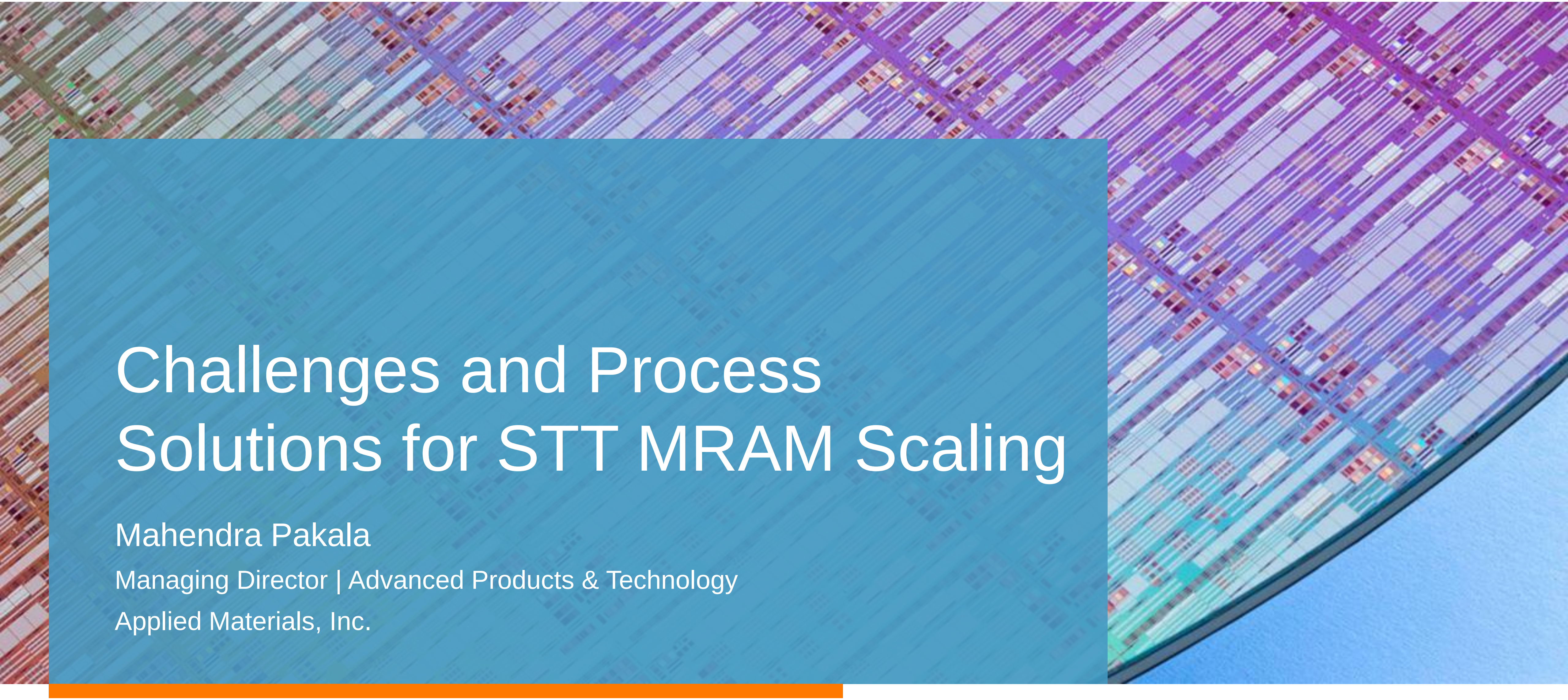

Challenges and Process Solutions for STT MRAM Scaling

Mahendra Pakala

Managing Director | Advanced Products & Technology

Applied Materials, Inc.

AGENDA

- New Memory Application Space
- Applied Solutions for MRAM
- MRAM Scaling (Process and Device)

AGENDA

- New Memory Application Space
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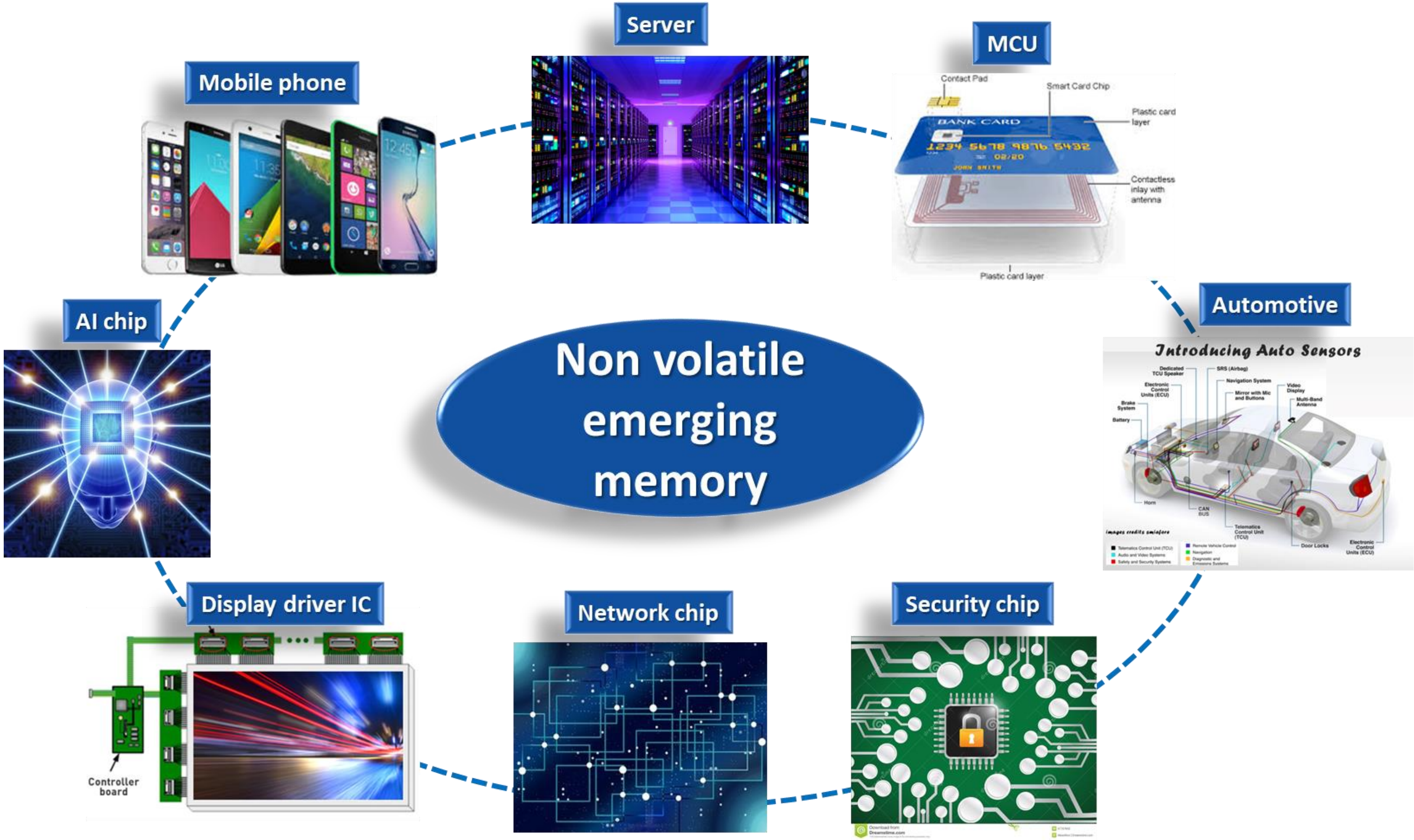
Emerging Memory | Markets



Non volatile emerging memory

Server

MCU

Automotive

Security chip

Network chip

Display driver IC

AI chip

Mobile phone

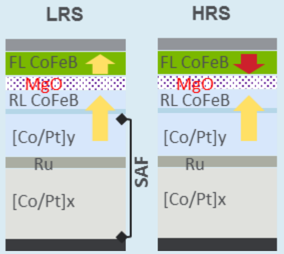
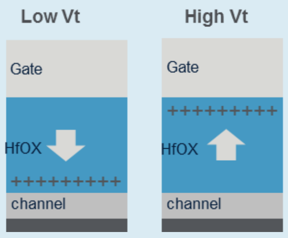
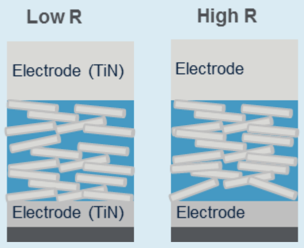
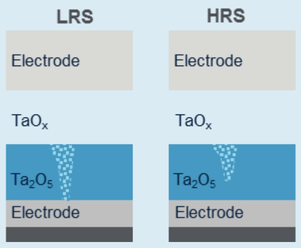
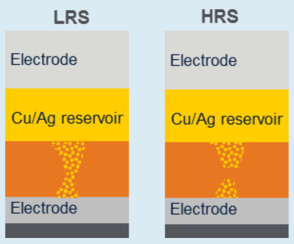
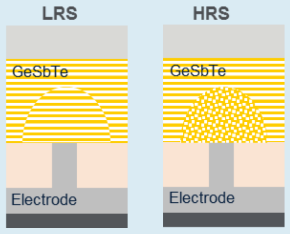
AI – Big Data Driving a Renaissance of Hardware Development and Investment

	INITIAL DEPLOYMENT	CLOUD	EDGE
Accelerators GPU, TPU, ASICS, FPGAs	Now	✓	Autos
Near Memory DDR, SRAM, HBM, NAND, SCM	Now to 2 years	✓	✓
New Memory MRAM, ReRAM, PCRAM, FeRAM	Now to 5 years	✓ ←	✓
In-Memory Compute Analog, ReRAM, PCRAM	2 to 5 years	✓ ←	✓
Novel HPC Quantum, Synaptic	5 to 10 years	✓ →	✓

New Memory Outlook

Product Availability
🟩 MFG / Ready
🟨 Sampling

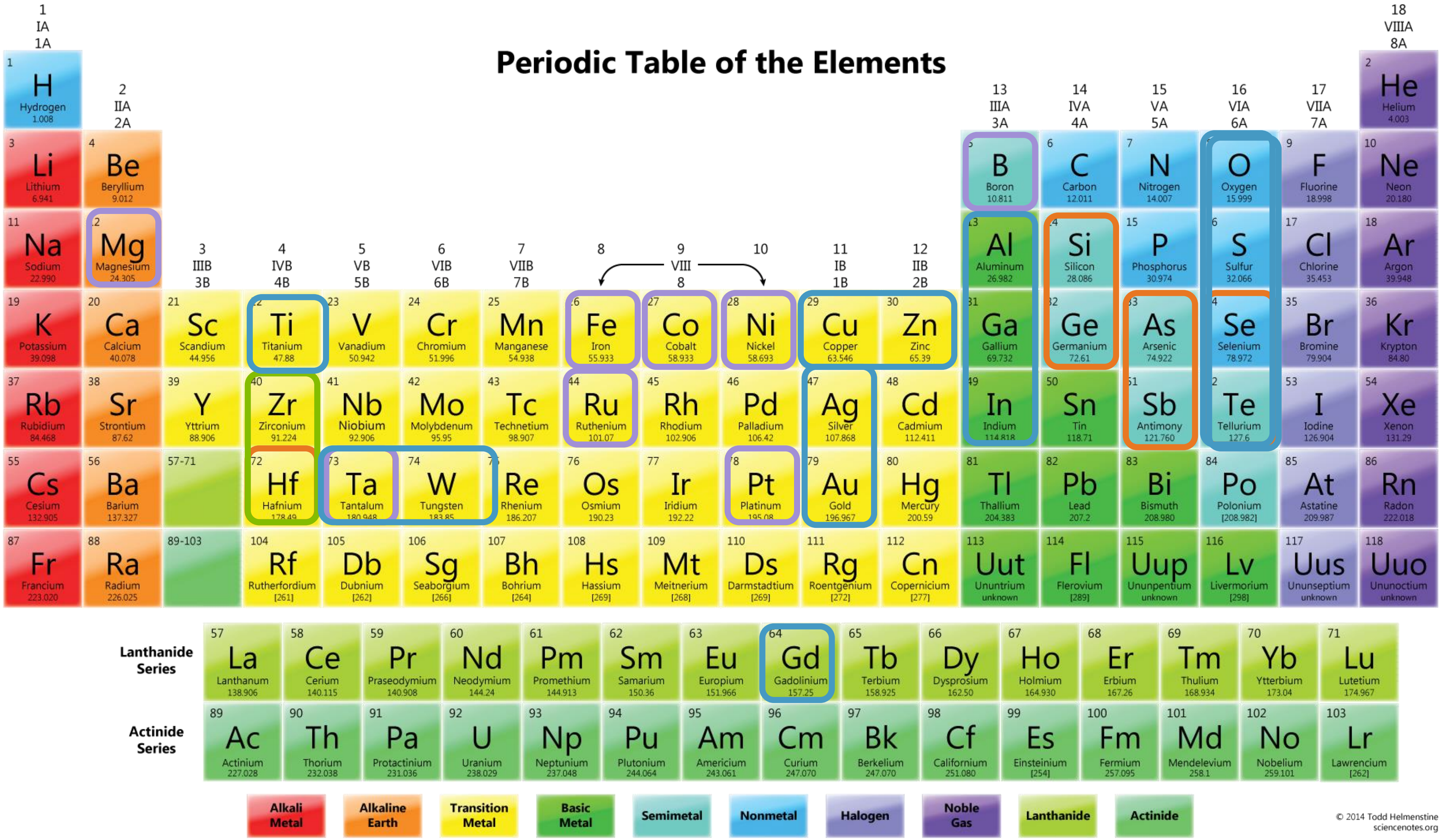
Performance

		STT MRAM	HfOx FEFET	NRAM	OXRAM	CBRAM	PCM
	MEMORY						
	Standalone* (node)	🟩 256Mb/1 Gb (40/22nm, ES/GF)	R&D	*R&D*	🟩 4 Mb (180nm, Fujitsu)	*R&D*	🟩 128 Gb (20nm, Intel, Micron)
	Embedded* (node)	🟩 < 100 Mb (2xnm SEC, TSMC)	*R&D*	*R&D*	🟩 64 kB (180nm, PAN)	🟩 0.512 Mb (> 100nm, Adesto)	🟨 *128 Mb* *(28nm, ST)*
	Cell Size (F2)	10 – 20	10 - 20	*< 4 - 8*	< 4 – 8	< 8 – 16	*< 4 - 8*
WFE	**Deposition**	**PVD**	**ALD**	**Spin Coat**	**PVD**	**PVD**	**PVD**
	Etch	**IBE / RIE**	NA	**RIE**	**RIE**	**RIE / IBE**	**RIE**

- PCRAM, STT MRAM and RERAM (OxRAM and CBRAM) enter volume manufacturing phase
- PVD is preferred process to deposit these complex material systems
- RIE is preferred etch process. IBE being introduced for scaled STT MRAM

**Announcements from Everspin, GF, SEC, Panasonic, ST, Adesto, Techinsights*

Example of Elements to Enable New Memories



Periodic Table of the Elements

© 2014 Todd Helmenstine
sciencenotes.org

PCM, Selector

- M-K. Lee, IEDM 2012
- G.H. Kim, APL 2012
- L. Zhang, IEDM 2014

STT-MRAM

- K. Ando, JAP 2014

FE-FET

- X. Tian, APL 2018
- A. Pal, APL 2017

CBRAM

- Adesto Technologies, IEEE 2013 talk

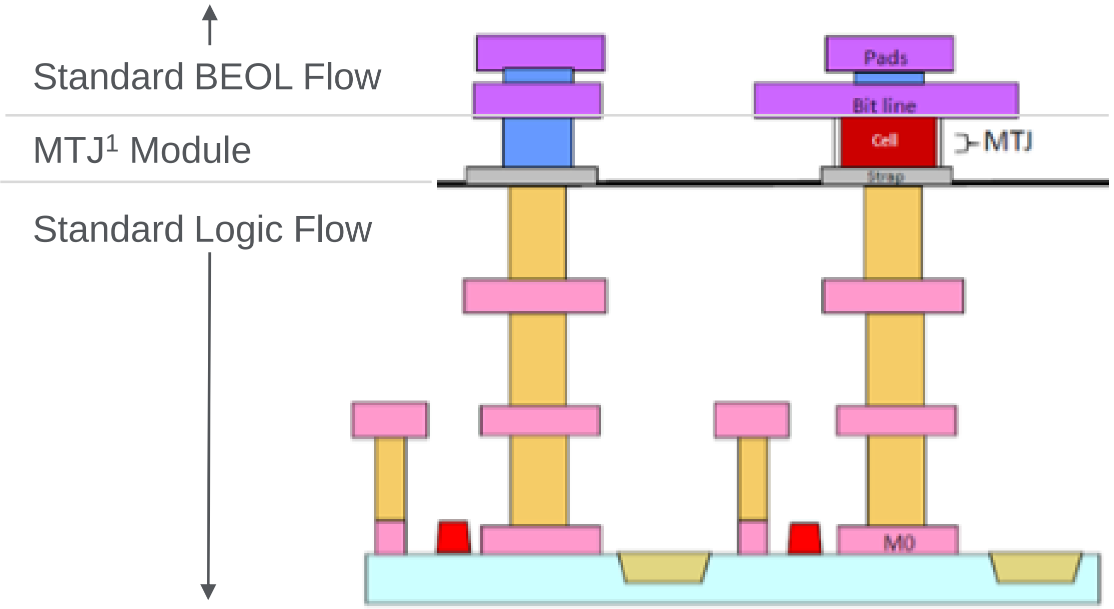
AGENDA

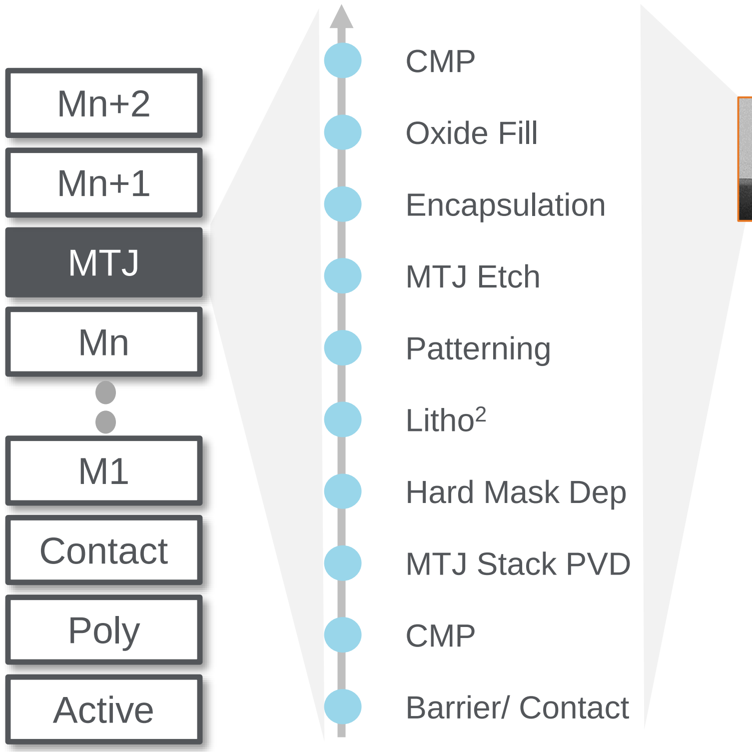
New Memory Application Space

Applied Solutions for MRAM

MRAM Scaling (Process and Device)

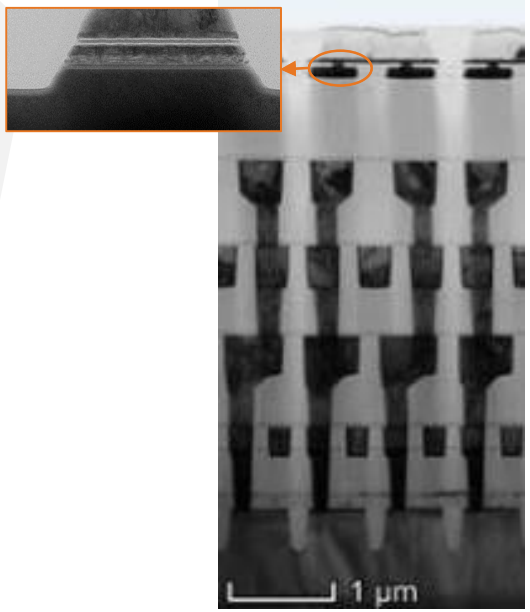
STT MRAM Fabrication | Typical Process Flow





- Mn+2
- Mn+1
- MTJ
- Mn
- M1
- Contact
- Poly
- Active

- CMP
- Oxide Fill
- Encapsulation
- MTJ Etch
- Patterning
- Litho[2]
- Hard Mask Dep
- MTJ Stack PVD
- CMP
- Barrier/ Contact



Applied Internal Data based on Spin Memory design

MTJ Module conveniently inserted in logic flow with up to 4 additional masks[2]

---

[1] *MTJ: Magnetic Tunnel Junction*

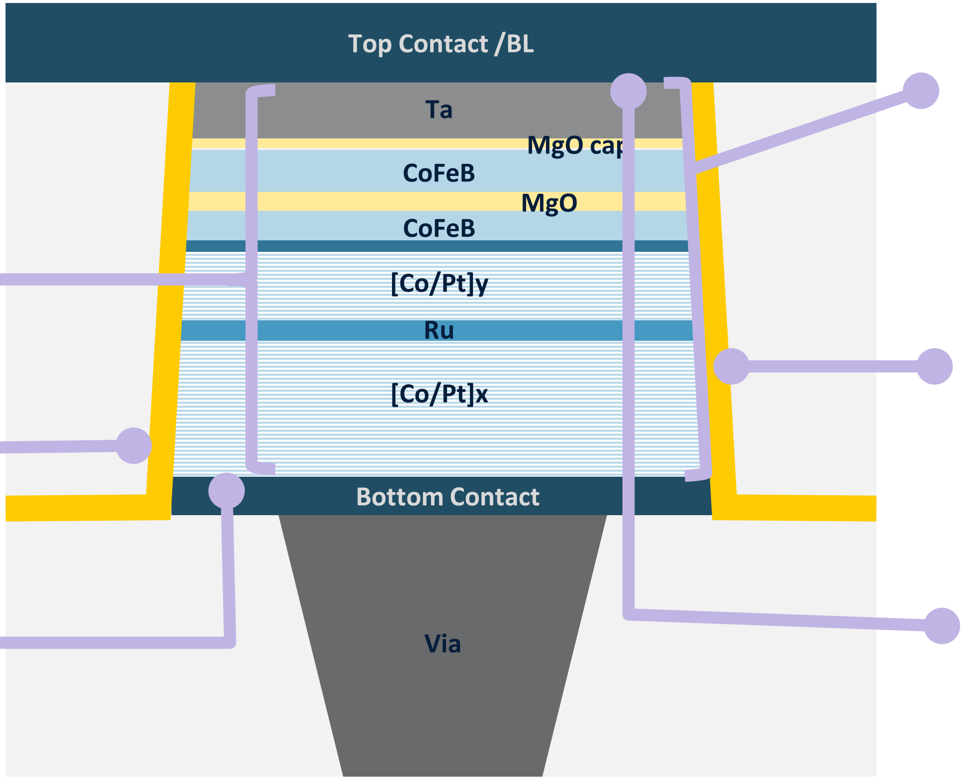
[2] *Optional bottom and top contact and mark open mask steps*

MTJ Module Fabrication | Critical Steps

MTJ PVD:
- Complex stack of 30+ layers
- Precise thicknesses & uniformity
- Sharp interfaces
- Formation / preservation of textures
- MgO stoichiometry & defect control

ILD: Low Temp

Bottom-electrode CMP:
Atomic smooth surface



MTJ Etch:
- No re-dep on sidewall
- Minimize damage
- Non-corrosive
- Straight sidewall

Encapsulation:
- Low Temp
- Hermetic

Oxide CMP:
- High selectivity on oxide
- Damage free

Critical: Controllability of uniformity, stoichiometry, structure, interfaces & damage free patterning
MTJ CD of 20-50nm and dense pitch is desired

MTJ Module Fabrication | Wafer Fab Equipment

Bottom Electrode CMP

MTJ Stack Dep

MTJ Pillar Patterning

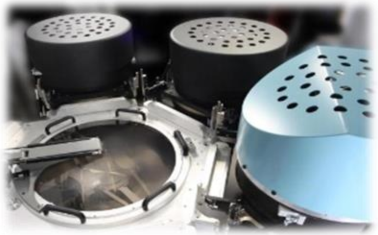
MTJ Etch & Encapsulation

Oxide Fill & CMP

LK Prime™

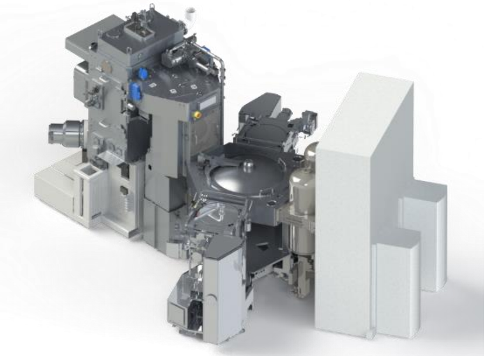
Endura™ Clover

Centura™ Sym 3



VeritySEM™ (Metrology)

Centura™



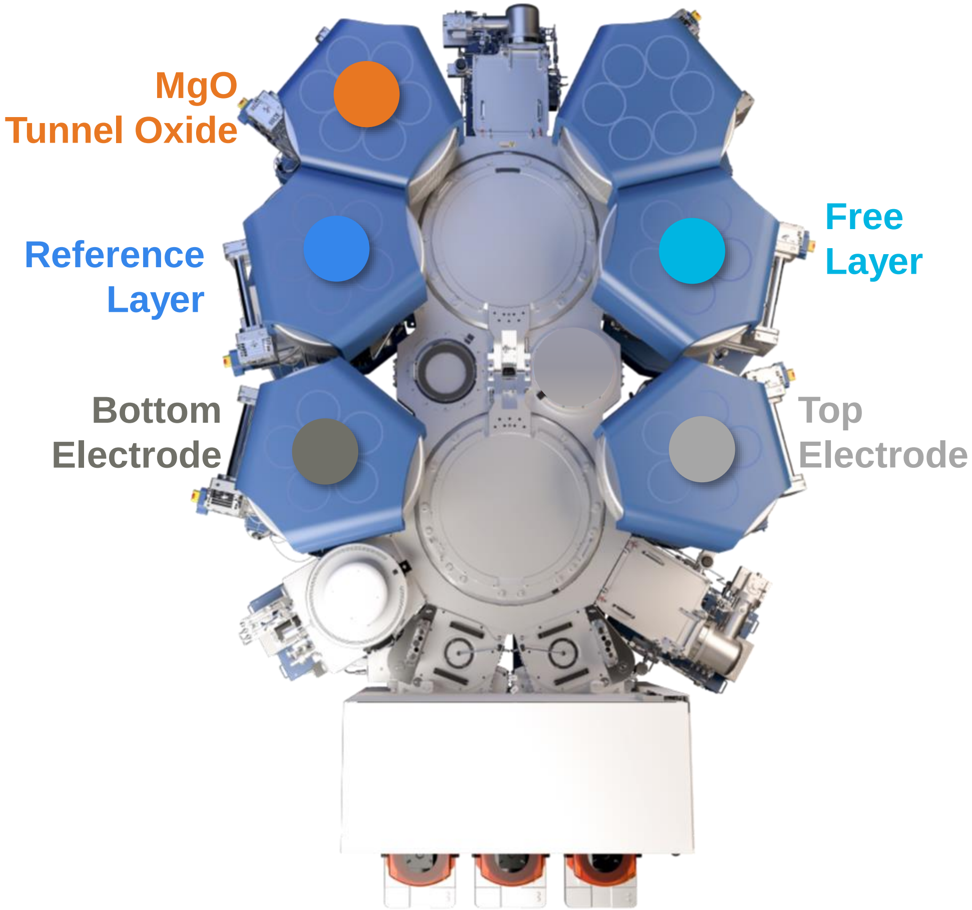
Producer™

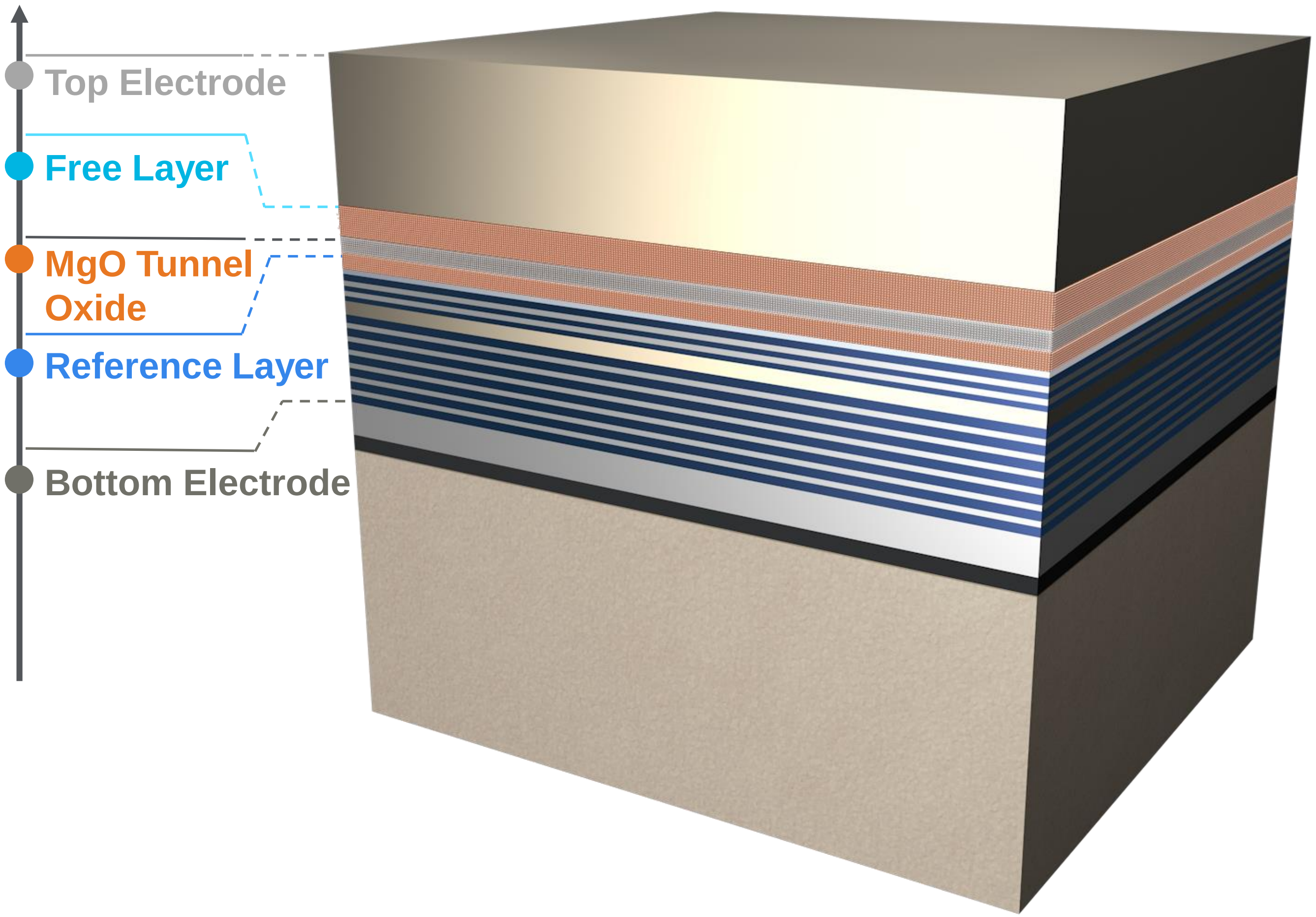
MTJ Stack Dep: Endura® Clover™ MRAM PVD System

- Ultra-high purity environment for pristine film and interface → **UHV platform (low E-9)**
- Complex cell stack → **Multi-cathode Clover PVD chamber**
  - Complex stack: 10+ materials with 30+ layers
  - Ultrathin film in the range of a few angstroms
- High quality tunnel barrier → **Clover PVD RF-MgO chamber**
  - Critical for high on/off signal and endurance
- Special treatments → **Cooling/Anneal chambers**
  - Surface preparation, thermal treatment for optimal performance
- Stability in HVM → **OBM real-time monitoring**

Additional details in talk NEWM-202B-1 on Wednesday

30+ Layers, 10+ Materials in Single Integrated System





Integrated Material Solution with Multi-Cathode Chambers for Complex MRAM Stack

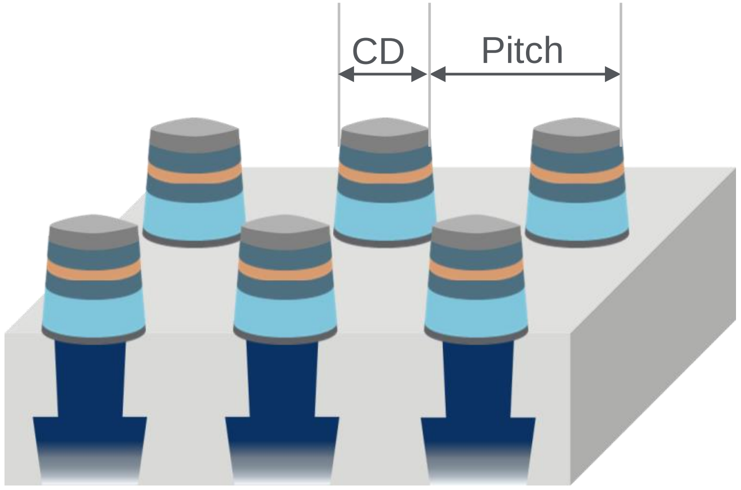
Additional details in talk NEWM-202B-1 on Wednesday

AGENDA

- New Memory Application Space
- Applied Solutions for MRAM
- MRAM Scaling (Process and Device)

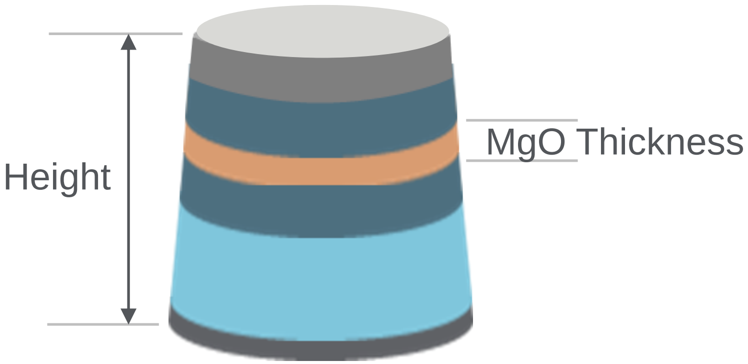
STT MRAM Scaling

Pitch and CD



Reduce pitch/CD to increase bit density (reduce cost / bit)

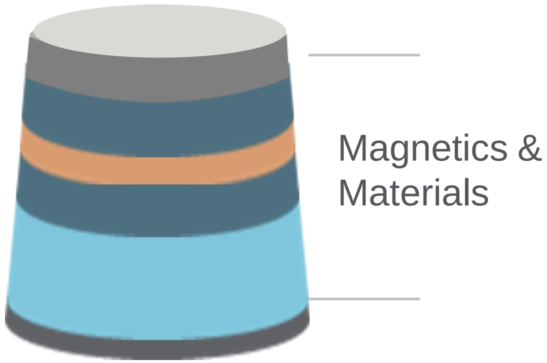
Stack Height / MgO Thickness (RA*)



Reduce height to maintain AR
Reduce MgO thickness to scale V_{DD}

Spin Efficiency

(~ Data Retention ÷ Programming Current)



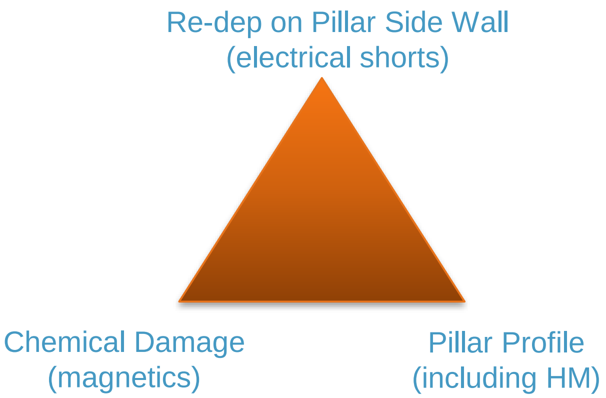
Material engineering to increase spin efficiency

** RA : Resistance-Area product*

Pitch Scaling

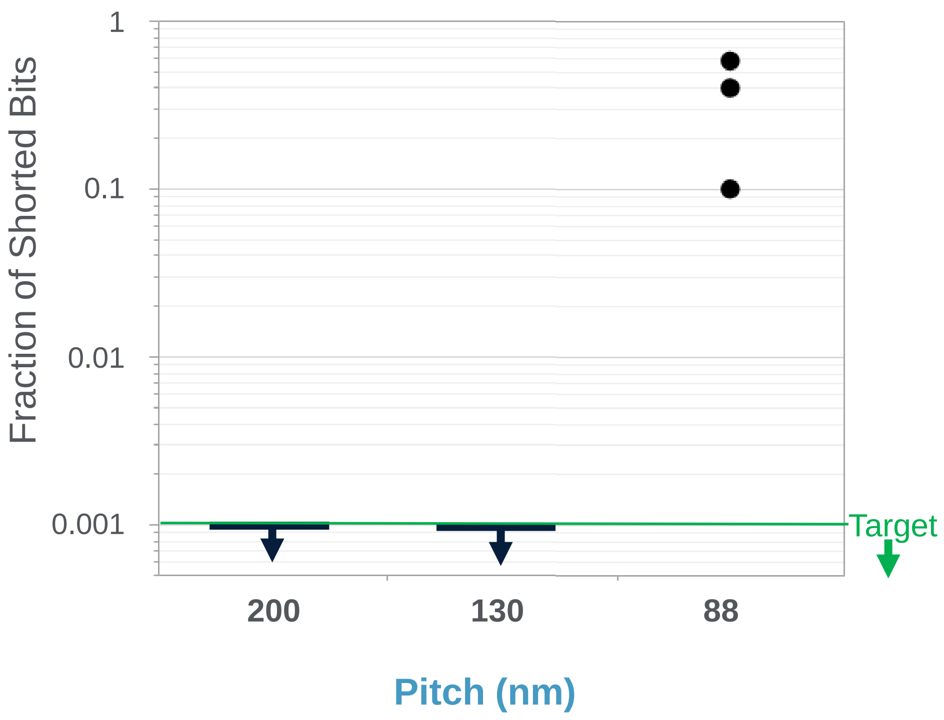
Key Scaling Challenge: Reducing yield loss (shorts and opens) as cell pitch shrinks

MRAM Etch Trilemma

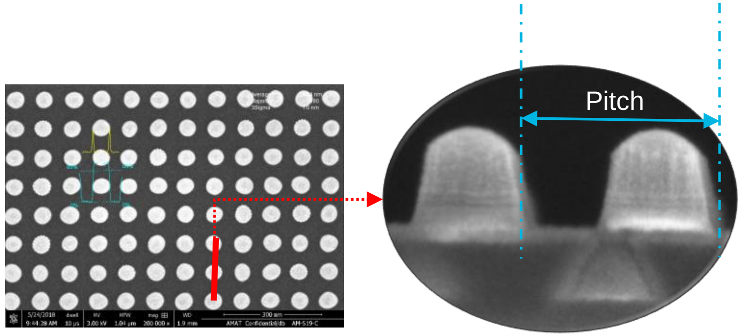


First order effects:
- Profile impacts yield (opens/shorts)
- Re-dep on pillar impacts yield (shorts)
- Chemical damage impacts performance

Shorts Versus Pitch



Etch Profile at 88nm Pitch



Pitch: 88nm;
Cell size: 0.008um^2

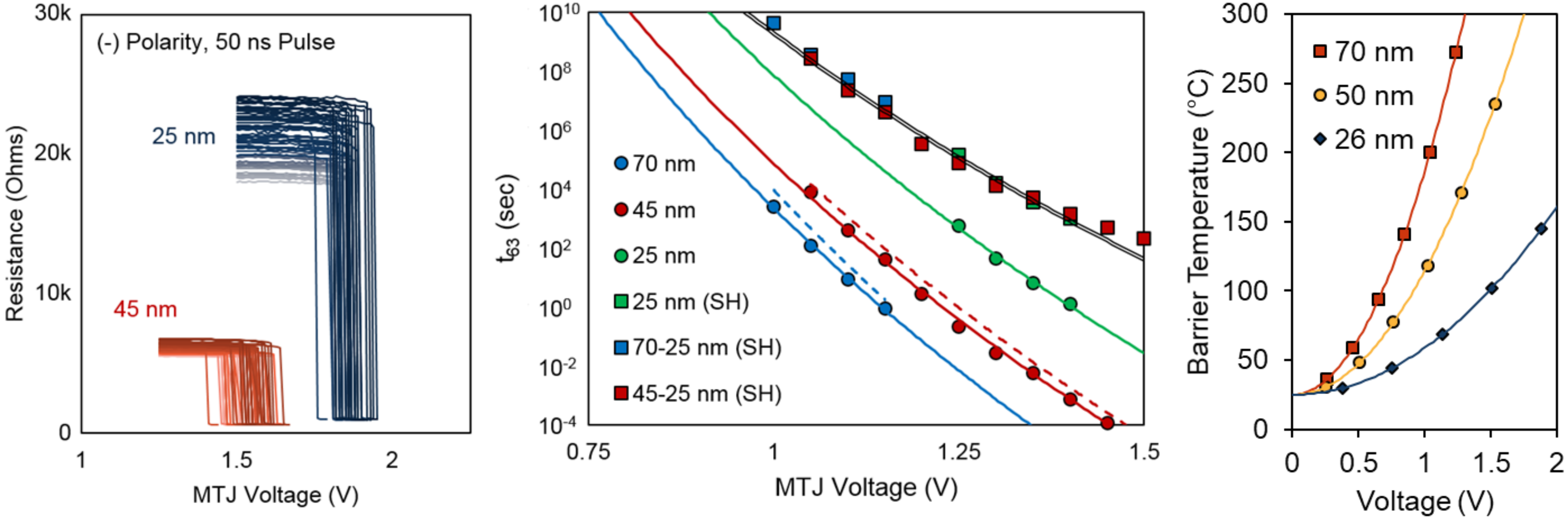
Applied Internal Data

Pitch scaling to next node (pitch ~ 130-150nm) demonstrated. Sub 100nm pitch area of development

CD Scaling

Key challenge: Maintaining / reducing device resistance to conform to V_{DD}. Benefit: Positive impact on endurance

Breakdown and TDDB dependence on CD



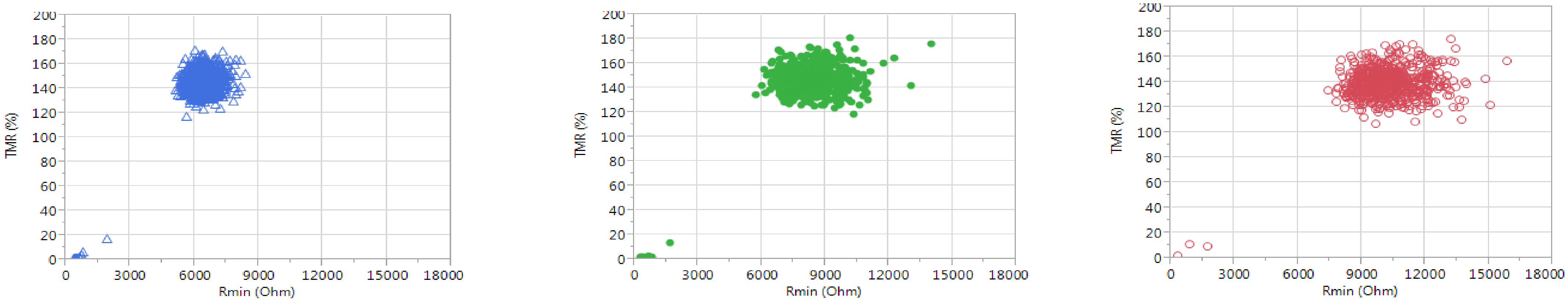
Qualcomm & Applied, (IEDM), Dec. 2016.

MgO tunnel oxide breakdown voltage / t_{63} improves as CD (size) is reduced from thermal effect

CD Scaling

Key challenge: Increased distributions for device resistance (and magnetics)

Resistance Distribution with CD


Pitch: 200 nm
CD: 55 nm

Pitch: 165 nm
CD: 50 nm

Pitch: 130 nm
CD: 45 nm

Applied Internal Data

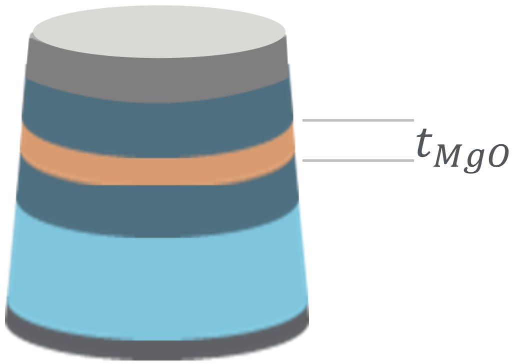
TMR%[1] constant with CD. Resistance distributions CV[2] slightly worse for smallest CD

---

[1] *TMR: Tunnel magneto-resistance*
[2] *CV : Coefficient of Variation*

MgO Thickness (RA) Scaling

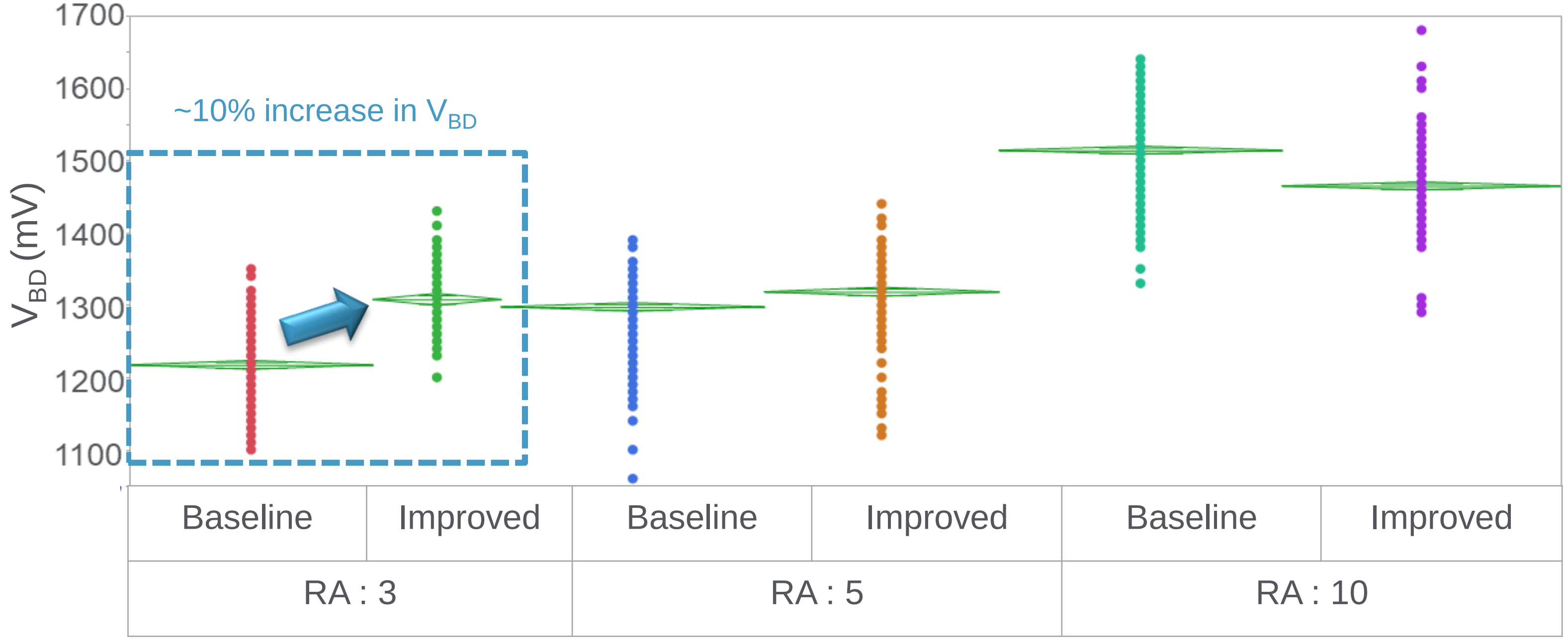
Reducing MgO tunnel oxide thickness to reduce Resistance and V_{DD}



$$RA \approx c * t_{MgO}{}^{n}$$

$$V_D = RA * J_c$$

MgO breakdown for two different MgO Tunnel Oxide Process



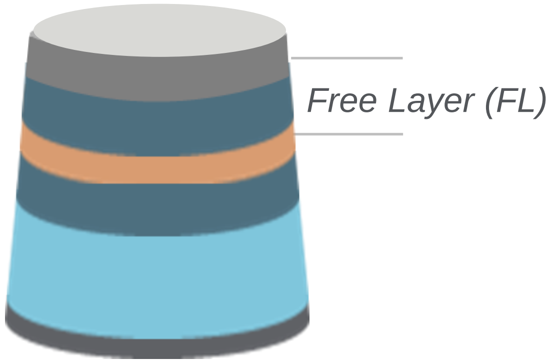
t_{MgO}: *MgO Thickness*

Applied Internal Data

MgO tunnel oxide breakdown voltage improved by optimizing PVD process / in-situ treatment

Data Retention at Low Programming Current (Spin Efficiency)

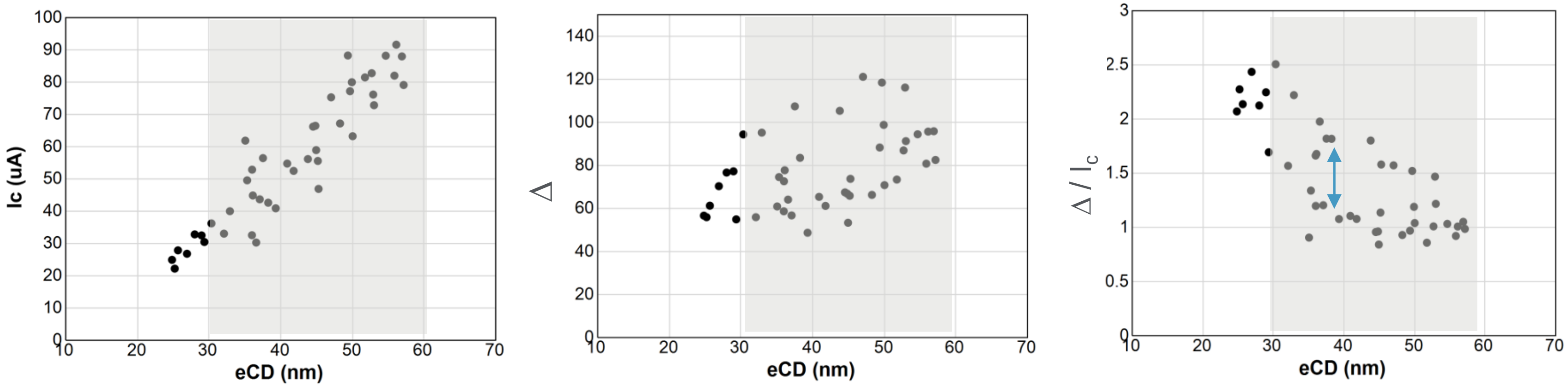
Key challenge: Maintaining data retention while reducing program current, as CD scales



Proxy for Data Retention: $\Delta = \frac{H_k m_{free}}{2k_B T}$

Programming Current: $I_{c0} = \frac{2e}{\hbar}\frac{\alpha}{\eta} m_{free}\left(H_{k,eff}\right)$

Programming Current (I_c), Δ and spin efficiency (Δ/ I_c)



Upto 2X increase in Δ / I_c value by materials engineering*

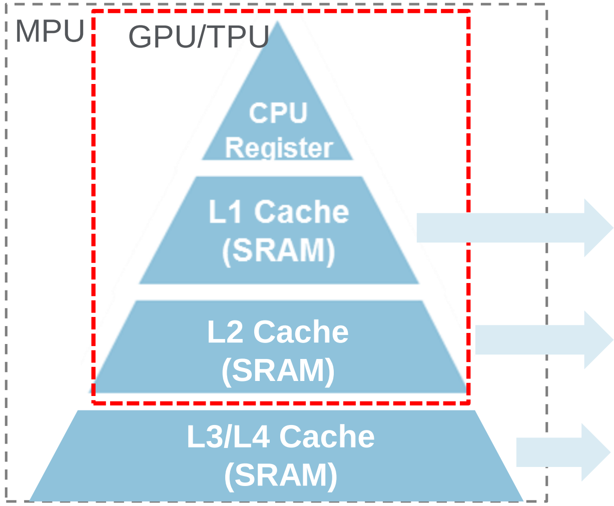
** Multiple free layer configurations used in these plots*

Applied Internal Data

Materials Engineering of PVD Stack enables longer data retention while reducing programming current

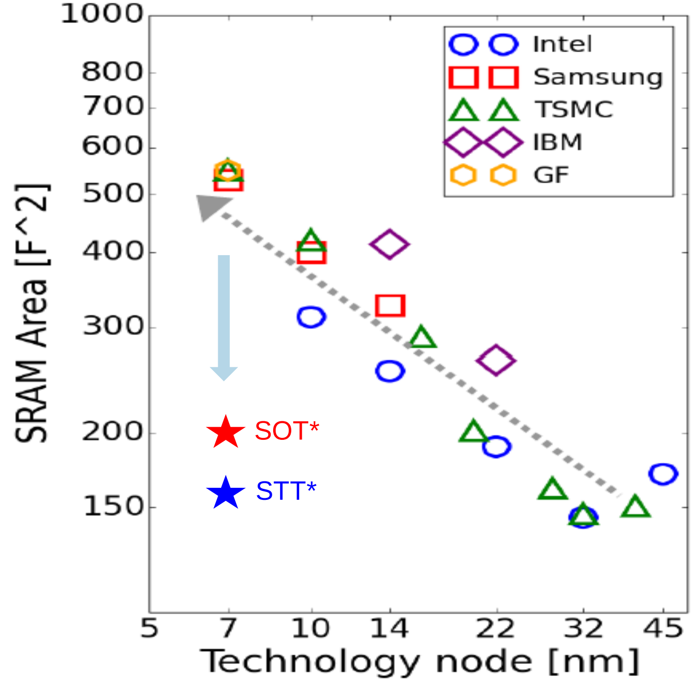
New Application: SRAM Cache Scaling and MRAM

Cache use in Processors



Latency (speed)	Size
< 1 ns	10's of KB
< 3 ns	100's of KB 10's of MB in GPU
< 5 - 10 ns	10's of MB

SRAM cell area scaling challenged



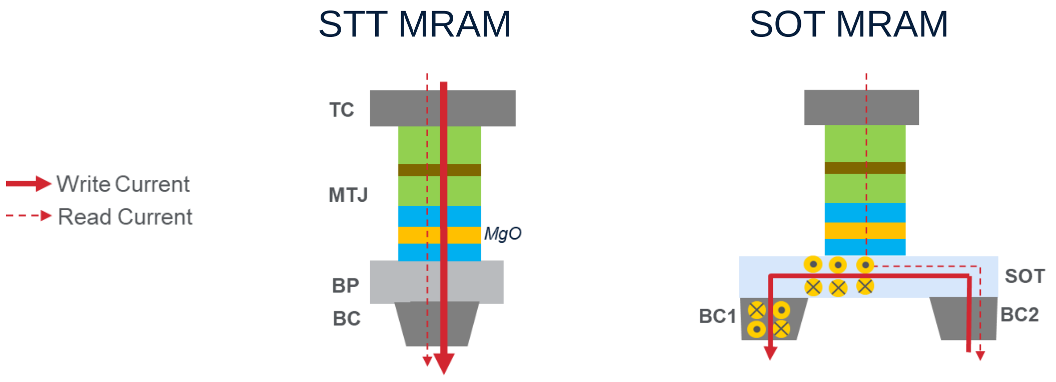
TDK, VLSI 2018

- MRAM has potential to replace SRAM as cache to increase density, if performance becomes comparable
- Additional applications possible due to non-volatility of MRAM

* Glossary
SOT : Spin Orbit Torque
STT : Spin Transfer Torque

Beyond STT MRAM: SOT MRAM for L1/L2 Cache

Difference & Similarities between STT and SOT MRAM



	STT MRAM	SOT MRAM
Read	TMR Effect	TMR effect
Write	Spin Transfer Torque	**Spin Orbit Torque**

Fast write of < 1 ns possible for SOT MRAM, potentially with infinite endurance (> 1E12)

Summary

- Multiple emerging memory technologies (STT MRAM, PCRAM and RERAM) entering manufacturing phase
  - Addressing different application (Embedded vs NV RAM vs SCM) in different markets (IOT, AI/Data Center)
- Manufacturing challenges with complex materials have previously limited new memory adoption → Innovative PVD and Etch Technologies enable High Volume Manufacturing
- Scaling path for STT MRAM beyond 22nm node is robust, with many options to improve performance and reduce bit cost that would further drive new applications
- STT / SOT MRAM are promising candidates for high performance non-volatile cache with higher density/capacity than 6T SRAM

APPLIED MATERIALS®

make possible