Short Loop Characterization and Tracking System for MRAM Process Development

Tomasz Brożek and Dennis Ciplickas

PDF Solutions, Santa Clara, CA

PDF SOLUTIONS

MRAM Landscape

- MRAM maturity very high for both Storage and eFlash replacement, and broad applications, including IoT and AI/ML
  - STT-MTJ in production, SOT-MTJ in development
  - 40nm and 28/22nm qualified, scaling to 14/16nm FinFET node
- Development and Manufacturing challenges
  - Learning cycles for development and process improvement very long and costly – no simple way to accelerate and reduce NRE
  - Process control monitors and in-line metrology incapable to catch excursions, tool drift and MRAM module variability, resulting in lower and unpredictable yields, observed only during wafer sort or final test
- New tools are needed for fast diagnostics and feedback across the full lifetime loop of MRAM product

MRAM DEVELOPER DAY

MRAM Difficulties

Recent STT-MRAM Technology: From Lab to Fab

Y. J. Song, Samsung Electronics Co., Ltd.

Advantages of Embedded STT-MRAM

- Key advantages: a simple structure and easy plug-in integration
  Low cost and easy migration into different baseline platform

Simple Structure

1T/1MTJ Embedded in 28 FDS
Just +3 Masks
*e-flash : +13~15 masks

MTJ Module

Plug-in Integration

- Easy plug-in between Cu metal lines

Bulk | FD-SOI | FinFET

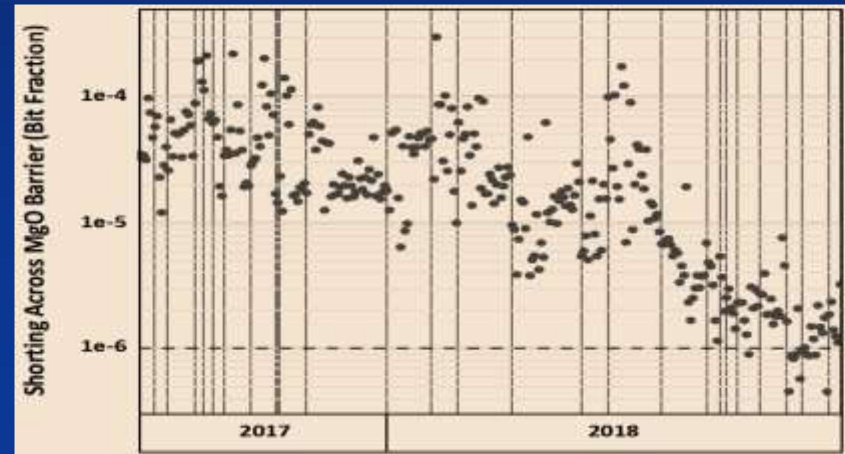
Symposia on VLSI Technology and Circuits — Slide 11

STT-MRAM Technology Difficulties

Physical Difficulty
- Very thin film (<10Å)
- Many metallic layers
- Ultra flat film
- Crystalline film
- Hard to pattern

Electrical Difficulty
- Small sensing margin
- Large switching current
- Stochastic behavior (soft fail)
- Process-induced degradation

Metrology Difficulty
- Ultra thin film monitoring
- Magnetic property measurement
- Shunting detection
- Retention measurement



Source: INTEL, IEDM'2018

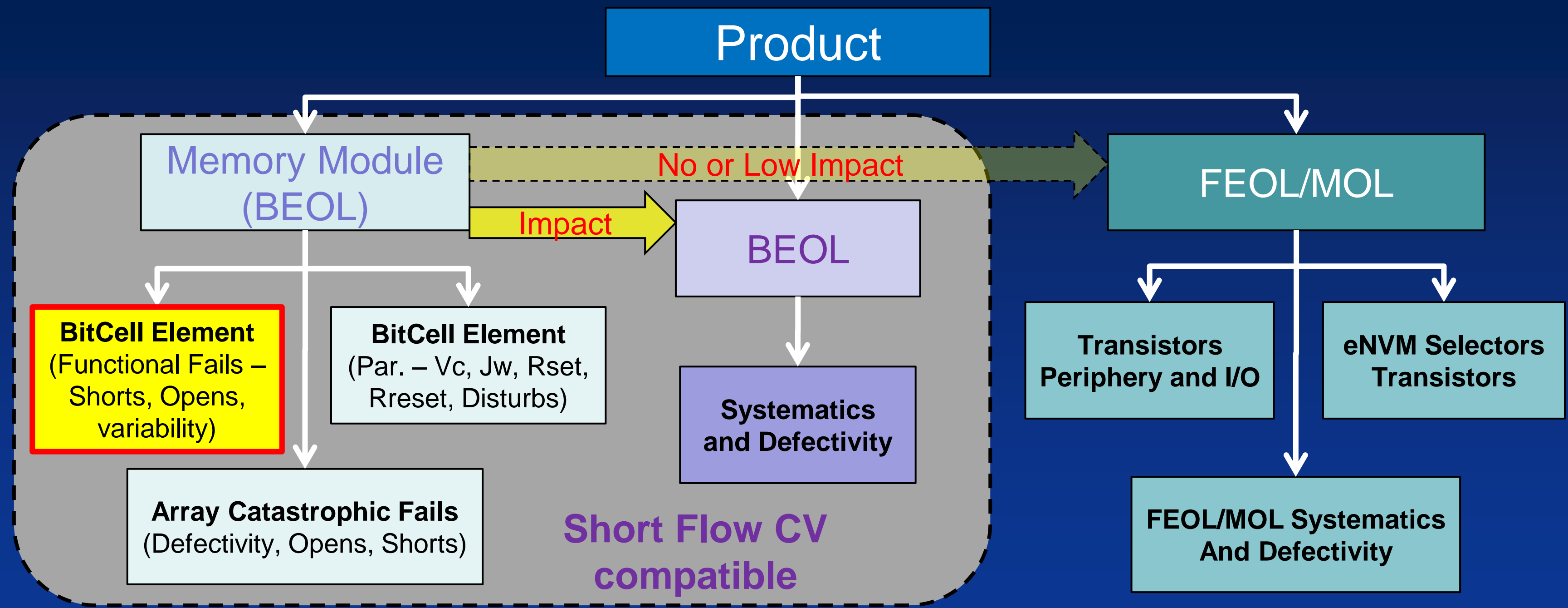
New tools are needed !!!

Agenda

- Proposed Electrical Characterization tool
- MRAM Characterization with Short Flow test chip
- Passive Arrays for MRAM cell statistics
- Challenges and test methodology
- Simulated results
- Applications
- Conclusions

MRAM DEVELOPER DAY

Characterization Needs for Development and Yield Ramp

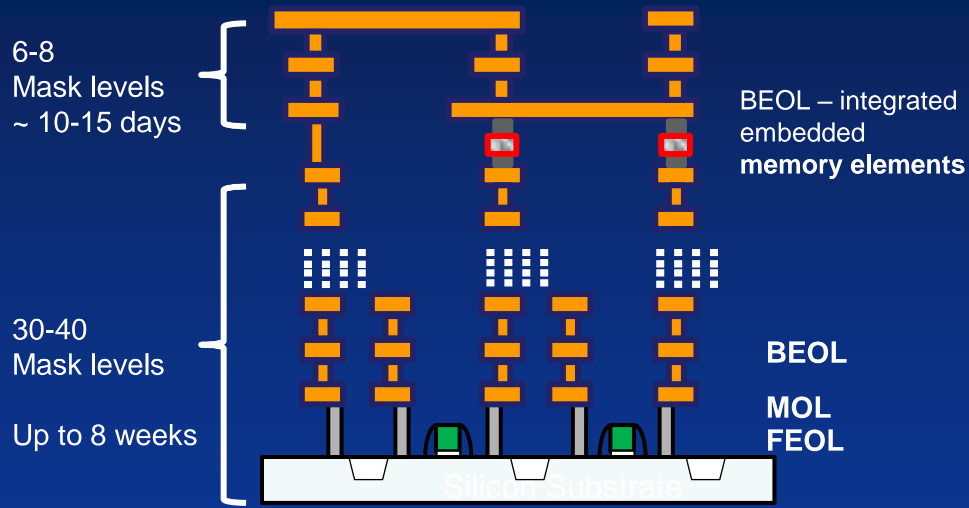


- Challenge – design test structures to characterize all areas/modules of MRAM Chip

Full Flow vs Short Flow approach

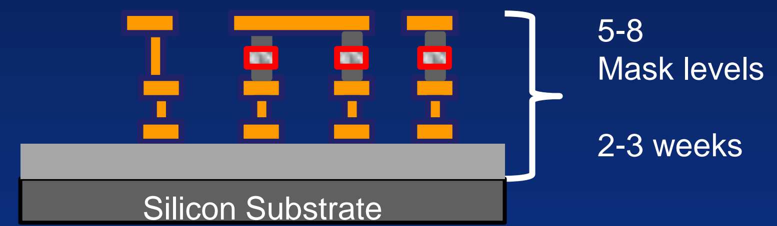
MRAM DEVELOPER DAY

Full Flow Test Vehicle with Memory Array



Benefits	Challenges
➢ Full Memory Characterization ➢ Large Statistics ➢ Bitmapping and Localization ➢ Fast Testing	➢ Long Processing time ➢ Sensitivity to other failure modes ➢ Wafer Cost ➢ Parametric Characterization

Short Flow Test Vehicle with Isolated Bits



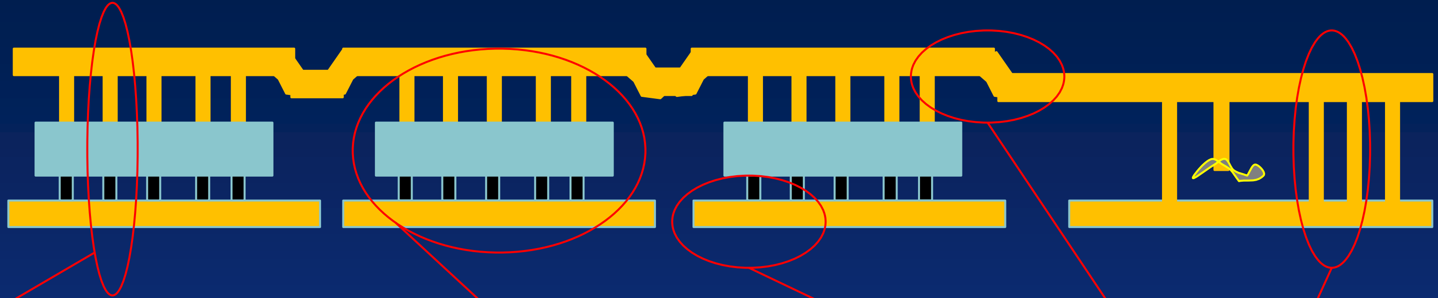
Benefits	Challenges
➢ Short Processing Time ➢ Lower Cost ➢ Good Parametric Characterization ➢ Fast Learning Cycle	➢ Low Statistics ➢ Long Testing Time ➢ Product-like Test Conditions

PDF SOLUTIONS

MRAM DEVELOPER DAY

Short Flow Characterization Content

High density, fast-testable test structures



Single Bit
- 1R (or 1R-1R) configuration
- Parametric extractions and Variability
  - Array Location effects
  - Misalignment Process Window
- Early Reliability study
  - Endurance Cycling
  - Retention studies
  - Disturb studies

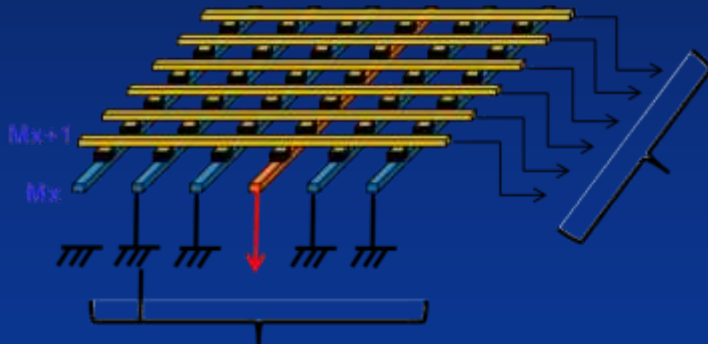
Bit Statistics
- **Passive Arrays** – millions of Bits/wafer
- Cell functionality statistics
- Bit failure Binning
- Switching parameter Binning
- Fail Bit mapping
  - Within Array fails
  - Across wafer fails
  - Failure Analysis support

Failure Modes
- Array Failure Modes
  - BitLine and Wordline failures
  - Array edge effects (patterning, Loading effects, CMP planarity)
  - Via Opens/Shorts
  - TE/BE Opens and Shorts
- Impact on Logic BEOL
  - Toll Via patterning and fill
  - Memory material residue

MRAM DEVELOPER DAY

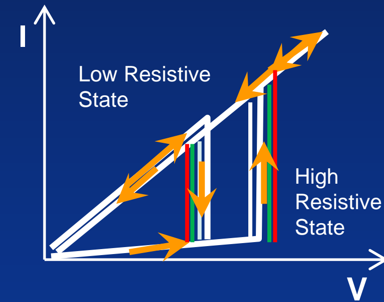
MRAM – Bit in Cross-Point Array

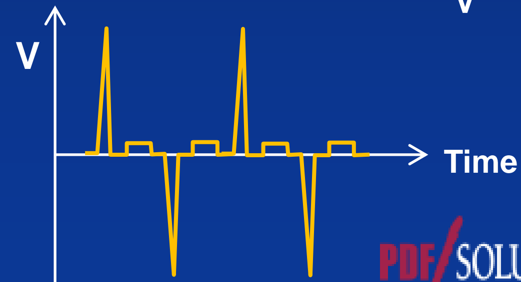
- Cross-Point Array enables high Bit count per test pin
- Parallel testing of Bits in the Arrays speeds up the test
- Compatible with many emerging memory types
- Compatible with +2- or +3-mask integration
- Supports Short-Flow learning cycles



16 - 128 WL connections
Program and Read on multiple Cells

16 - 128 BL connections
- Simultaneous Read on all BL's
- I-V sweep collection
- Pulse opearation



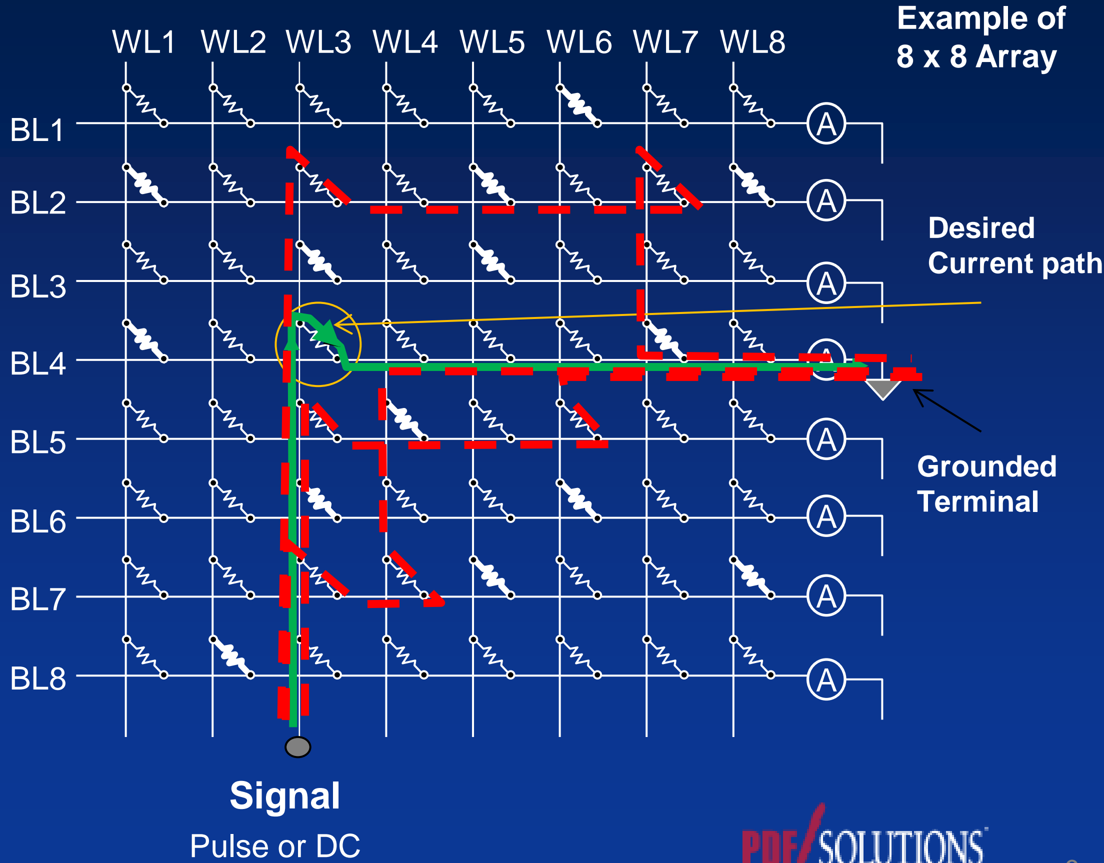


PDF SOLUTIONS

Testing Challenges – Sneak Leaky Paths

Cross-Point arrays suffer from the so-called Leakage Sneak Path effect

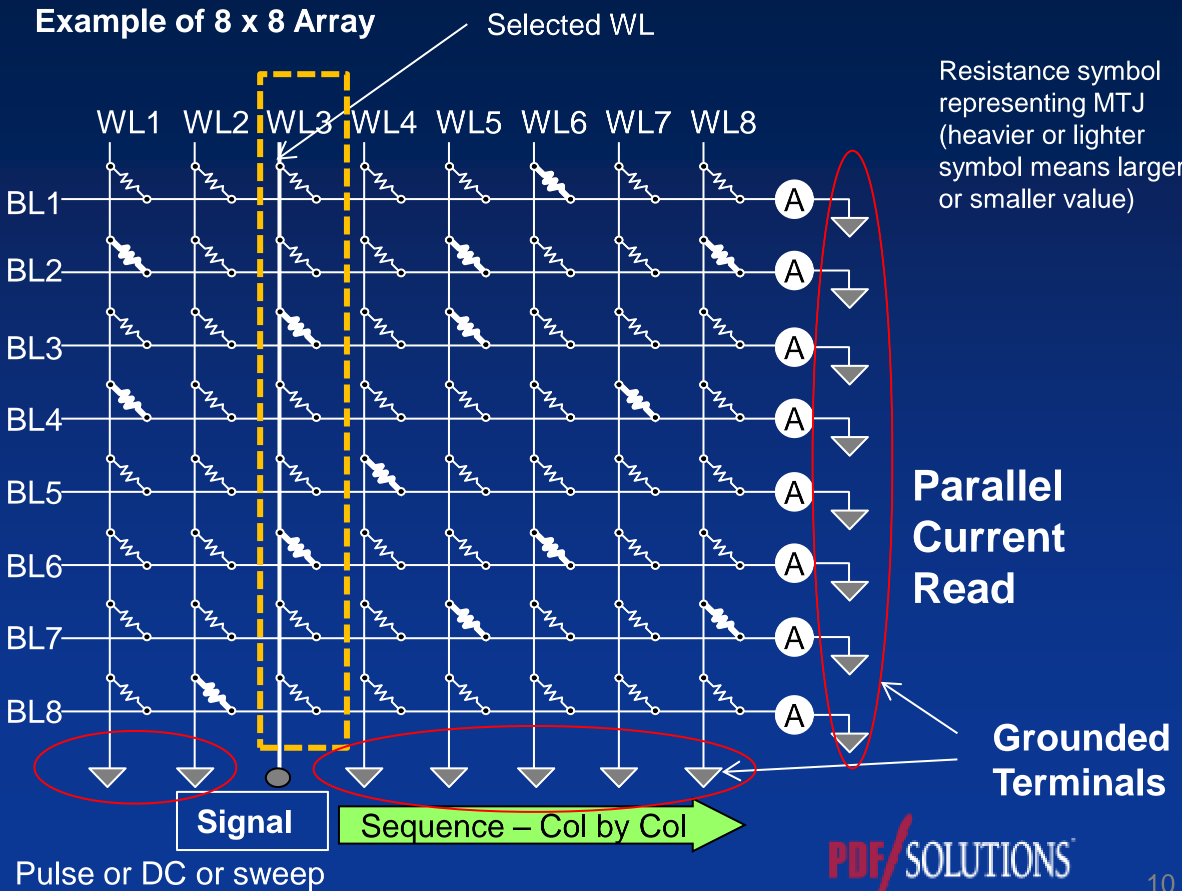
→ there are multiple parallel current paths, which introduces an error in measurement of a single Resistive element at a crossing of a single Column and a single Row



Ideal Case with Ideal Array

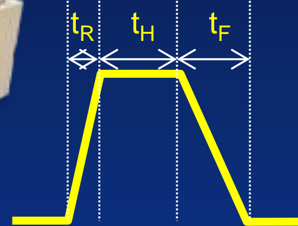
- General Idea of testing the Cross-Point Array to avoid Sneak Leakage Path – avoid Voltage drop between neighbor WL's and Neighbor BL's

The current flows only from the selected WL to the grounded terminal of the BL's through the highlighted memory elements. All other memory elements are not biased as they are between two grounded BL and WL



Array Test - Multi-channel Parametric Tester

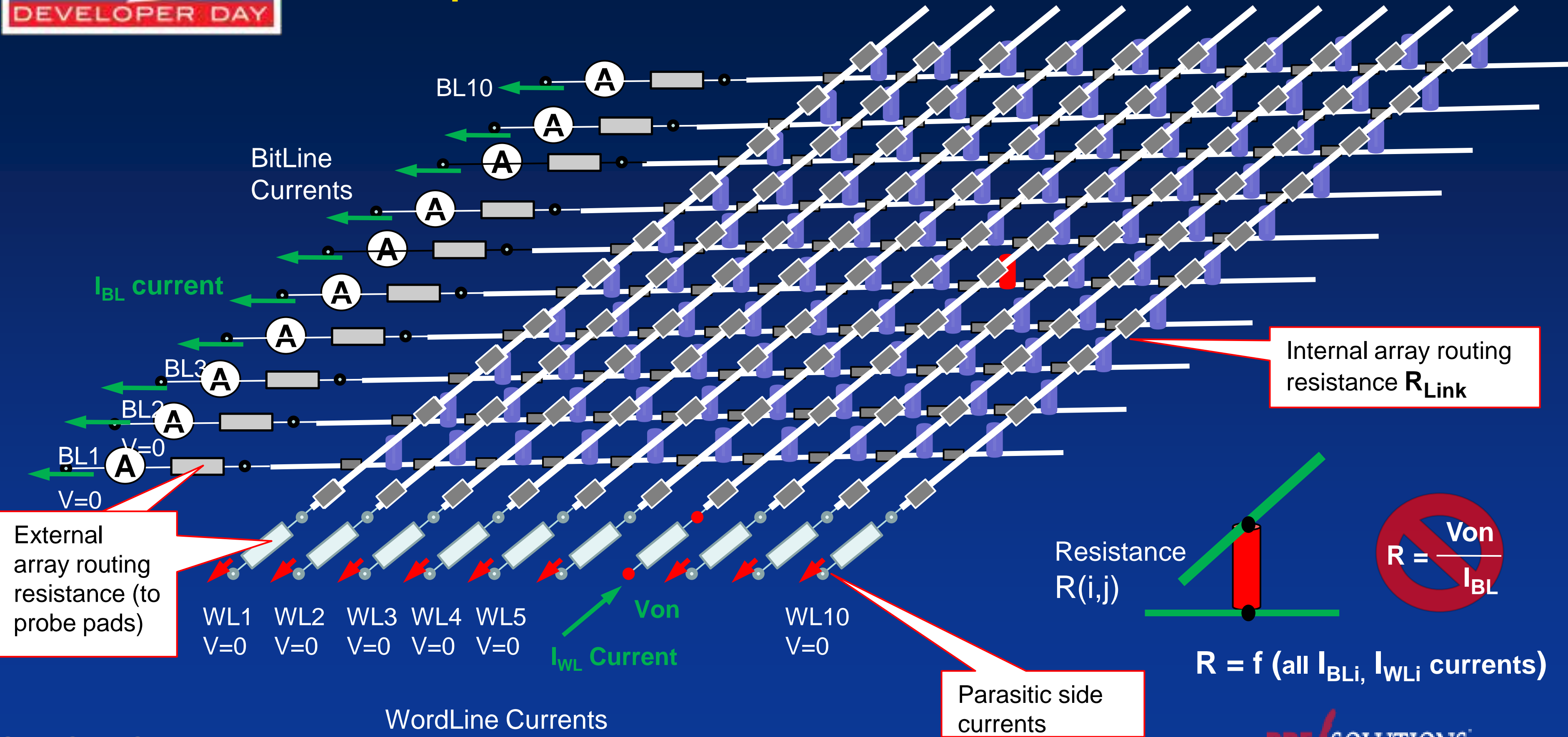
Characteristics	pdFasTest®
Voltage Force Current measure	256 independent parallel dual-port channels
Arbitrary Waveform Pulse Voltage Output	Waveform Generator Various ranges, application specific
Channel synchronization	All channels can be synchronized
Rising/Hold/Fall time	Nano-sec range for Memory testing
Leakage measurement	pA range
Dynamic Current measurement during pulse	Possible on selected channels



pdFasTest® enables parallel testing of Bits in Arrays with cross-point configuration, including high-speed P/E pulses and full parametric characterization of the Rows/Columns

PDF SOLUTIONS

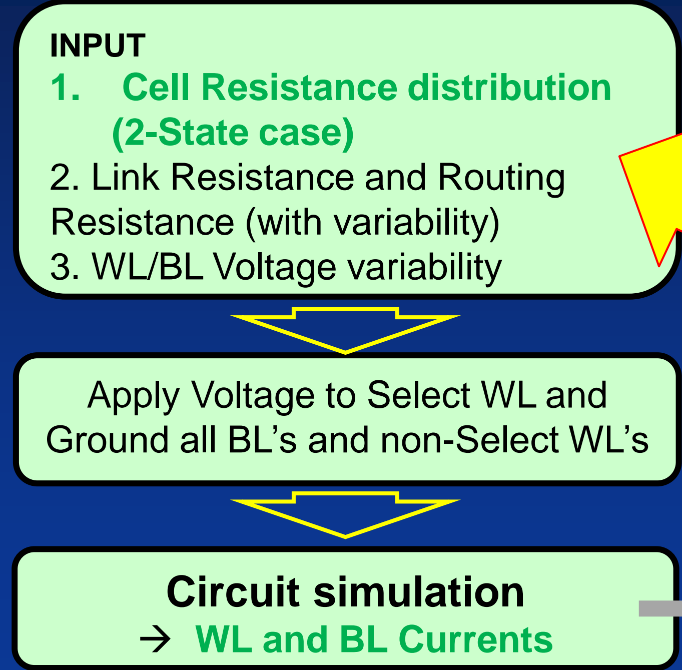
Impact of Parasitic Elements

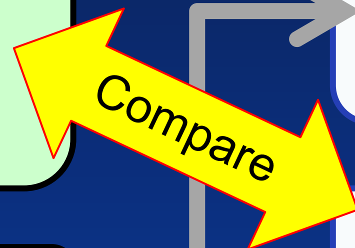


How Much Parasitics Can We Tolerate?

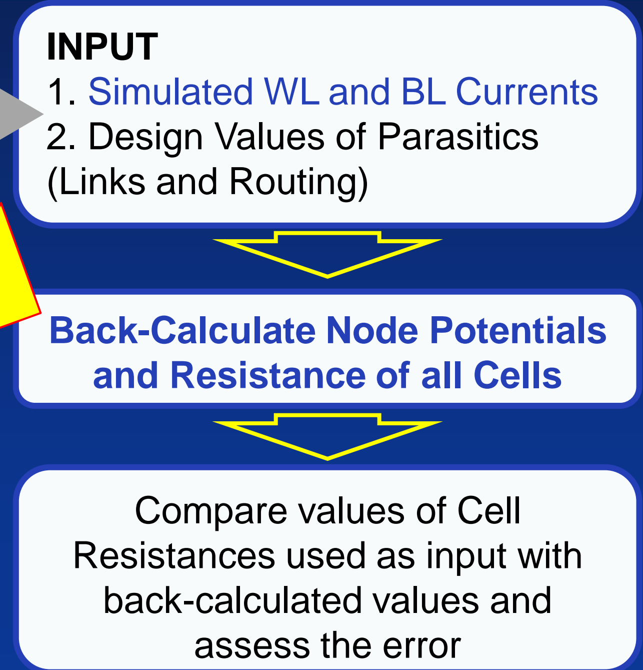
Test Algorithm to Account for Parasitics

Simulate Real Case Test – Including Variability





Simulate Resistance Extraction



Resistive State Detection Capability

- Mix of Cells with R_{PP} (1 kΩ) and R_{AP} (2.5 kΩ)
- Variable RLink - by Design & Process
- Good Margin to distinguish Cell state

MRAM – Array with 50% Low Resistive (1 kOhm) and 50% High Resistive State Bits (2.5 kOhm)

Resistance – Cum Plot

2 Ohm Links

High Resistive State Bits

Low Resistive State Bits

2 Ohm Links +/- 30% variation

2 Ohm Links 30%variation BL source Voltage var

20 Ohm Links +/- 30%

Simulated Test result

Input Resistance

Memory Element Resistance

Error

mram-R=1000-noavar02-novvar

mram-R=1000-wavar02-novvar

mram-R=1000-wavar02-wvvar

mram-R=1000-wavar20-novvar

2 Ohm Links

2 Ohm Links +/- 30% variation

2 Ohm +/- 30% Links BL source Voltage var

20 Ohm Links +/- 30% variation

Low Resistive State Bits

High Resistive State Bits

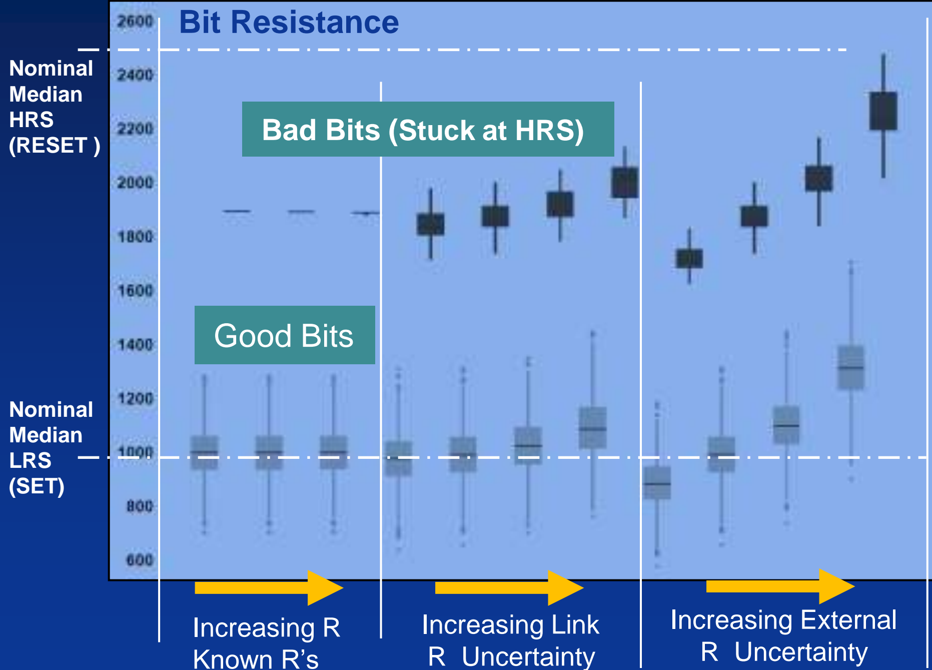
Memory Element Resistance

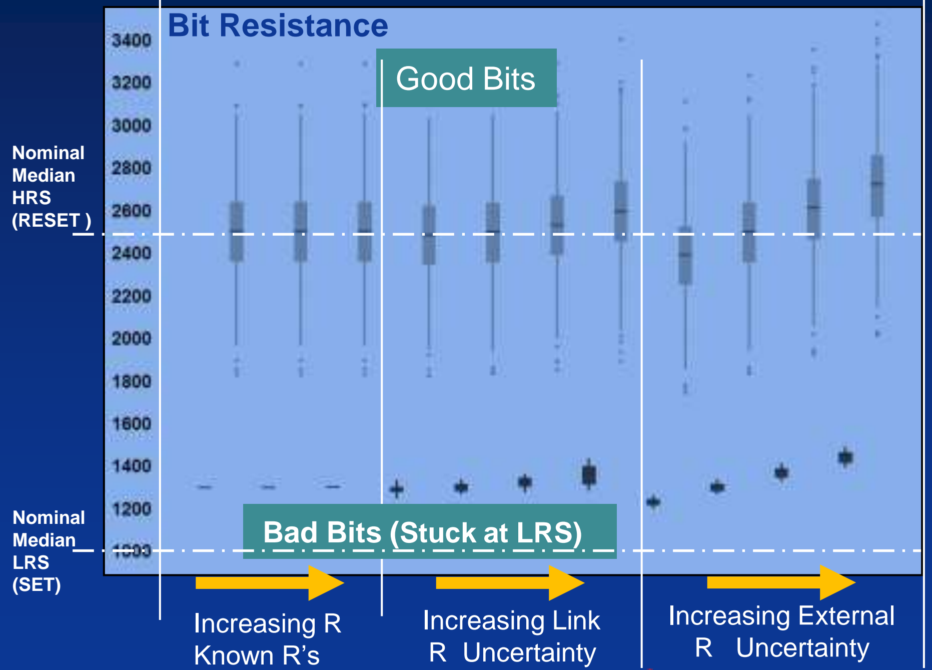
PDF/SOLUTIONS

Outlier Bad Bit Detection

- Stack at HRS (R_{AP}) and LRS (R_{PP})
  - Bad Bit stuck at Opposite State with 3σ from Nominal Median

10 x 10 Arrays

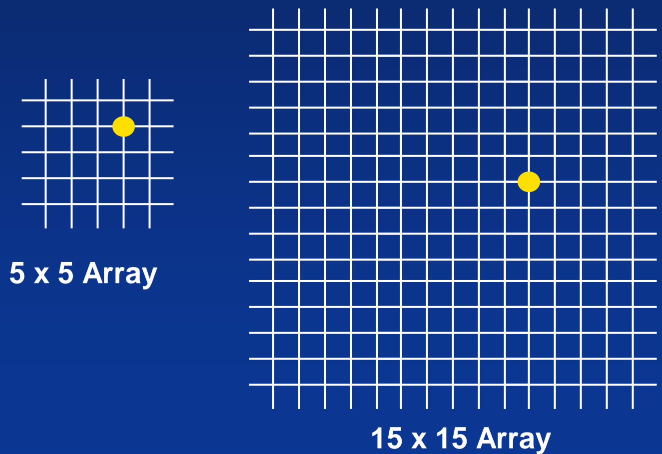




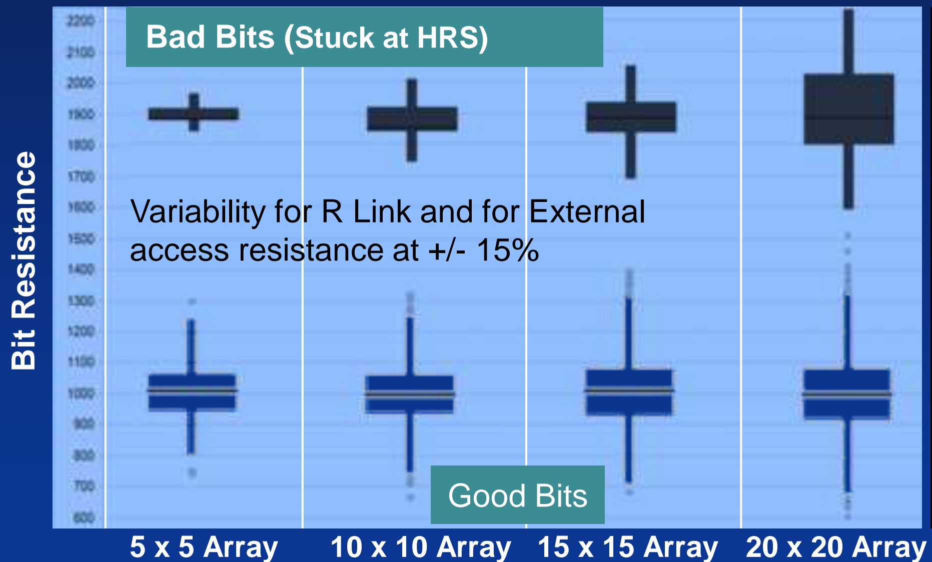
MRAM DEVELOPER DAY

Outlier Bad Bit Detection – Array Size

- Impact of Parasitics and variability increases with the Passive Array size
  - Reduce the Parasitics by Design and monitor Process Variability
  - Need to balance the Trade-offs



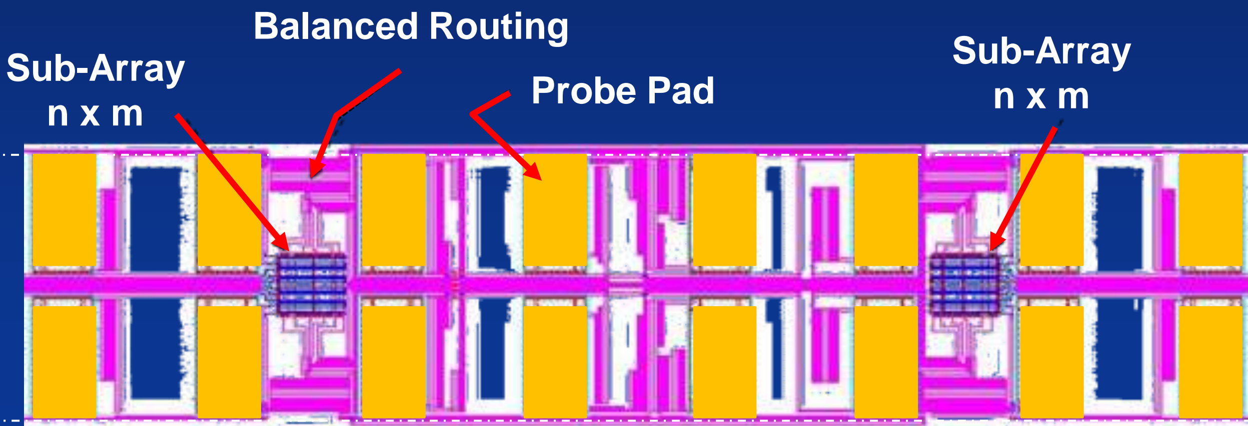
Simulation of 10 arrays with a single bad bit



PDF SOLUTIONS

MRAM PA – Test Structure Design

- Balance the trade-offs between Array size and Test Error due to Parasitics
- Minimize the resistance between neighbor tested bits inside the Array
- Minimize Routing resistance between the Array and the Probe pads
- Provide well controlled Ground connection to all unselected terminals

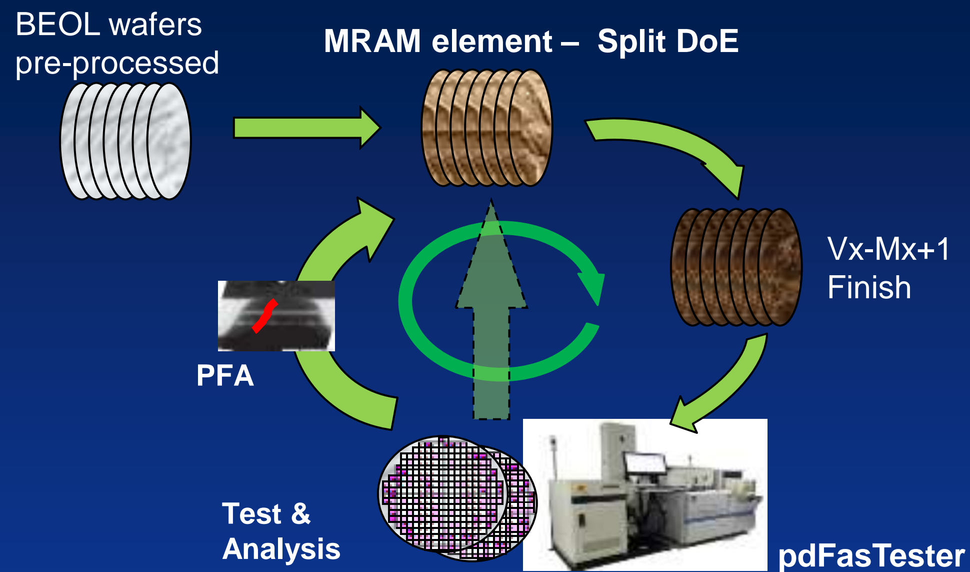


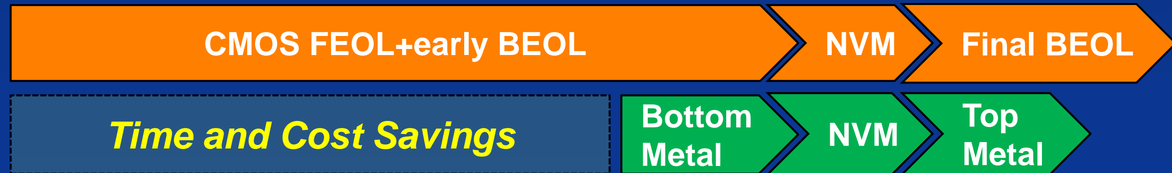
Proven Design

MRAM DEVELOPER DAY

Short Flow characterization Loop for MRAM

- Short Flow to Build Passive Arrays to test MRAM elements (design representing real array)
- Short manufacturing cycle - Start at Mx, process MRAM and Vx, and test at Mx+1
  - Fast TAT for processing
  - in-line testable
- Reduced cost
  - Low Mask count
  - Low cost wafers for experiments (no CMOS)
  - Smaller number of process steps





MRAM DEVELOPER DAY

Manufacturing control

Recent STT-MRAM Technology: From Lab to Fab

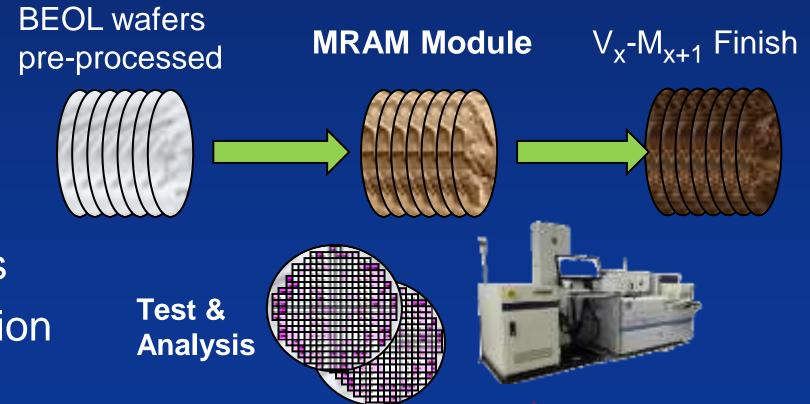
Y. J. Song, Samsung Electronics Co., Ltd.

Challenges for Mass Production

- **Consistency**
  -. Maintain the quality as a function of time and H/W variation
- **Process Margin**
  -. Process margin should be large enough to tolerate process variation
- **Equipment Compatibility**
  -. Process should be compatible with various machines

Problem:

- No good in-Line monitor for consistency of quality of multi-layer stack Deposition and Etch
- Long delay to get the feedback from Memory Array test
- Large number of wafers at risk in case of equipment drift of PM release hidden issues



- Use Short Flow Test Chip with a 3-day cycle time to monitor key Deposition and Etch Steps and Tools
- Implement Test Chip based Tool release to production after scheduled PM and unscheduled downtime

PDF SOLUTIONS

Summary

- We developed characterization tool for electrical evaluation of MRAM cells in stand-alone and embedded arrays
  - Millions of bitcells can be tested for statistical characterization
  - The test structures can be used with Short Flow wafers with no FEOL and selector/addressing circuitry
- Using resistive array simulation we demonstrated test capabilities and resolution which enables detection of bad bits
  - Proprietary parametric tester with high parallelization and pulse capabilities provides accurate testing with acceptable test time per bit
  - Test structure design for Passive Array testing needs to be carefully optimized to minimize test and resistance extraction errors
- Proposed Short Flow methodology supports accelerated MRAM development, scaling, and porting to next nodes, as well as provides a fast TAT tool for manufacturing control and tool monitoring

Acknowledgements

This work was a team effort done at PDF, and could not be achieved without

- Christopher Hess
- Hendrik Schneider
- Yuan Yu
- Christoph Dolainsky
- Rakesh Vallishayee
- Tuan Pham