MRAM Developer Day 2019
MRAM Update

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Chiplets and MRAM

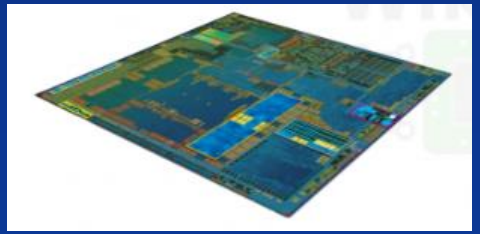
ABSTRACT: Avalanche Technology will offer MRAM chiplets based on its pMTJ STT-MRAM technology. Avalanche's MRAM chiplets use Generic MRAM Interface (GMI). The GMI is modeled on the widely-used HBM interface and is optimized for memory accesses. In addition to the memory interface, MRAM chiplets will usually need a second interface to communicate with the rest of the chiplets in a multi-chiplet system. For example, Intel's Advanced Interface Bus (AIB) protocol is in the forefront for direct chiplet-to-chiplet communication for DARPA's CHIPS (Common Heterogeneous Integration and Intellectual Property (IP) Reuse Strategies) program. To be used in AIB-based systems, an MRAM chiplet will need an AIB interface and an adapter from the AIB to the HBM interface for the MRAM array. This session will discuss GMI and AIB interface analogies and show the path for a GMI to AIB translator.

Chiplets and MRAM

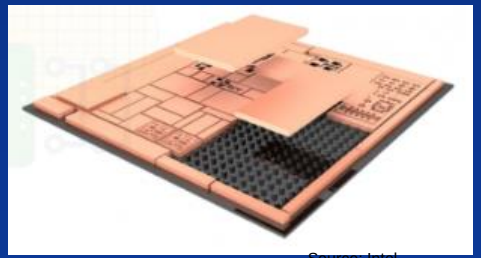
Chiplets Architecture – **Independent constituents making up a large chip built out of multiple smaller dies**

- The silicon Industry is spearheading the creation of an industry-wide ecosystem of discrete modular, reusable IP blocks, which can be assembled into systems using integration technologies
- Designers can mix and match the desired chiplets from many different vendors based on their specific needs
- One interconnect option is Intel's advanced interface bus (AIB) interconnect as an interconnect standard for chiplet architecture

Today's Monolithic



Chiplet - Modular



Source: Intel

Today's ASIC Flow

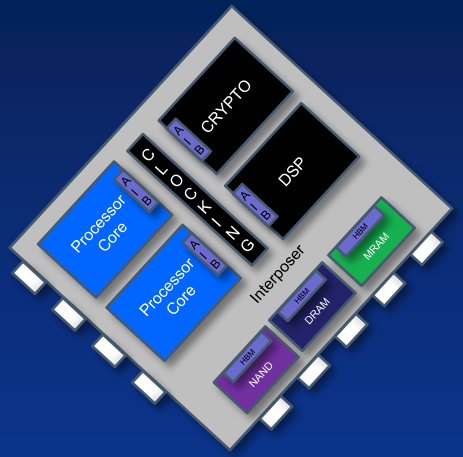
- Purchase IP
- Configure IP
- Connect & Test
- Close Timing
- Manufacture
- Package Design
- Assemble & Test

Chiplets ASIC Flow

- Purchase Chiplets
- Package Design
- Assemble & Test

Chiplets and MRAM

- Heterogeneous Integration Advantages
  - Mix and match processes, functions, etc.
- Time to Market advantages
  - No need to port all functions to a single new technology node
- Focused investment
  - Research and development on those portions of the chip that can be profitably shrunk
- Higher Yields
  - Smaller dies waste less wafer area



Die-to-Die Physical Interface

Two emerging interface standards for chiplets:

- Intel's Advanced Interface Bus (AIB) is one die-to-die PHY level standard
  - AIB is a clock-forwarded parallel data transfer protocol similar to DDR DRAM
  - Maximum frequency is 1GHz
  - Needs advanced packaging with 2.5D interposer technology
  - Higher level protocol stacks can be built on top of AIB (e.g. PCI Express)

- High Bandwidth Memory (HBM) Interface is another die-to-die standard specifically for high performance RAMs
  - Very wide bus - 128-bit channels per die for a total of 8 channels
  - Channels are completely independent running at frequencies up to 500MHz
  - HBM2 and HBM3 standards can achieve higher throughput
  - Needs advanced packaging with 2.5D interposer technology

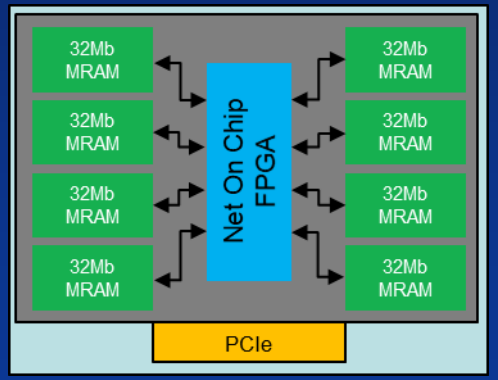
Avalanche's MRAM Chiplets

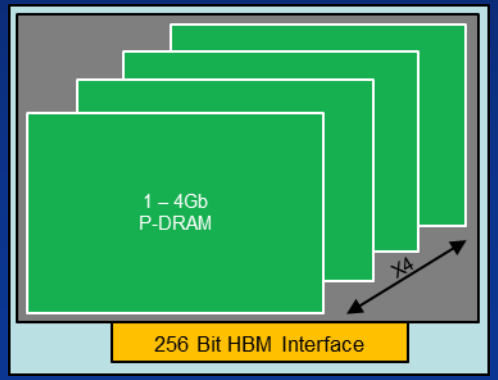
Phase 1

- MegaChiplet Implemented as PCIe solution
- MegaChiplet is based on Avalanche Technology's Current P-SRAM
- Services densities up to 512Mb
- Providing low latency non-volatile memory solution for HPSC Chiplet Platform

Phase 2

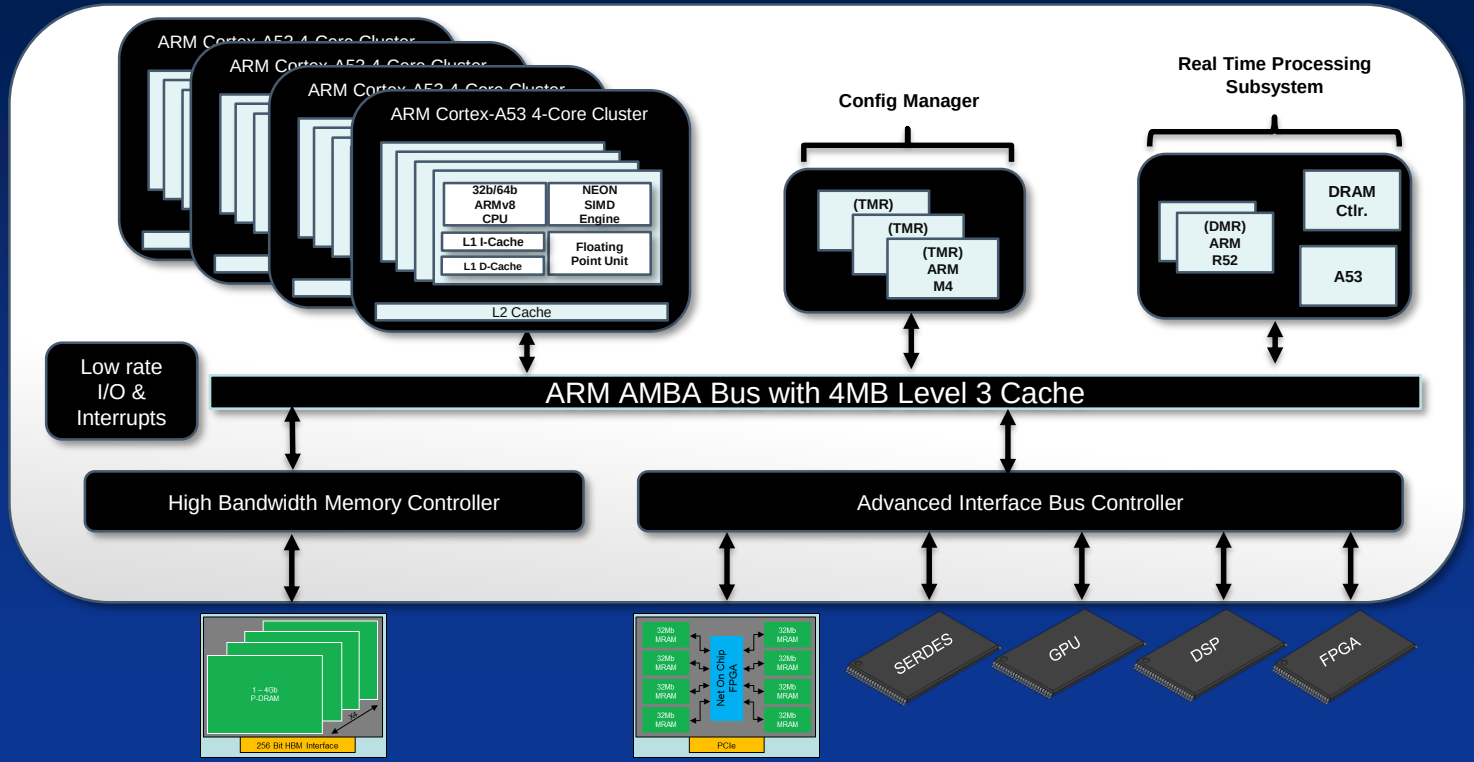
- NextGen Chiplet will be based on Avalanche Technology's Persistent DRAM technology
- Will incorporate HBM interface natively
  - FPGA/ASIC Translator not required
- Service densities up to 16Gb





Information processing engines with P-SRAM for Neuromorphic Computing

High Performance Computing



Chiplet Architecture Evolution – High Performance with Flexible Mixed Signal Macros

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Thank You