# MRAM Developer Day
# 2019 MRAM Update

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# Disclaimer

- Observations and opinions…

- ~40 years experience in wide variety of memory
- >13 years experience in MRAM
- 2012-2017 CEO/Chairman at Spin Transfer Technologies, Inc.
  - 2006-2012 Crocus Technology
- Currently consulting for young companies in emerging memory technologies

# MRAM ~~at the~~ Just Out of the Gate

MILESTONE!

| | <2007 | 2008 | 2010 | 2012 | 2017-18 | 2019 |
|---|---|---|---|---|---|---|
| Maximum Standalone Density | <4Mbit | 4Mbit | 16Mbit | 64Mbit | 256Mbit | 1 Gbit |
| Magnetic Technology | GMR | MTJ Toggle | MTJ Toggle | MTJ Spin Transfer In Plane | MTJ Spin Transfer Perpendicular | MTJ Spin Transfer Perpendicular |
| Leading CMOS Support | ~180nm | 180nm | 130nm | ~90nm | 28-40nm | 22-40nm |

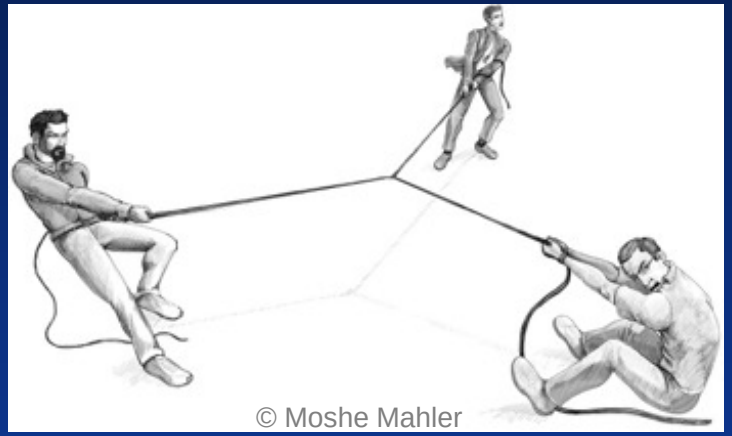
Scaling Barrier Breakthrough

~ $10^8$ units shipped

# 3rd Generation Constraint:
## STT MRAM 3-WAY Tug of War

**Write Current**
RETENTION

**Write Voltage**
ENDURANCE




**Write Pulse Width**
SPEED

**3rd generation STT MRAM cannot simultaneously provide speed, endurance, and retention for high speed SRAM application –**

**typically, speed and endurance sacrifice retention**

# Four+ Generations of Production MRAM

| Gen.1 | Gen.2 | Gen.3 | Future Gen.4 | Beyond Gen.4 |
|---|---|---|---|---|
| Toggle (2006) | Planar STT (2012) | Perp. STT (2018) | SOT | Volt. Cont., Multiferroic |
| Not Scalable beyond 130nm (write power) | Not Scalable beyond 65/40 nm (retention) | Fully scalable Endurance-Retention-Speed tradeoff → **Limited persistence and/or endurance and/or speed** | Fully scalable Infinite endurance + high intrinsic speed = persistent RAM compatible | |


KEY OBSERVATIONS:

- **Embedded STT will never replace conventional SRAM in SOC**
- **SOT promises to remove STT write endurance constraint**

# The Big News: Manufacturing Ramp at Foundries

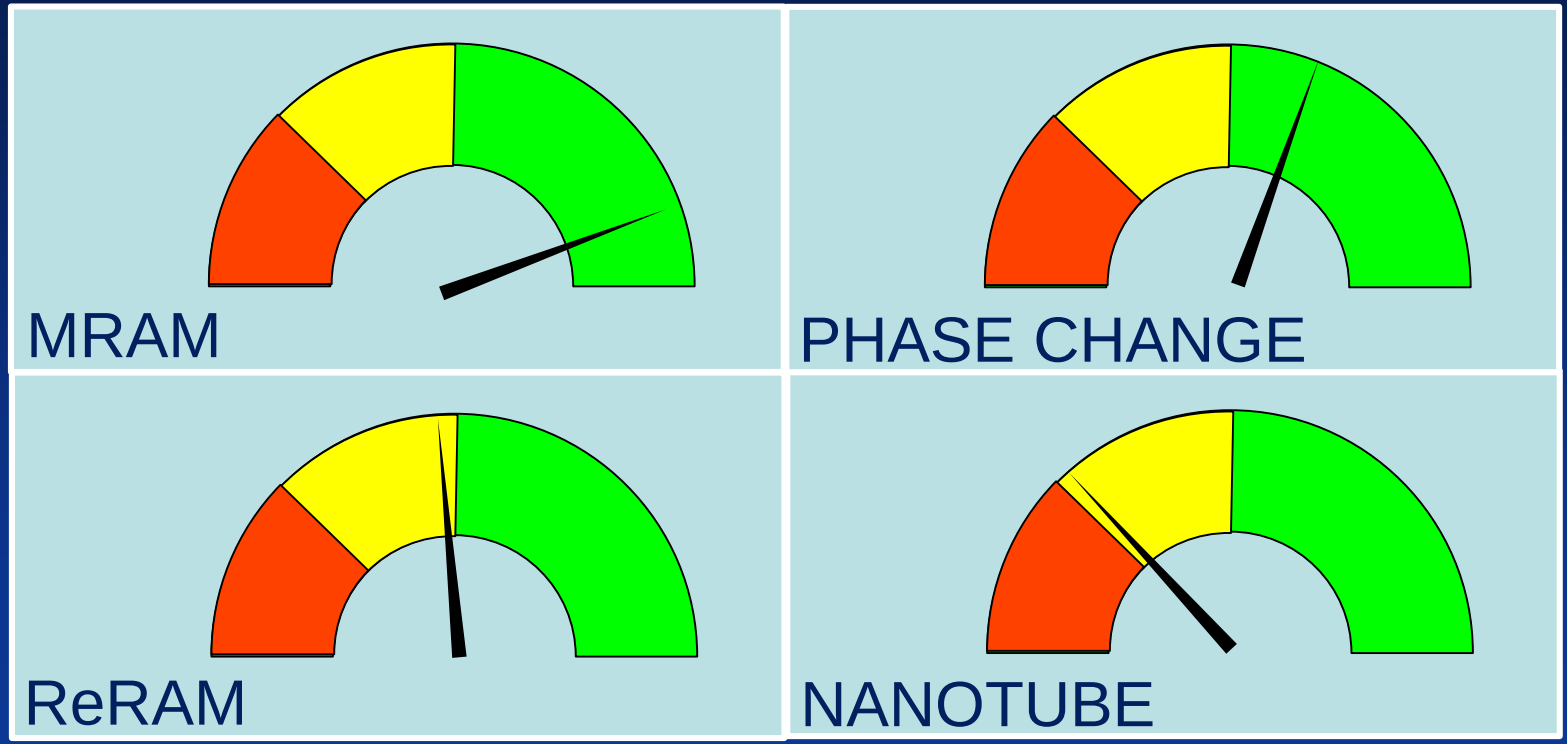
- Samsung, TSMC, Global Foundries, Intel in ramp up in 22-28nm insertions
  - As ‘embedded memory’ in SOC
- STT-MRAM introduction primarily as ‘roadmap substitution’ for embedded NOR Flash replacement
  - Plus some use as ‘pseudo’ RAM
    - Compromises on speed, endurance, retention
  - Production in early ramp
- STT-MRAM not applicable as general purpose embedded SRAM replacement

# More Big News: Production Equipment Availability

- Essential 300mm tools with suitable wafer throughput and technical capability reaching availability
  - Applied Materials, TEL, Canon/Anelva
  - Magnetic film deposition and etch are principle requirements
  - Test & Measurement also – H-probe
- Yield and other process control converging on manufacturable, but not yet equal to incumbent memory types

# Emerging Memory Technology

*Market/Production Momentum*



# Discrete MRAM in Storage

*'The Low Hanging Fruit'*

**RAID systems**
5-10+ memories per RAID system controller
$100-1000 per system
5M+ units/year

**SSD / HDD controller**
R/W cache, Logical/Physical Address Table, etc…
$1-4 per drive
$50-100 per system in high end storage system
500M+ units per year

**"Front End"** multi-Gb **buffer**
in mission critical high performance SDD
1-2 memories per drive
$10-20 per drive
150M units per year

## Critical mission: 'Protect Data in Flight'

Requires: Speed and Endurance of DRAM, with instantaneous power-off data retention

# ‘High Impact’ MRAM Application Promise
*Top 10 List*

1. >1 Million IOP SSD
2. SOC Embedded Flash Replacement
3. Unified Memory (XIP) Microcontroller
4. ‘High Training Rate/Low Training Energy’ NVM Memory for AI
5. Big-Capacitor-Free Performance SSD
6. ‘High Endurance’ Flash Gap
7. Persistent Cache for Mobile CPU
8. SOC Embedded SRAM Replacement
9. Persistent Cache for Storage System
10. Rad Hard High Density Flash Replacement

# ‘High Impact’ MRAM Application Promise

## *Top 10 List - Near Term Impact Predictions*

1. >1 Million IOP SSD
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3. Unified Memory (XIP) Microcontroller
4. ‘High Training Rate/Low Training Energy’ NVM Memory for AI
5. Big-Capacitor-Free Performance SSD
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# Editorial

*Why new chip memory is so hard…*

- Practical equipment/manufacturing barrier
  - Production fabs don't do development and cost $5-10 billion
  - Full development today requires >$200 million
    - New physical structures 'manufacturability' isn't known till late in development cycle
- Multi-dimensional 'chicken & egg' situation

- Takeaway: It's HUGE that leading CMOS foundries have installed production equipment, invested in processes, have announced support, and are on the threshold of MRAM production

# (More) Editorial

*Why new chip memory is so hard…*

- Matching new technology manufacturing yield/performance curve to design expectations
  - Combining well-known CMOS yield characteristics with ambiguous and optimistic ‘new device’ yield statistics is hard
    - Cross-functional engineering teams universally underestimate

- Takeaway: Teams that focus on bridging both the ‘yield curve gap’ with margin and the ‘cross-functional interdependency gap’ will win in this emerging market

# XIP User Group Formation

- Key future application of MRAM
  - Example:  Flash and SRAM collapsed into single memory in microcontroller

- Benefit modeling is complex…cost, power/energy, performance/latency
- Memory partitioning an open question
  - Fixed code updates, scratch RAM, variable storage, protected address space, etc
- Memory cycle/speed provisions:  wait states, error recovery, cache support, etc
- Design tool requirements?...debugger, compiler/assembler, etc

- User group in formation….contact me if interest…


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