Temperature challenges of 3D NAND devices referring automotive standards and use cases

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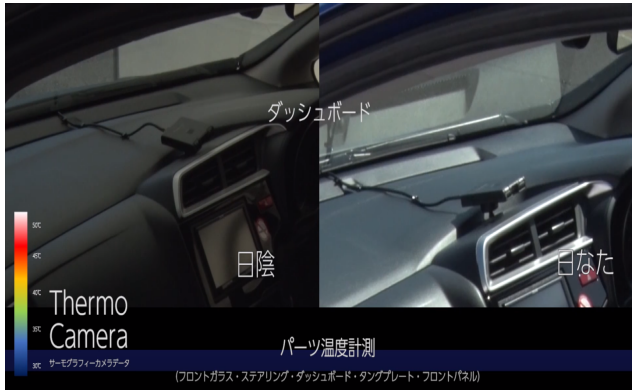
Outline

- **Automotive Applications & Temperature Challenges**
  - Temperature Differentiation
  - Temperature Scenarios V.S. Applications
  - Temperature Related Standards
- **3D NAND IC Level: Cross Temperature Tests and the Findings**
- **How To Enhance Drive Reliabilities Due to Temperature Impact**
- **Test Result of Self-Recovery Calibration**
- **Take Away**

Disclaimer: Results in this presentation are not specific to a particular NAND Flash or a Flash memory vendor

Temperature Differentiation:
Car under shield vs. expose

Above Dashboard



Under shield

Under expose

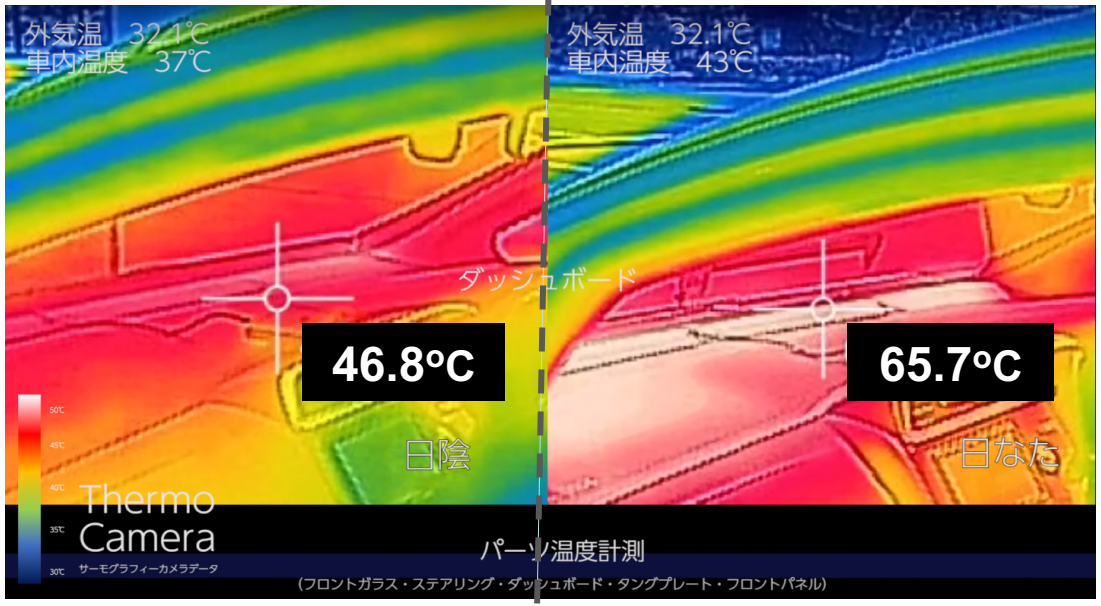


Photo source: jafchannel

Flash Memory Summit

Temperature Differentiation:
Car under shield vs. expose

Around Steering Wheel

Under Shield

Under Expose

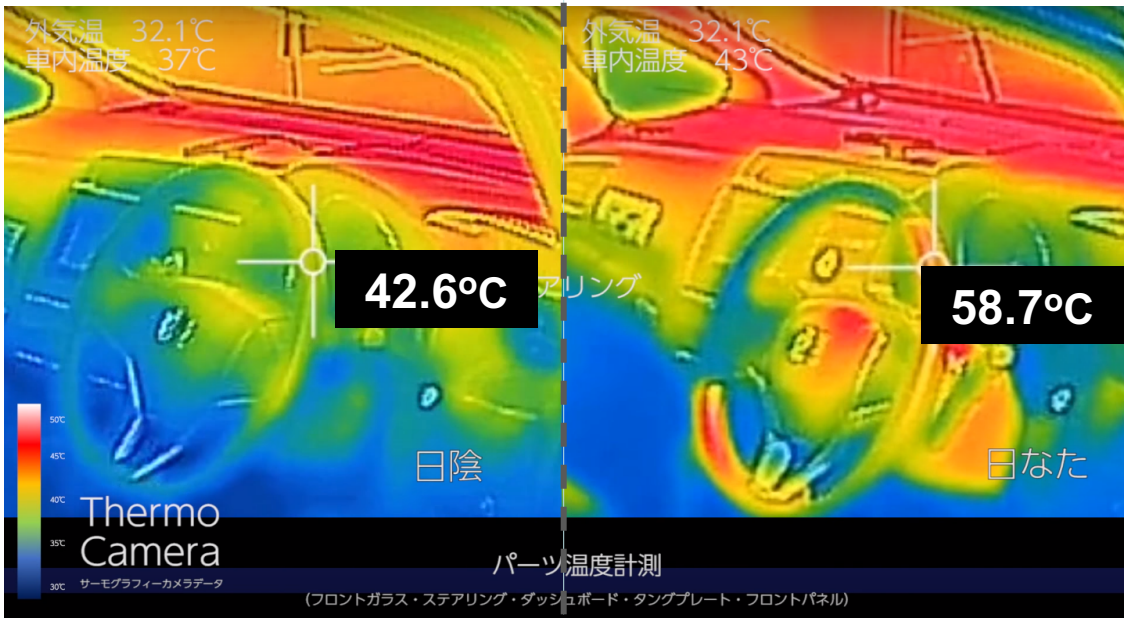
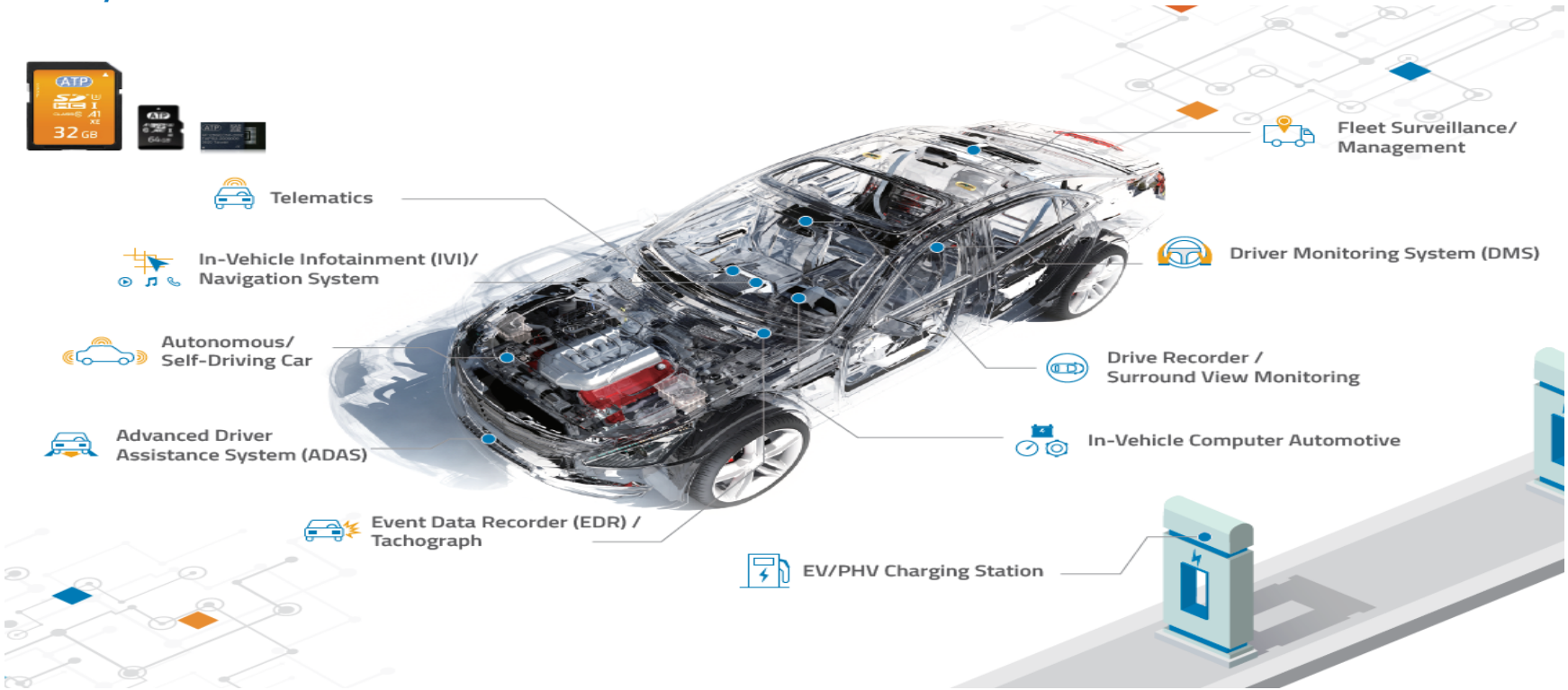


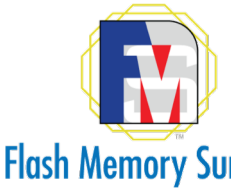
Photo source: jafchannel

Automotive Applications



Temperature Scenarios V.S. Applications

- Program & Read @ Same Temperature?
  e.g. IVI, Telematics, Gateway, In-vehicle computer, ADAS, DMS, Fleet management
- Program @ Low Temperature and Read @ High/Room Temperature?
  e.g. Drive Recorder, Data logger, EV charging station
- Program @ High Temperature and Read @ Low/Room Temperature?
  e.g. Drive Recorder, Data logger, EV charging station
- Program @ Room Temperature and Read @ High Temperature?
  e.g. Map Navigation, OS/Application program
- Program @ Room Temperature and Read @ Low Temperature?
  e.g. Map Navigation, OS/Application program

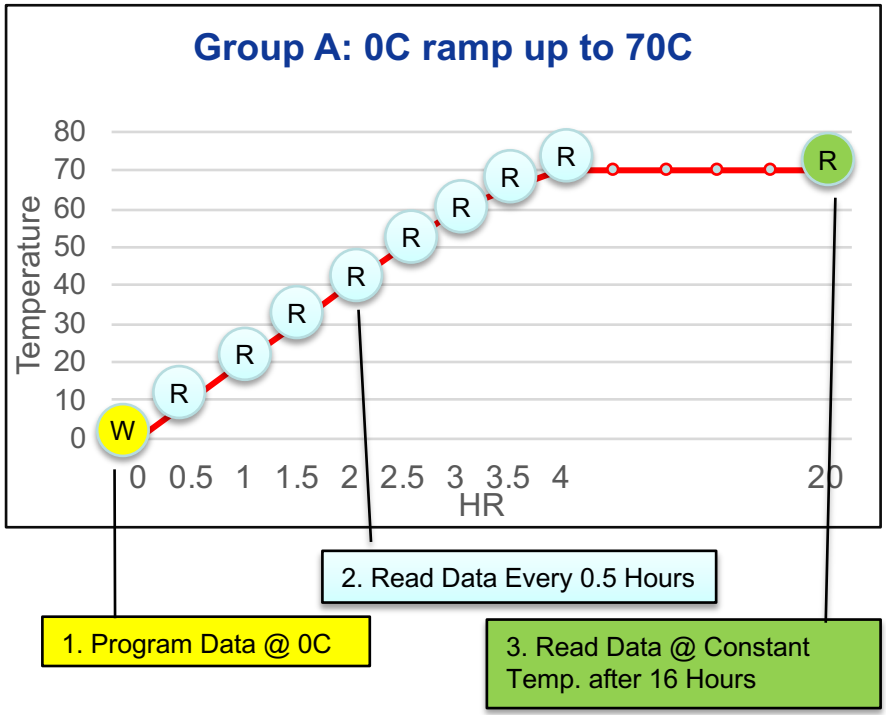


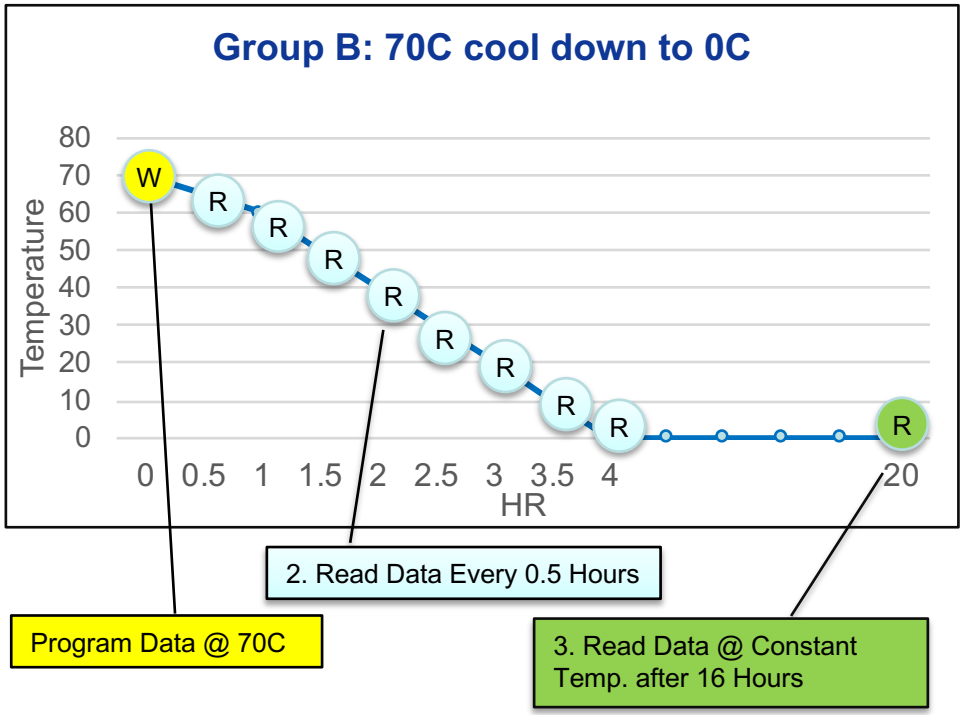
Temperature Related Standards- AEC-Q100 / AEC-Q104

	STRESS	TEST METHOD
AEC-Q100 / AEC-Q104	**Temperature Humidity-Bias or Biased HAST**	JEDEC JESD22-A101 or A110
	Autoclave or Unbiased HAST or Temperature-Humidity (without Bias)	JEDEC JESD22-A102, A118, or A101
	Temperature Cycling	JEDEC JESD22-A104
	Power Temperature Cycling	JEDEC JESD22-A105
	High Temperature Storage Life	JEDEC JESD22-A103
	High Temperature Operating Life	JEDEC JESD22-A108
	Negative Bias Temperature Instability	JEDEC JEP001
	Low Temperature Storage Life	JEDEC JESD22-A119
	Start Up and Temperature Steps	**ISO 16750-4**

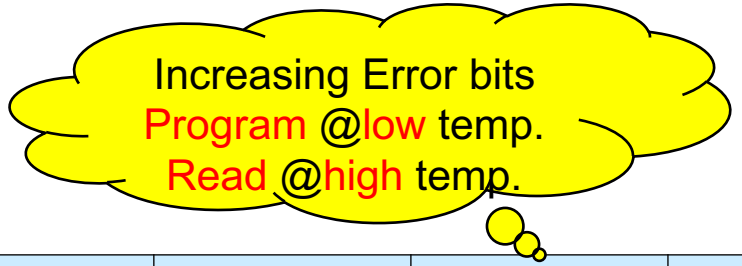
3D NAND IC: Cross Temperature Test (1)

Pre-cycle: 100 P/E cycles





Test Result (1)



Program @ 0C	Read @ 0℃	Read @20℃ (1 hour)	Read @ 40℃ (2 hours)	Read @ 60℃ (3 hours)	Read @ 70℃ (4 hours)	Keep constant 70℃ for 16hrs
UECC (ECC threshold 72bits/1KB)	N/A	N/A	747	2259	5320	10869

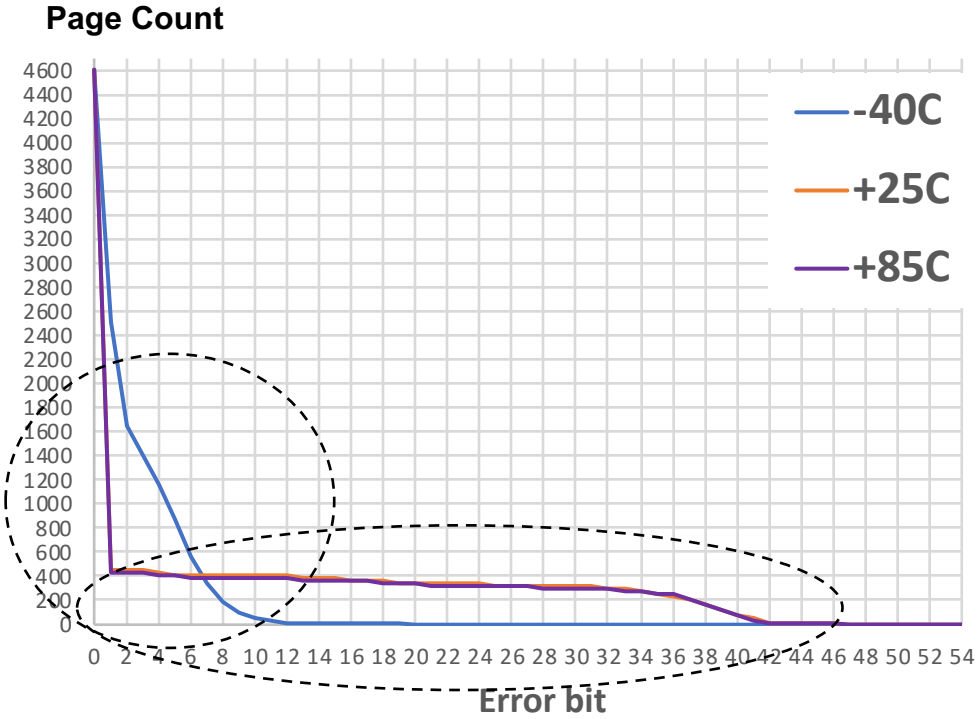
Program @ 70C	Read @70℃	Read @ 60℃ (1 hour)	Read @ 40℃ (2 hours)	Read @ 20℃ (3 hours)	Read @ 0℃ (4 hours)	Keep constant 0℃ for 16hrs
UECC (ECC threshold 72bits/1KB)	N/A	N/A	N/A	N/A	N/A	1

3D NAND: Cross Temperature Test (2)

Pre-cycle: 300

- Pre-cycle: 300
- **Program @-40C**
- Read @25C / 85C
  - @-40C, page count error bits < 20
  - @+25C, page count error bits < 47
  - @+85C, page count error bits < 47

⇒ **Error bits increasing after a certain cross temp. range (over 65C)**

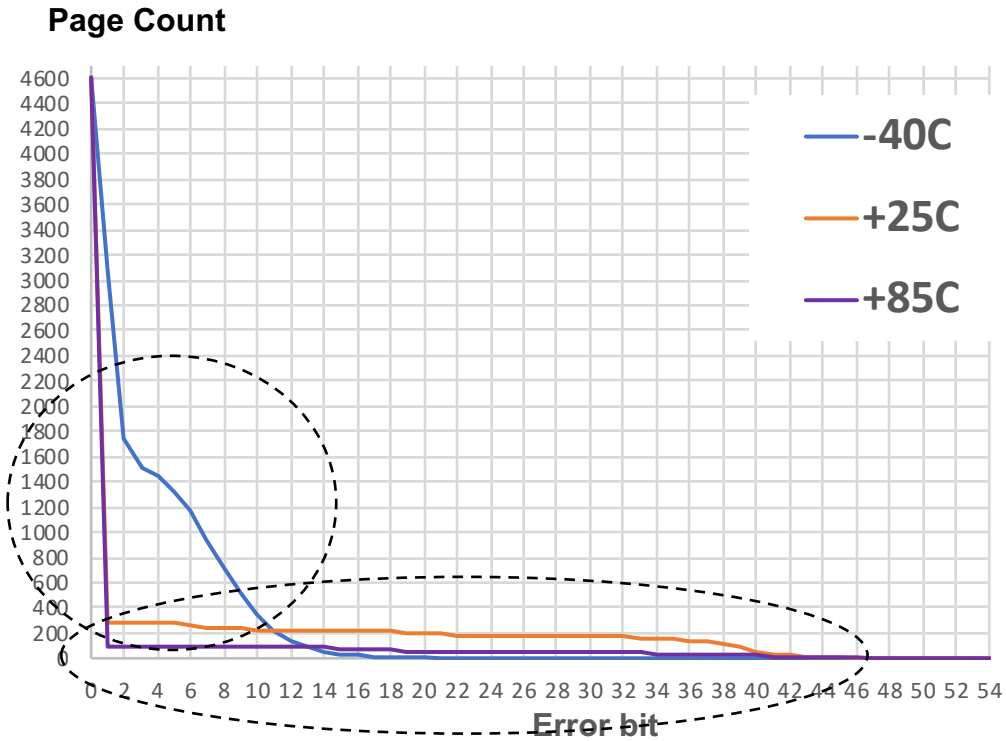


3D NAND IC: Cross Temperature Test (3)

Pre-cycle: 3000

- Pre-cycle: 3000
- **Program @-40C**
- Read @25C / 85C
  - @-40C, page count error bits < 21
  - @+25C, page count error bits < 46
  - @+85C, page count error bits < 47

⇒ **Error bits increasing after a certain cross temp. range (over 65C)**

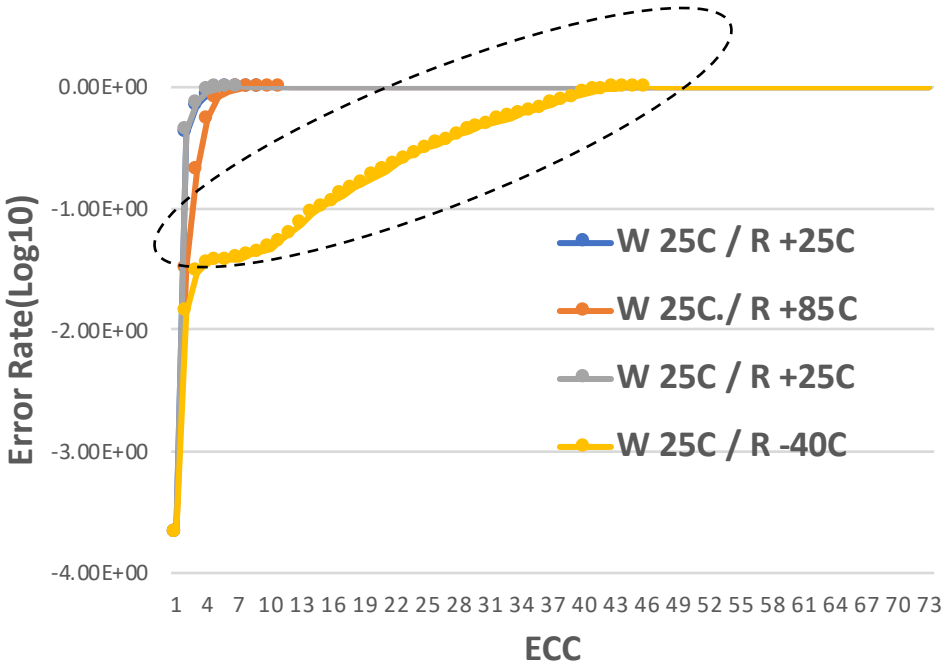


3D NAND: Cross Temperature Test (4)

Pre-cycle: 300 P/E cycles

- Pre-cycle: 300 P/E cycles
- **Program @ 25C,**
- Read @ 25C/+85C
  - @+25C, error bits < 9
  - @+85C, error bits < 11
- Read @ 25C/-40C
  - @+25C, error bits < 7
  - @-40C, error bits < 46

⇒ **Program @ 25C, Read @ -40C**
Error bits increasing a lot



How to Enhance Drive Reliabilities due to Temperature Impact

- Change Temperature Related Variables
  - High temp.: Improve heat dissipation, Fans, reduce transfer speed…
  - Low temp.: Multiple dies heating up, increase transfer speed…
- Self Recovery
  - Read voltage shifting adjustment by specific vendor CMD
  - Using Temperature Sensor to detect Temperature as trigger point under different conditions
  - Dynamic Self-Recovery Calibration is applied to adapt various temperature mode

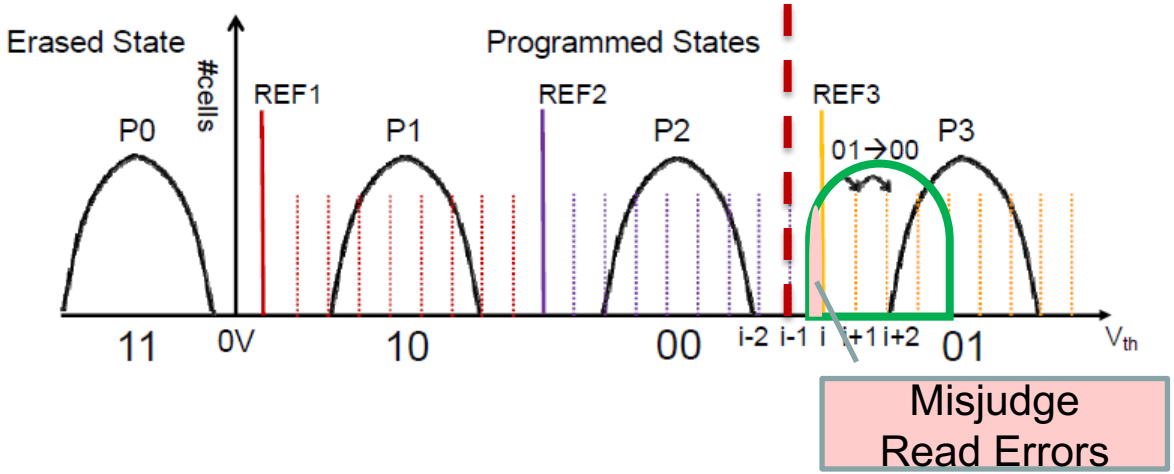
Note: Need Experiments to find suitable parameters. Be aware of timing & performance impact

Note 1 Source: 2017FMS IBM Research – Zurich Research Laboratory

Read Voltage Shifting

- Placement can shift beyond the reference voltage (REF3), causing read errors (misjudge 01 to 00)
- Read calibration can shift the reference voltage until a passing read point is found. (i=original reference voltage, after read retry shifting voltage to i-1, the error is recovered)

■ **3D NAND requires more Calibration levels than planar NAND**



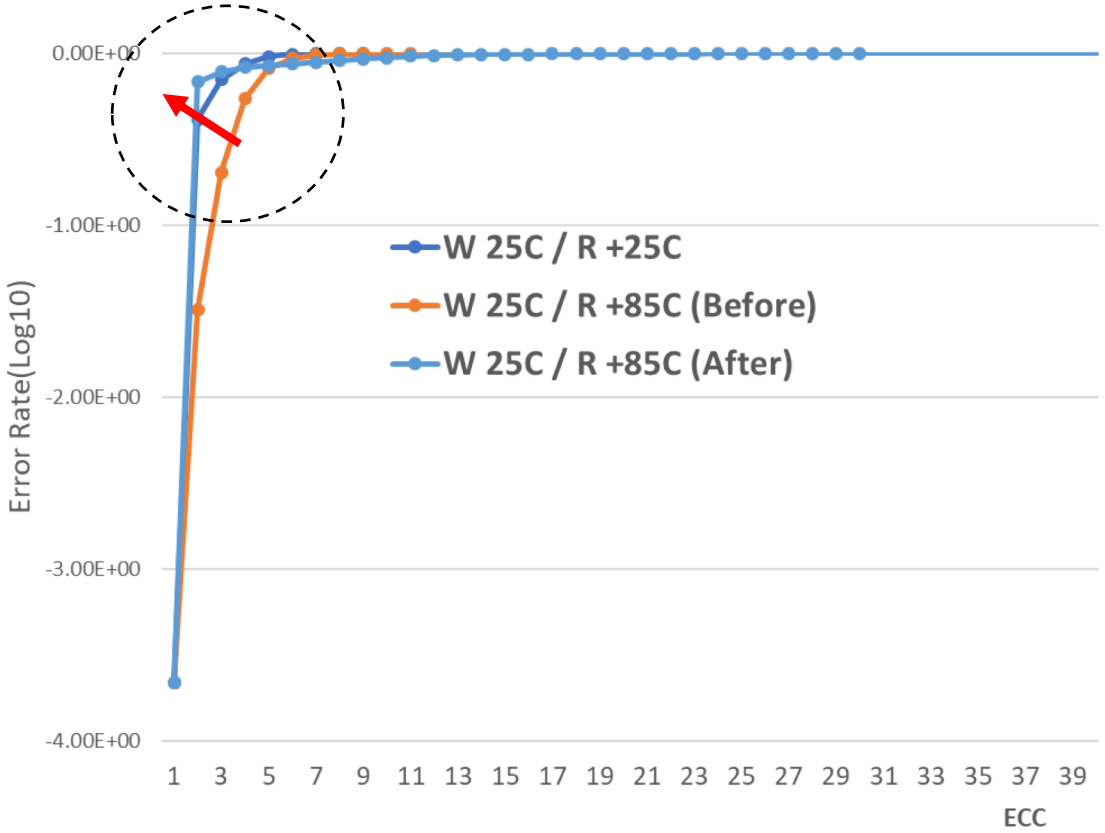
Read errors can be recovered (distribution not overlapping)
New Reference voltage is applied using temperature sensor as trigger indicator

Before & After (Read @+85C) Dynamic Self-Recovery Calibration

- Pre-cycle: 300 P/E cycles
- **Program @ 25C**,
- Read @ 25C/+85C

⇒ **Error bit Reduced,**

⇒ **Close to +25C read test result**

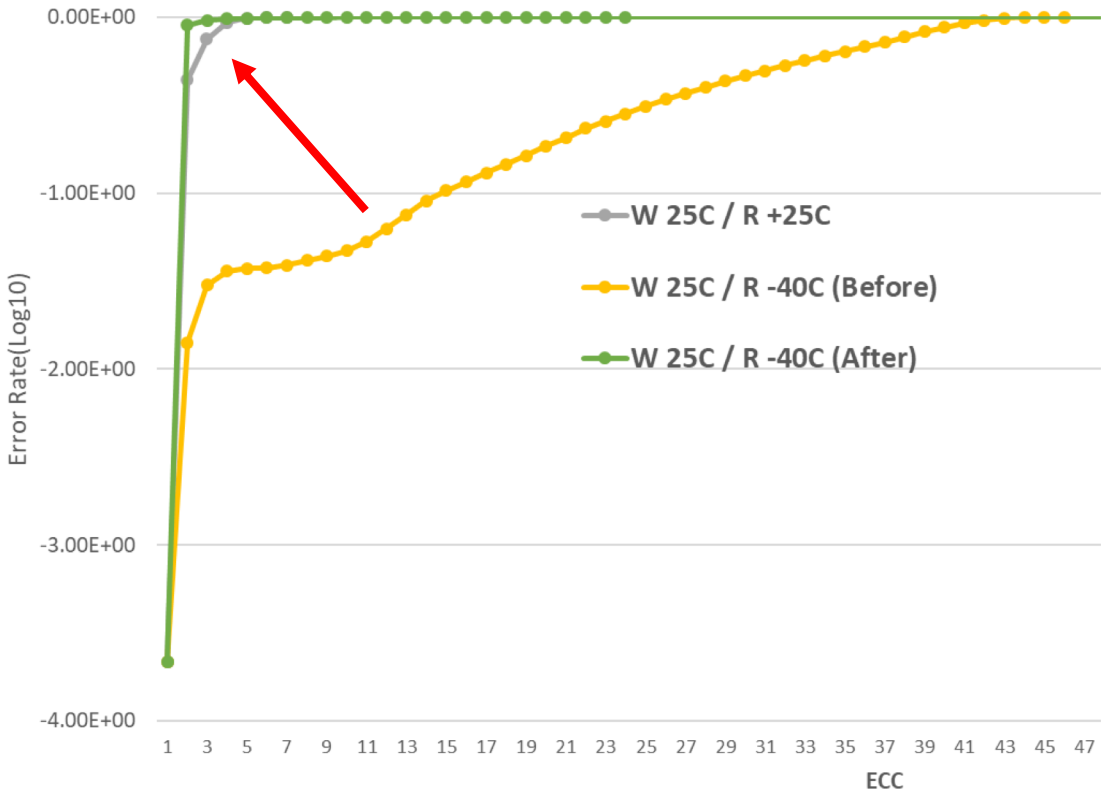


Before & After (Write @+85C) Dynamic Self-Recovery Calibration

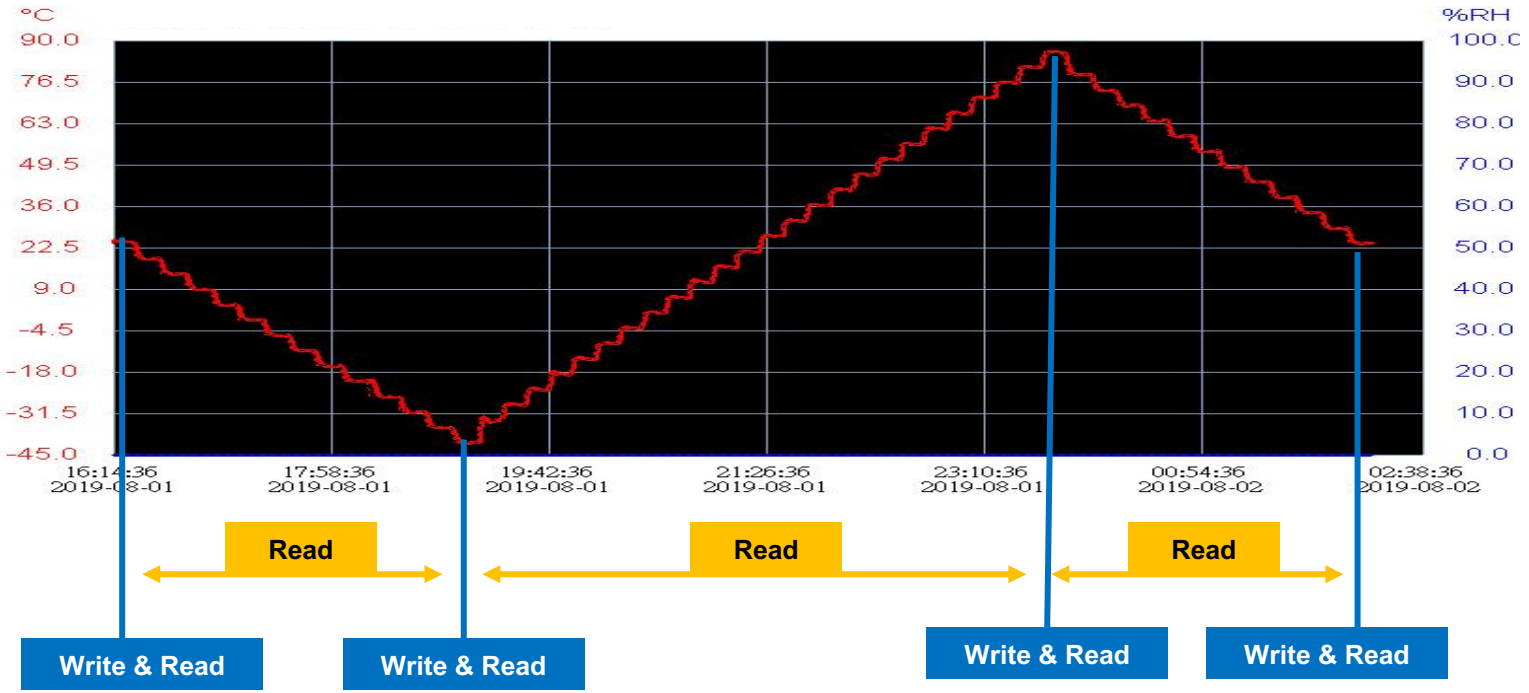
- Pre-cycle: 300
- **Program @ 25C**,
- Read @ 25C/+85C

⇒ **Error bit Reduced,**

⇒ **Close to +25C read test result**



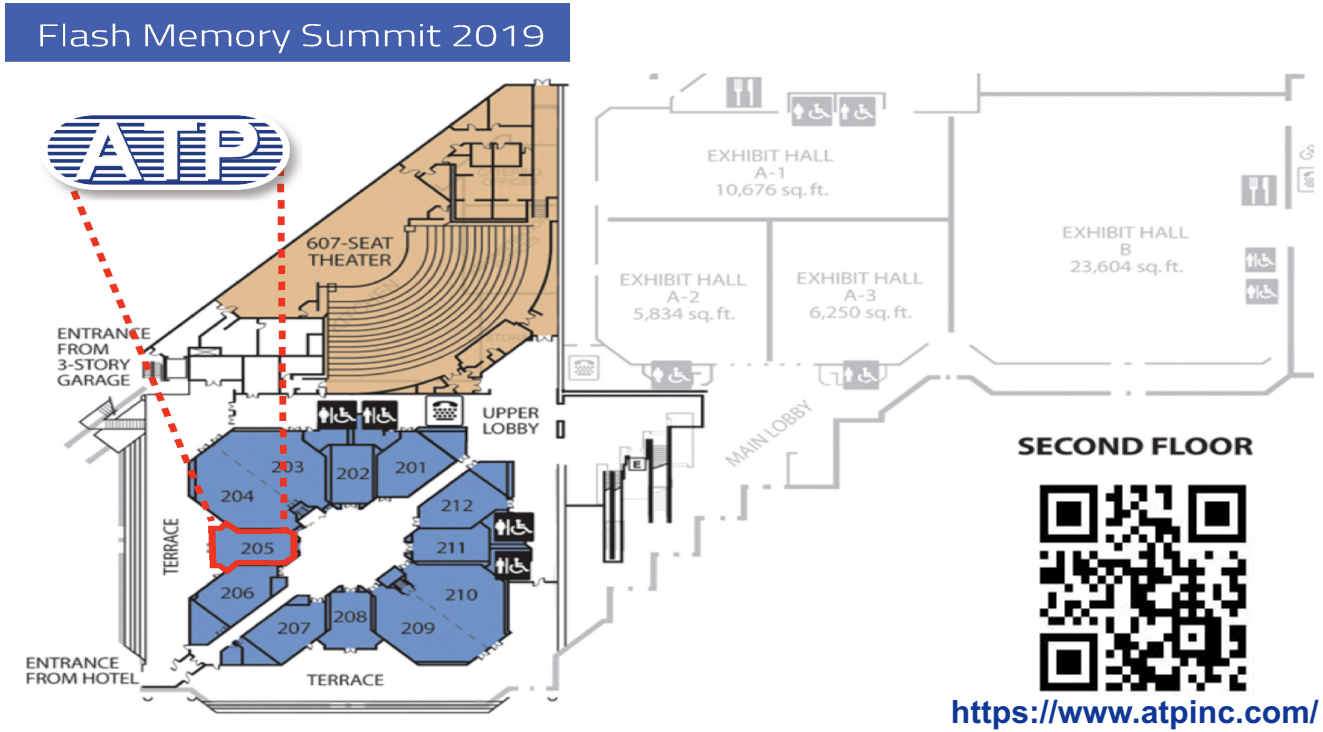
Device Level – Temperature Step Test (Mixed Workload Test Passed)



Take Away

- The traditional temperature test standards may not be enough to cover all temperature scenarios.
- Cross Temp.: Program Data & Read Data at “Different” temp. could generate more errors than at “Same” temp.
- In general, low temp. program + high temp. read is worse than high temp. program + low temp. read
- Program @ RT and read @ low temp. is worse than read @ high temp.
- **Dynamic Self-recovery FW calibration is proven to be effective to reduce error bit level @ cross temp. scenarios (recover errors so the result is similar as Program/Read @ same temperature)**

Visit ATP @ room 205 & Website



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