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FLIN:

Enabling Fairness and Enhancing Performance in Modern NVMe Solid State Drives

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Flash Memory Summit

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Executive Summary

- Modern solid-state drives (SSDs) use new storage protocols (e.g., NVMe) that **eliminate the OS software stack**
  - I/O requests are now scheduled inside the SSD
  - Enables **high throughput:** millions of IOPS

- OS software stack elimination **removes existing fairness mechanisms**
  - We **experimentally characterize fairness** on four real state-of-the-art SSDs
  - **Highly unfair slowdowns:** large difference across concurrently-running applications

- We find and analyze **four sources of inter-application interference** that lead to slowdowns in state-of-the-art SSDs

- **FLIN:** a new I/O request scheduler for modern SSDs designed to **provide both fairness and high performance**
  - Mitigates all four sources of inter-application interference
  - Implemented fully in the SSD controller firmware, uses < 0.06% of DRAM space
  - FLIN improves **fairness by 70%** and **performance** by **47%** compared to a state-of-the-art I/O scheduler

Outline

Background: Modern SSD Design

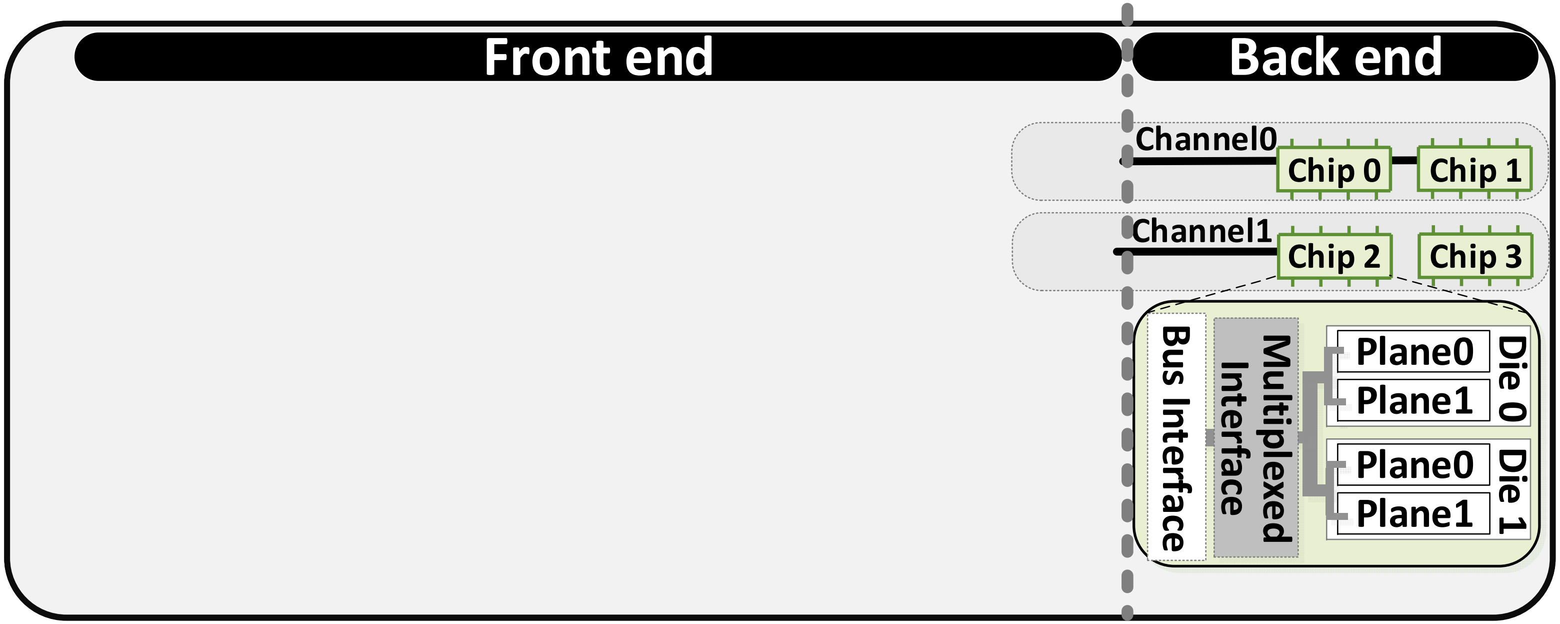
Unfairness Across Multiple Applications in Modern SSDs

FLIN:
Flash-Level INterference-aware SSD Scheduler

Experimental Evaluation

Conclusion

Internal Components of a Modern SSD



- **Back End:** data storage
  - Memory chips (e.g., NAND flash memory, PCM, MRAM, 3D XPoint)

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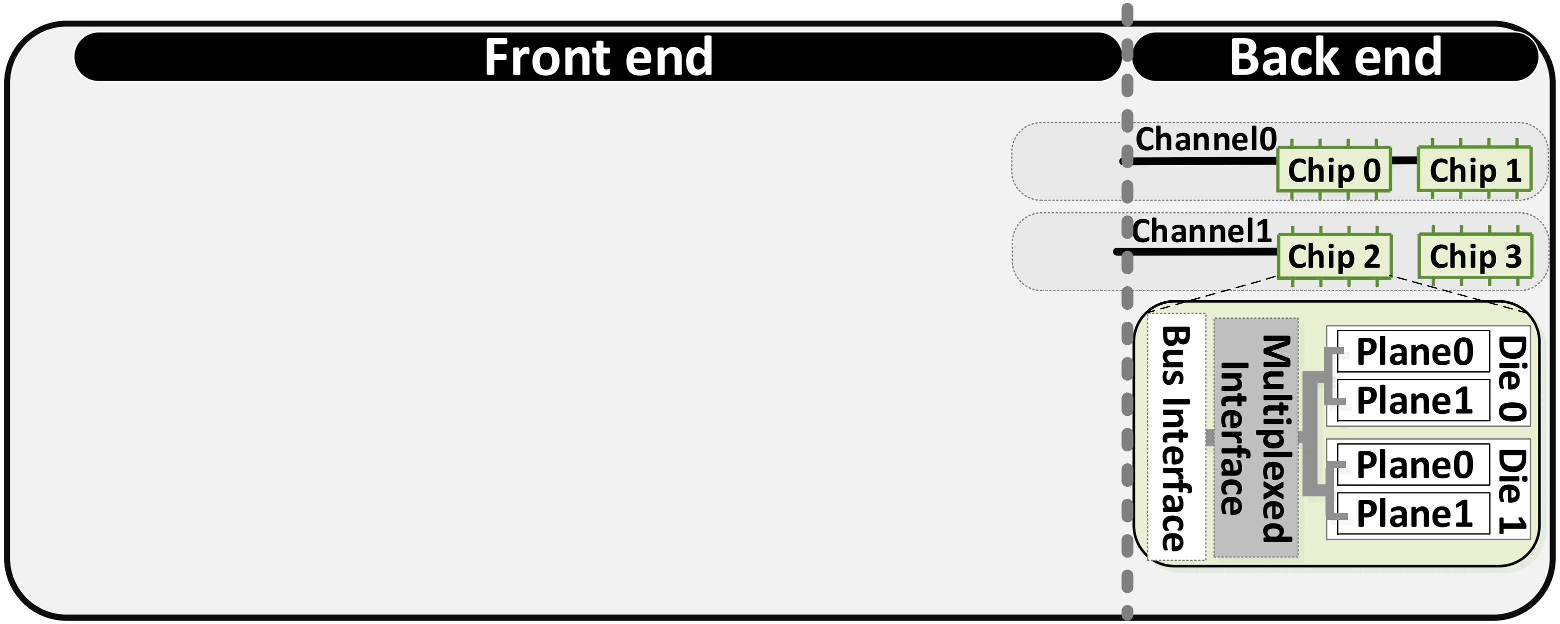

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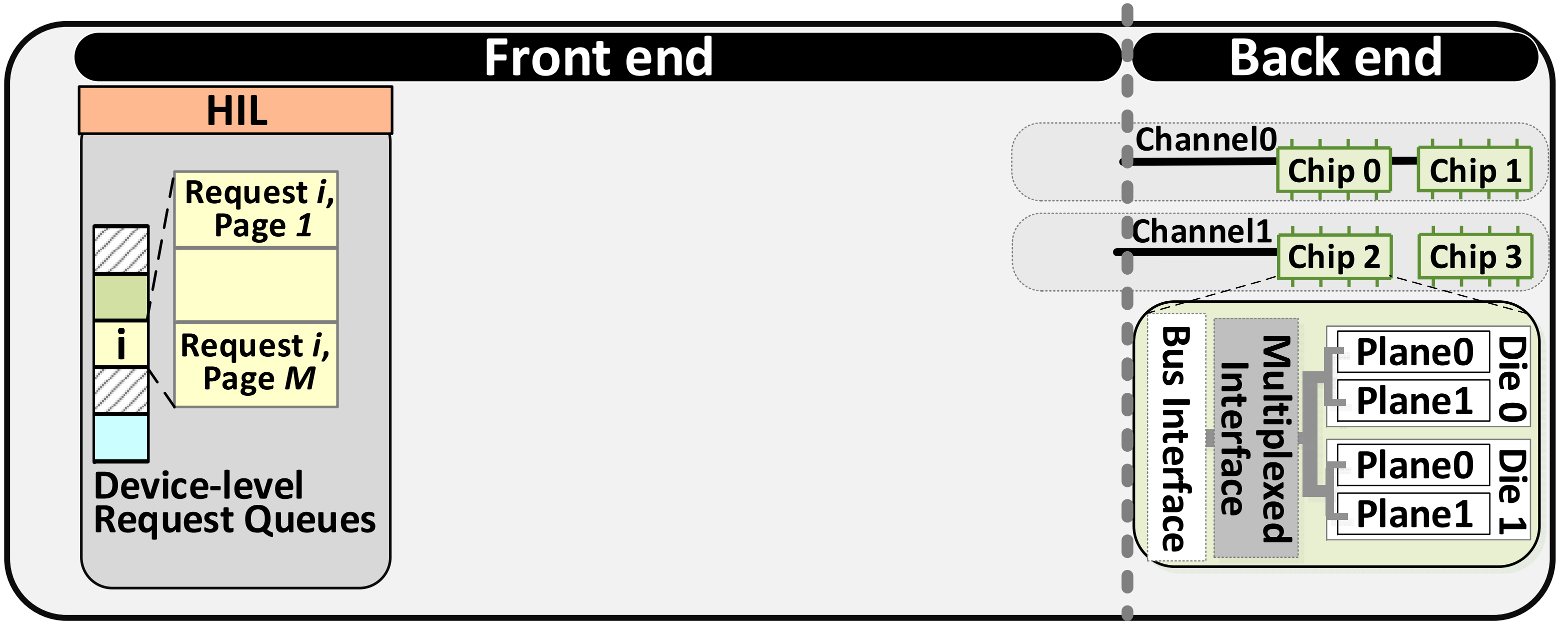

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  - **Host–Interface Logic (HIL):** protocol used to communicate with host

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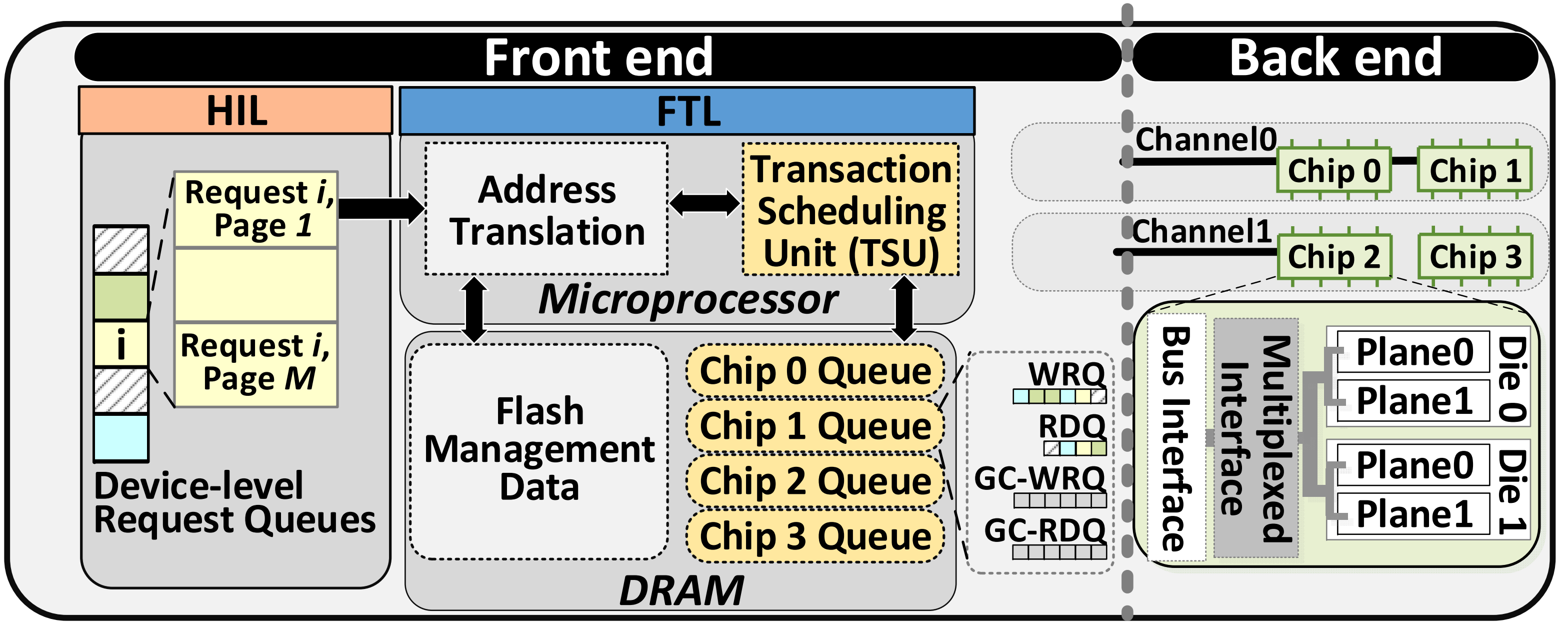

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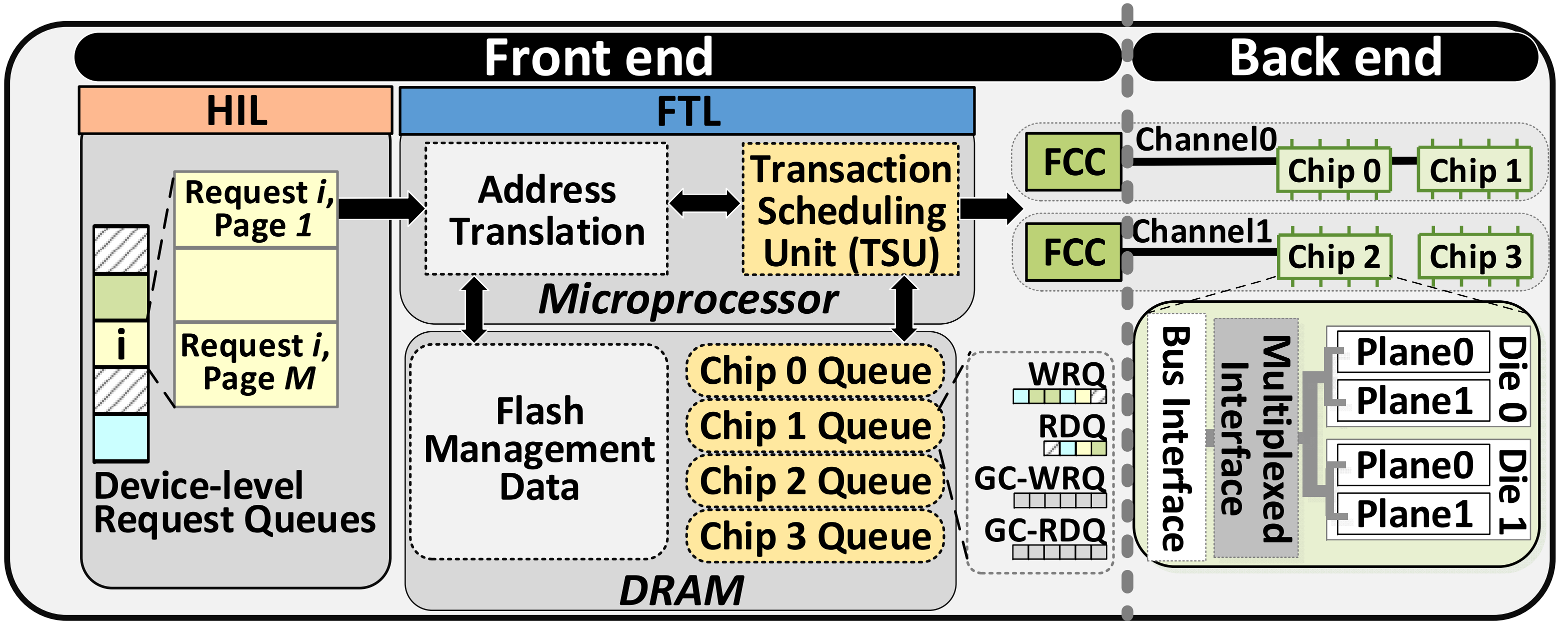

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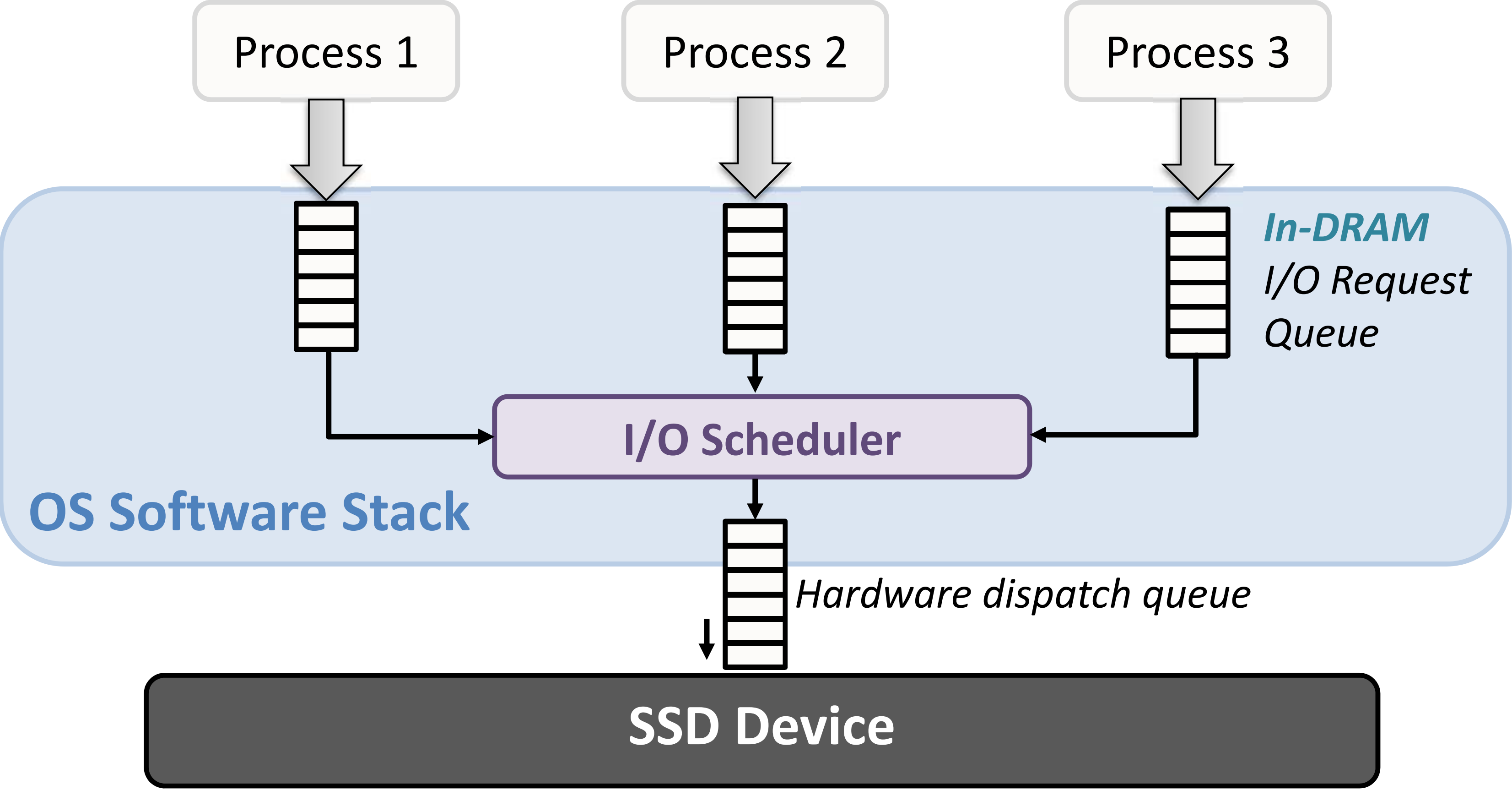
  - Flash Translation Layer (FTL): manages resources, processes I/O requests
  - Flash Channel Controllers (FCCs): sends commands to, transfers data with memory chips in back end

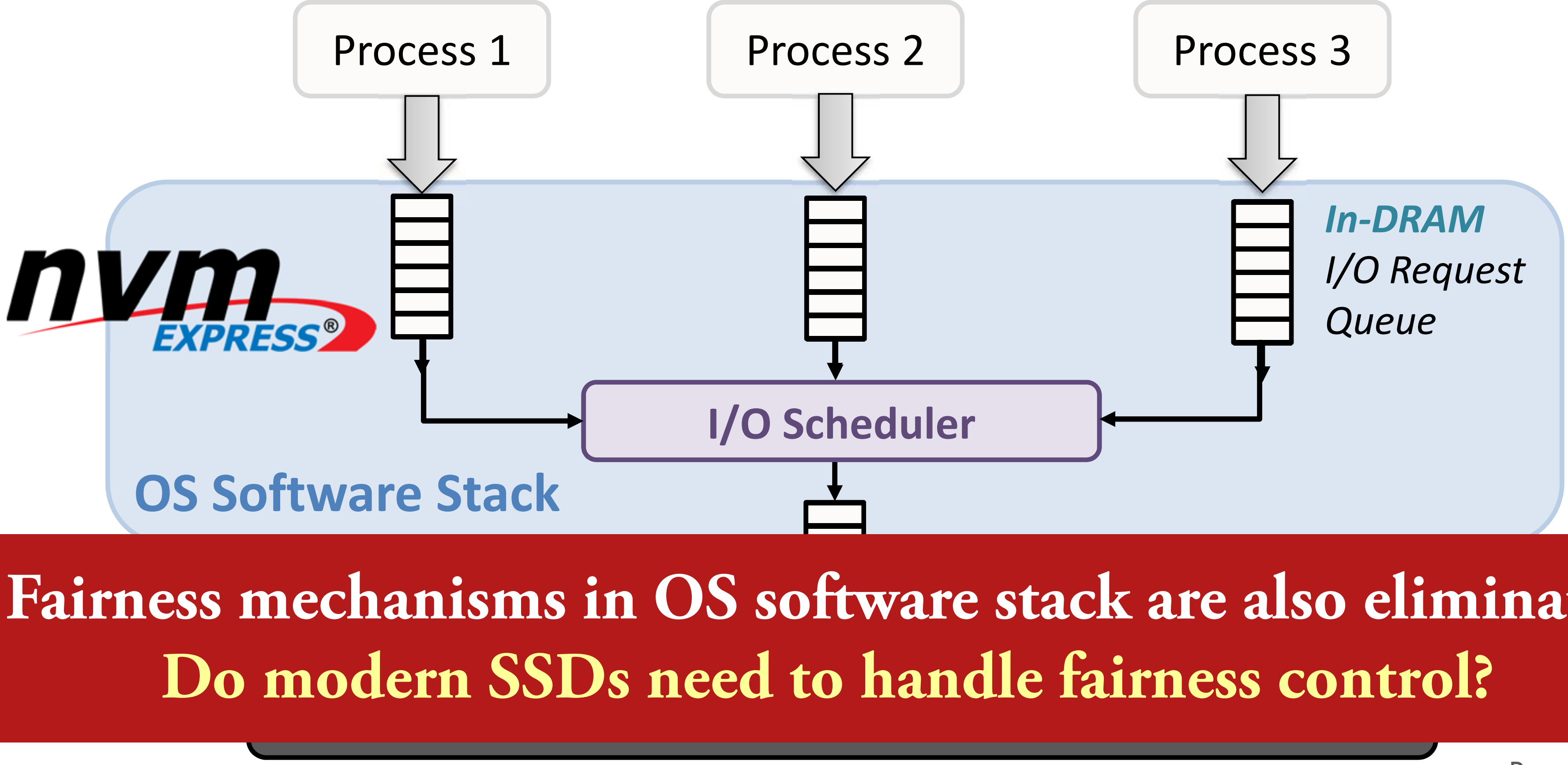
Conventional Host–Interface Protocols for SSDs

- SSDs initially adopted conventional host–interface protocols (e.g., SATA)
  - Designed for magnetic hard disk drives
  - Maximum of only *thousands* of IOPS per device



Host–Interface Protocols in Modern SSDs

- Modern SSDs use high-performance host–interface protocols (e.g., NVMe)
  - Bypass OS intervention: SSD must perform scheduling
  - Take advantage of SSD throughput: enables *millions* of IOPS per device



Fairness mechanisms in OS software stack are also eliminated

Do modern SSDs need to handle fairness control?

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Measuring Unfairness in Real, Modern SSDs

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- We measure fairness using four real state-of-the-art SSDs
  - NVMe protocol
  - Designed for datacenters

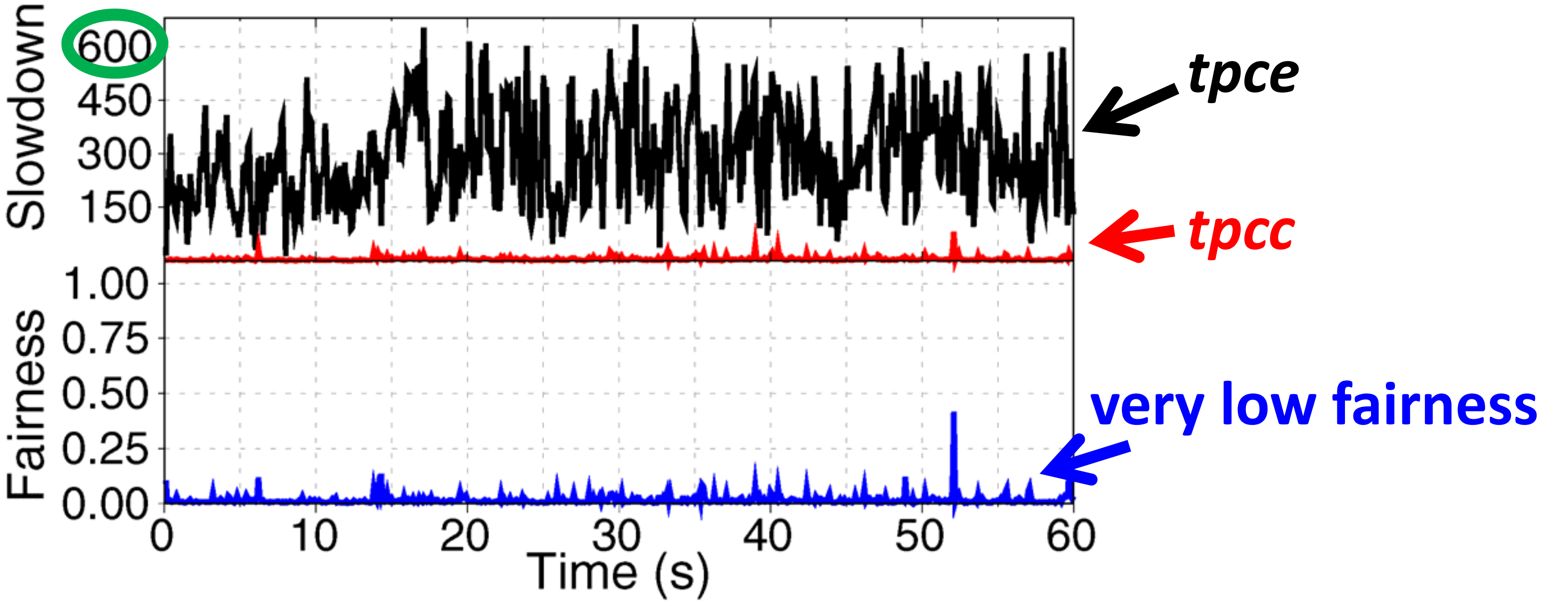
- Flow: a series of I/O requests generated by an application

- Slowdown = $\frac{\text{shared flow response time}}{\text{alone flow response time}}$ *(lower is better)*

- Unfairness = $\frac{\text{max slowdown}}{\text{min slowdown}}$ *(lower is better)*

- Fairness = $\frac{1}{\text{unfairness}}$ *(higher is better)*

Representative Example: *tpcc* and *tpce*



average slowdown of *tpce*:
2x to 106x across our four real SSDs

SSDs do not provide fairness among concurrently-running flows

What Causes This Unfairness?

- Interference among concurrently-running flows
- We perform a detailed study of interference
  - MQSim: detailed, open-source modern SSD simulator [FAST 2018]
    https://github.com/CMU-SAFARI/MQSim
  - Run flows that are designed to demonstrate each source of interference
  - Detailed experimental characterization results in the paper

- We uncover four sources of interference among flows

Source 1: Different I/O Intensities

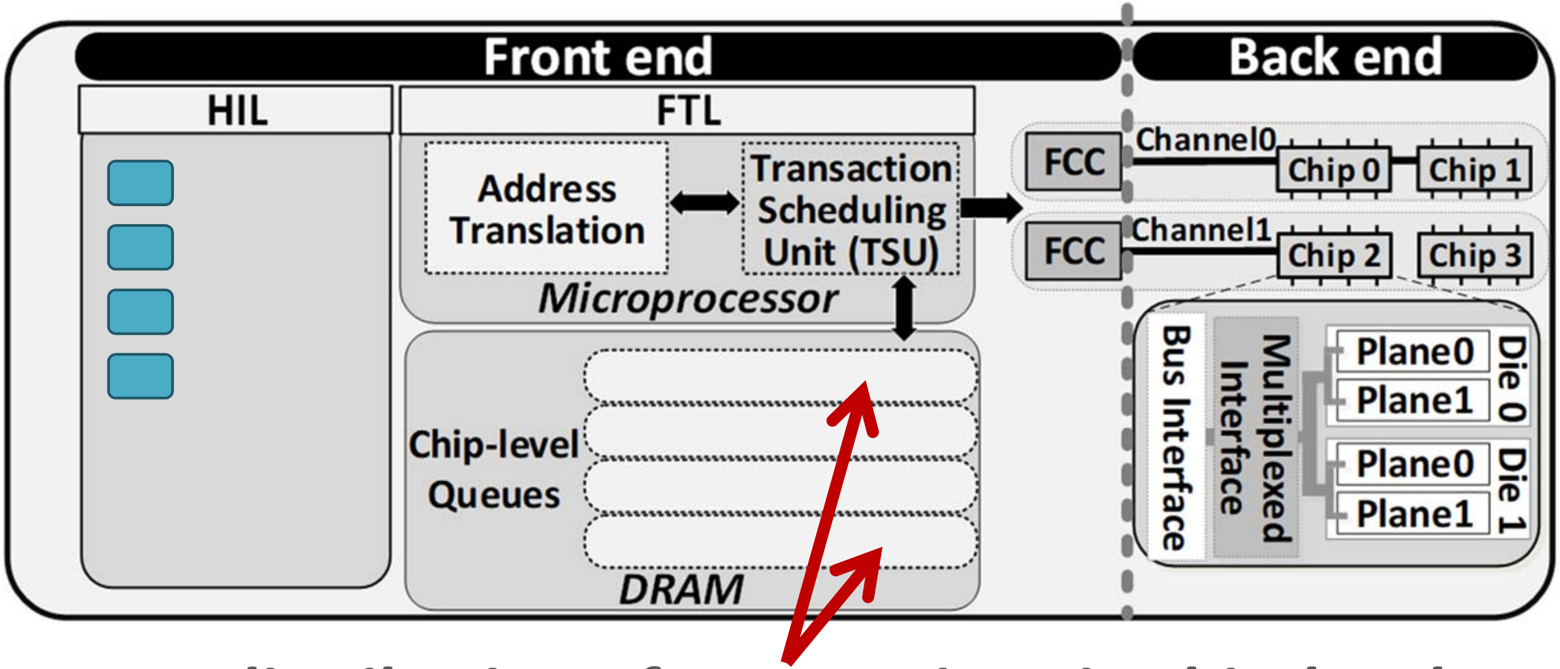
- The I/O intensity of a flow affects the average queue wait time of flash transactions

The average response time of a low-intensity flow substantially increases due to interference from a high-intensity flow

- Similar to memory scheduling for bandwidth-sensitive threads vs. latency-sensitive threads

Source 2: Different Access Patterns

- Some flows take advantage of **chip-level parallelism** in back end

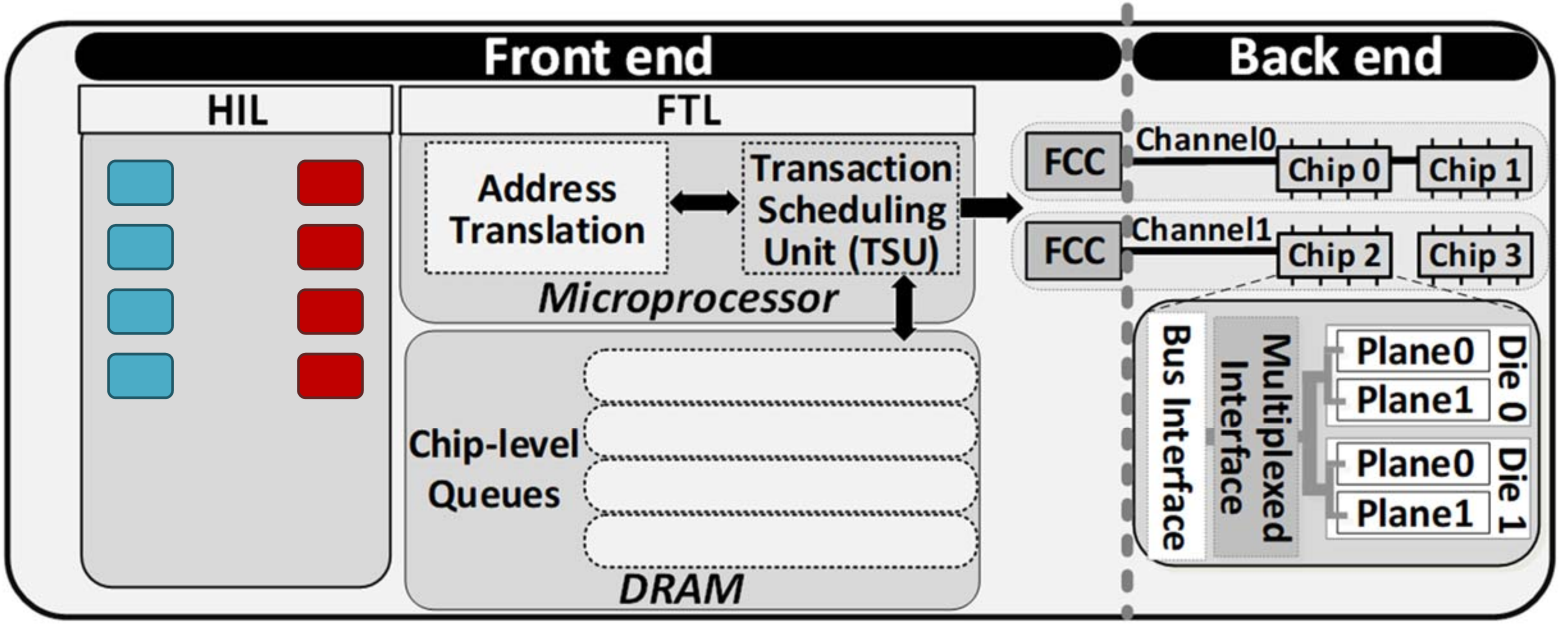


***Even* distribution of transactions in chip-level queues**

- Leads to a **low queue wait time**

Source 2: Different Request Access Patterns

- Other flows have access patterns that **do not exploit parallelism**



Flows with parallelism-friendly access patterns are susceptible to interference from flows whose access patterns do not exploit parallelism

Source 3: Different Read/Write Ratios

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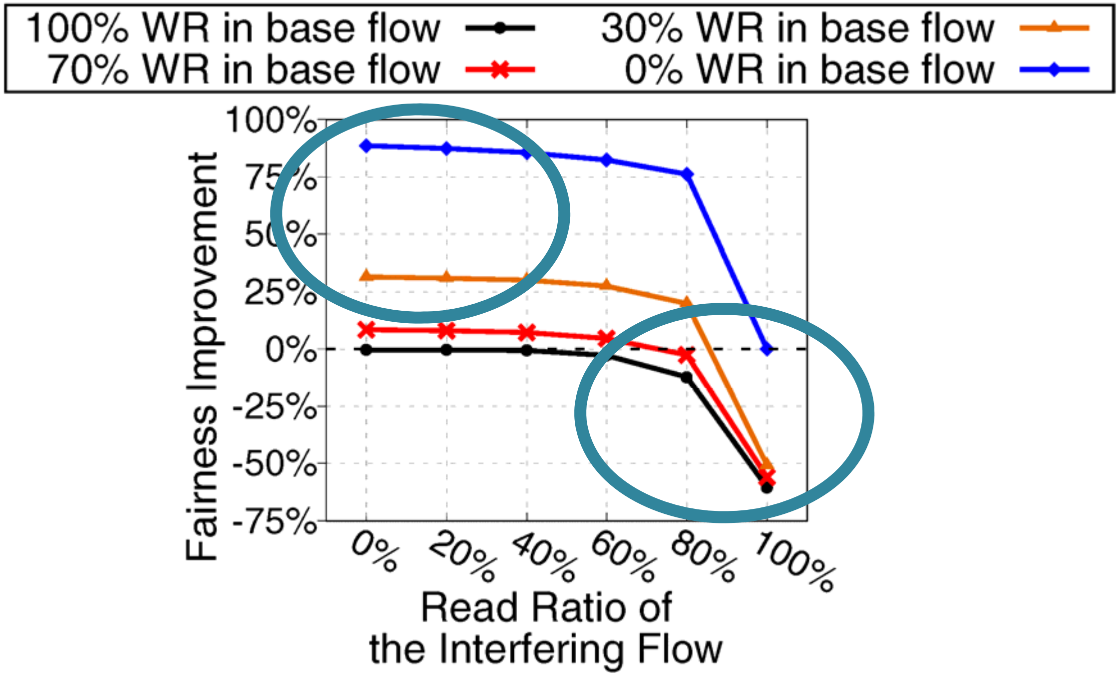
- State-of-the-art SSD I/O schedulers **prioritize reads over writes**
- Effect of read prioritization on fairness (vs. first-come, first-serve)



When flows have different read/write ratios, existing schedulers do not effectively provide fairness

Source 4: Different Garbage Collection Demands

- NAND flash memory performs writes out of place
  - Erases can only happen on an entire flash block (hundreds of flash pages)
  - Pages marked invalid during write

- Garbage collection (GC)
  - Selects a block with mostly-invalid pages
  - Moves any remaining valid pages
  - Erases blocks with mostly-invalid pages

- High-GC flow: flows with a higher write intensity induce more garbage collection activities

The GC activities of a high-GC flow can unfairly block flash transactions of a low-GC flow

Summary: Source of Unfairness in SSDs

- Four major sources of unfairness in modern SSDs
  1. I/O intensity
  2. Request access patterns
  3. Read/write ratio
  4. Garbage collection demands

OUR GOAL

Design an I/O request scheduler for SSDs that
(1) provides fairness among flows
by mitigating all four sources of interference, and
(2) maximizes performance and throughput

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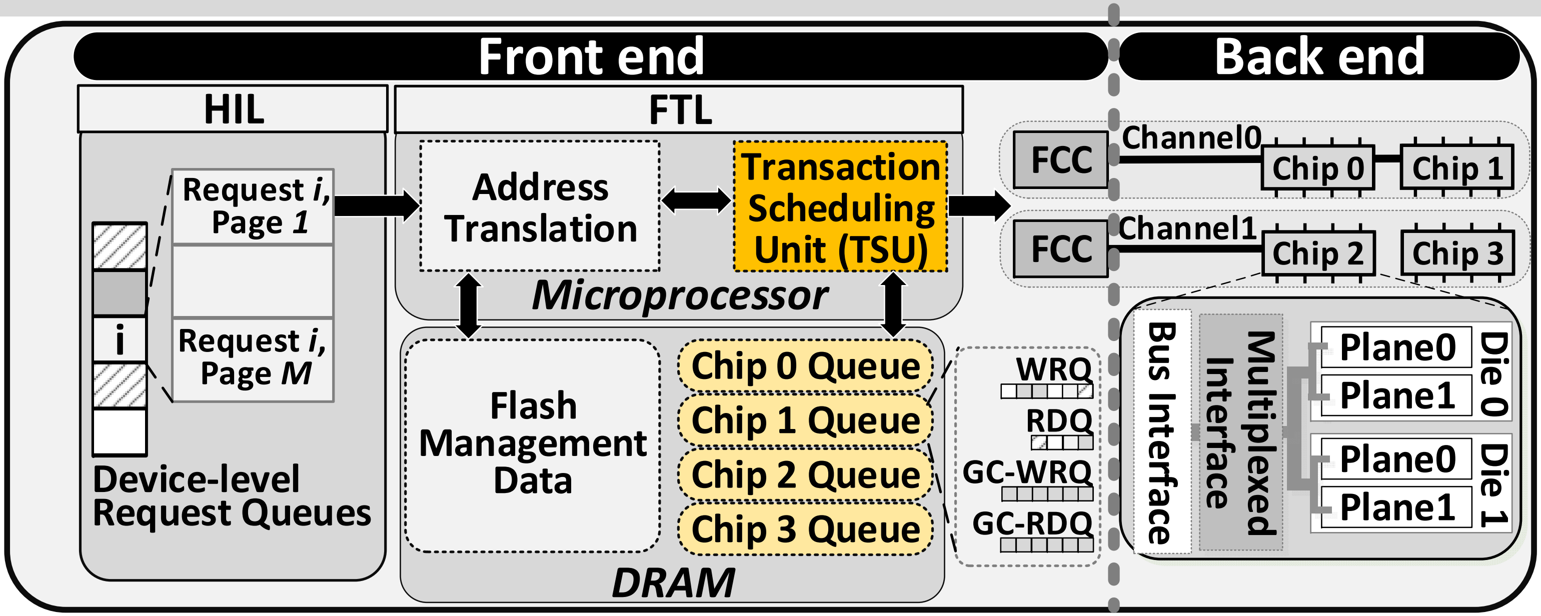
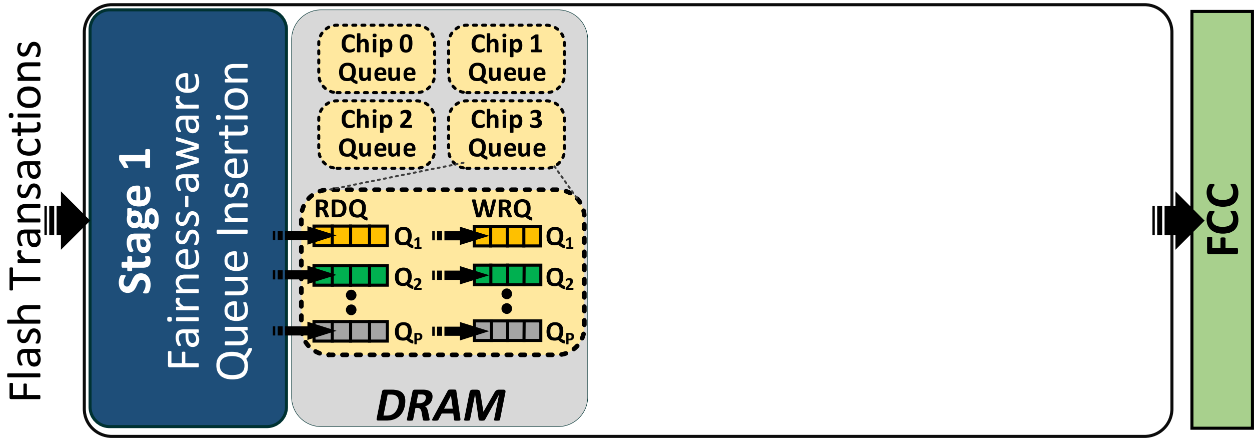
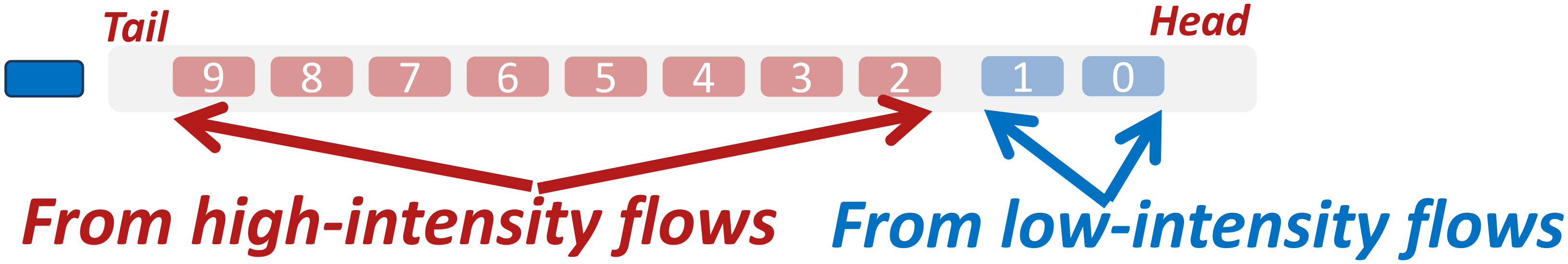


- FLIN is a three-stage I/O request scheduler
  - Replaces existing transaction scheduling unit
  - Takes in flash transactions, reorders them, sends them to flash channel
- Identical throughput to state-of-the-art schedulers
- Fully implemented in the SSD controller firmware
  - No hardware modifications
  - Requires < 0.06% of the DRAM available within the SSD

Three Stages of FLIN



- **Stage 1: Fairness-aware Queue Insertion**
  relieves I/O intensity and access pattern interference



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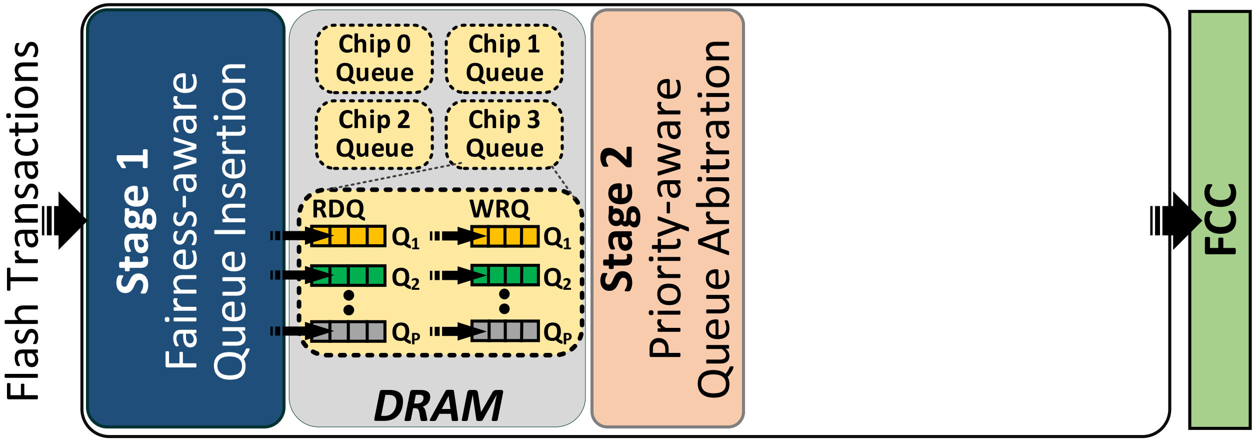

- Stage 1: Fairness-aware Queue Insertion
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- Stage 2: Priority-aware Queue Arbitration
  enforces priority levels that are assigned to each flow by the host

Three Stages of FLIN

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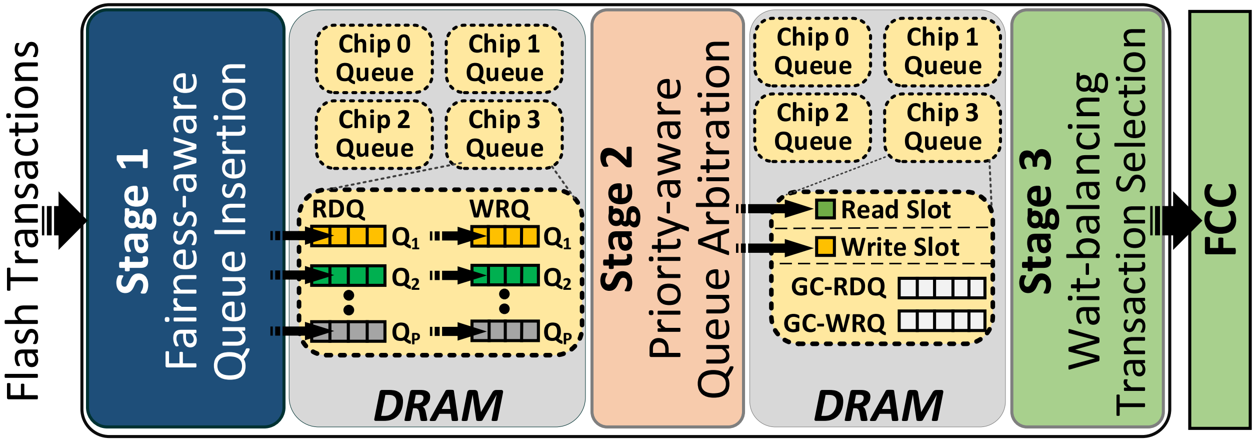

- Stage 1: Fairness-aware Queue Insertion
  relieves I/O intensity and access pattern interference
- Stage 2: Priority-aware Queue Arbitration
  enforces priority levels that are assigned to each flow by the host
- Stage 3: Wait-balancing Transaction Selection
  relieves read/write ratio and garbage collection demand interference

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Evaluation Methodology

- **Detailed SSD Simulator: MQSim** [FAST 2018]
  - Protocol: NVMe 1.2 over PCIe
  - User capacity: 480GB
  - Organization: 8 channels, 2 planes per die, 4096 blocks per plane, 256 pages per block, 8kB page size

Download the Simulator and FAST 2018 Paper at

http://github.com/CMU-SAFARI/MQSim

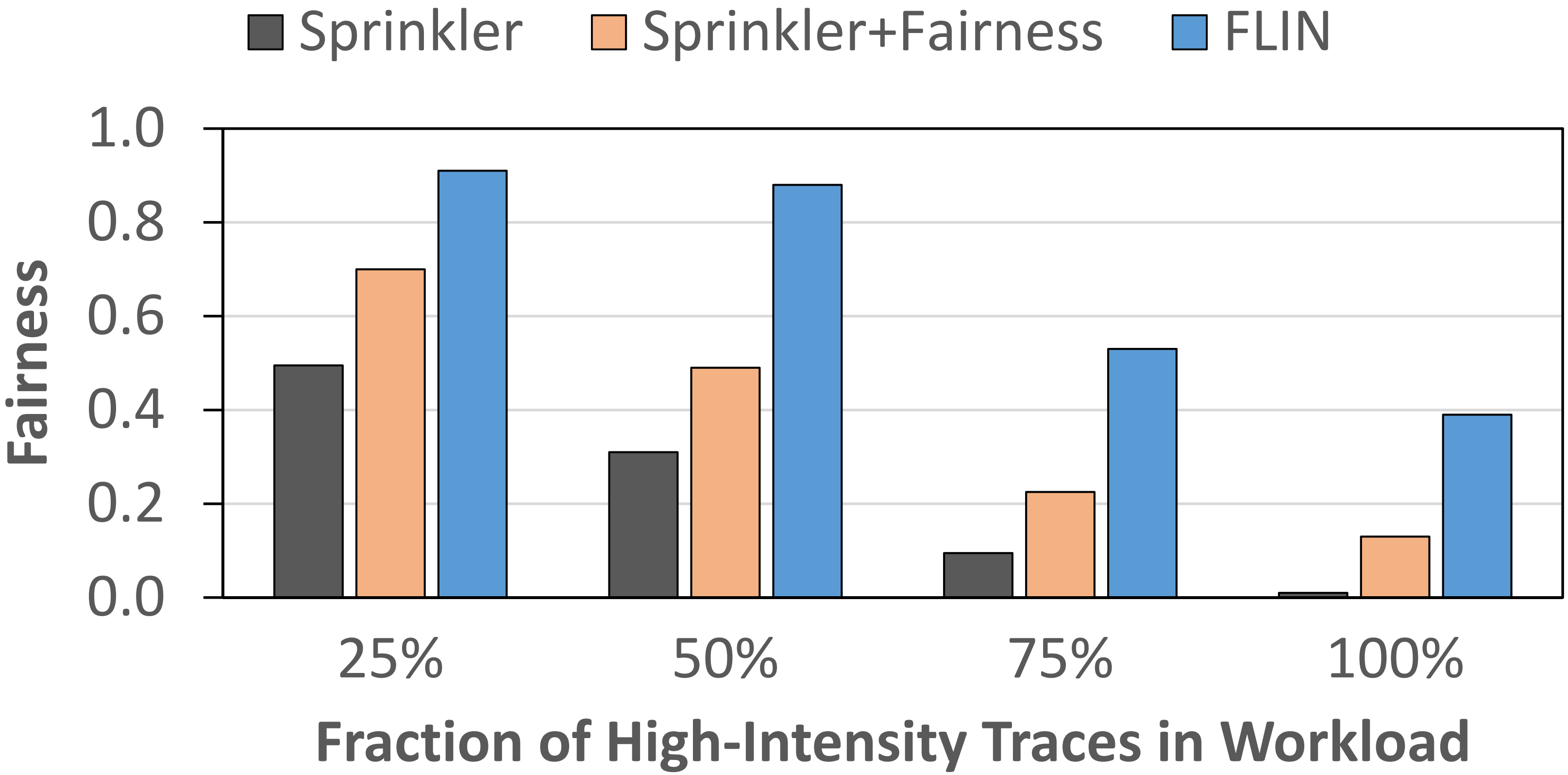
- **40 workloads containing four randomly-selected storage traces**
  - Each storage trace is collected from real enterprise/datacenter applications: UMass, Microsoft production/enterprise
  - Each application classified as low-interference or high-interference

Two Baseline Schedulers

- Sprinkler [Jung+ HPCA 2014]
  a state-of-the-art device-level high-performance scheduler

- Sprinkler+Fairness [Jung+ HPCA 2014, Jun+ NVMSA 2015]
  we add a state-of-the-art fairness mechanism to Sprinkler that was previously proposed for OS-level I/O scheduling
  - **Does not have direct information** about the internal resources and mechanisms of the SSD
  - Does not mitigate **all four sources of interference**

FLIN Improves Fairness Over the Baselines



**FLIN improves fairness by an average of 70%,
by mitigating *all* four major sources of interference**

FLIN Improves Performance Over the Baselines

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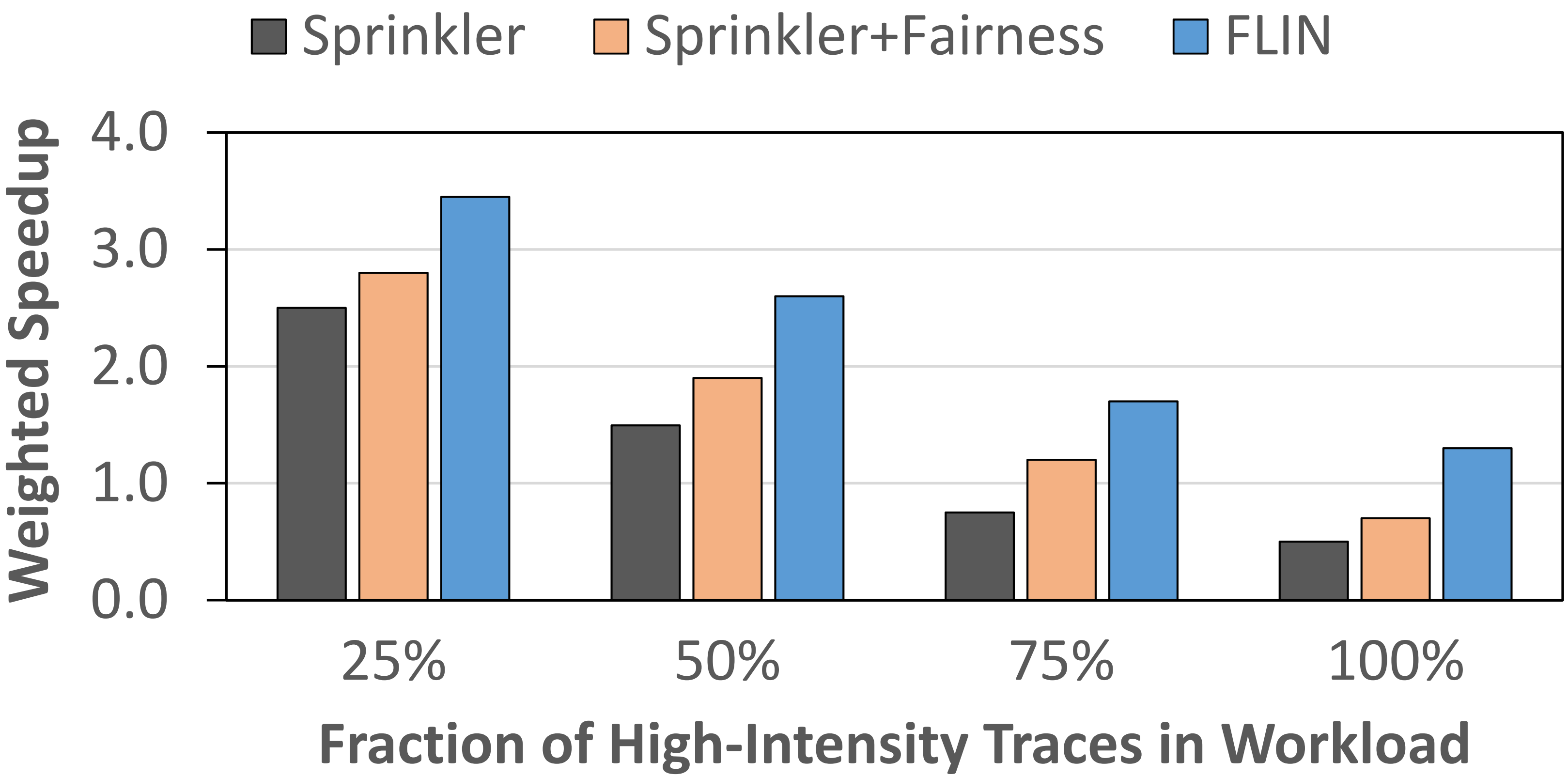

FLIN improves performance by an average of 47%, by making use of idle resources in the SSD and improving the performance of low-interference flows

Other Results in the Paper

- **Fairness and weighted speedup for each workload**
  - FLIN improves fairness and performance for *all* workloads

- **Maximum slowdown**
  - Sprinkler/Sprinkler+Fairness: several applications with maximum slowdown over 500x
  - FLIN: no flow with a maximum slowdown over 80x

- **Effect of each stage of FLIN on fairness and performance**

- **Sensitivity study to FLIN and SSD parameters**

- **Effect of write caching**

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  - Enables **high throughput:** millions of IOPS
  - OS software stack elimination **removes existing fairness mechanisms**
  - **Highly unfair slowdowns** on real state-of-the-art SSDs

- **FLIN:** a new I/O request scheduler for modern SSDs designed to **provide both fairness and high performance**
  - Mitigates all four sources of inter-application interference
    - » Different I/O intensities
    - » Different request access patterns
    - » Different read/write ratios
    - » Different garbage collection demands
  - Implemented fully in the SSD controller firmware, uses < 0.06% of DRAM
  - FLIN improves **fairness by 70%** and **performance** by **47%** compared to a state-of-the-art I/O scheduler (Sprinkler+Fairness)

FLIN:

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Download our ISCA 2018 Paper at

http://ece.cmu.edu/~saugatag/papers/18isca_flin.pdf

References to Papers and Talks

Our FMS Talks and Posters

- FMS 2019
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  - Saugata Ghose, Enabling Fairness and Enhancing Performance in Modern NVMe Solid State Drives
- FMS 2018
  - Yixin Luo, HeatWatch: Exploiting 3D NAND Self-Recovery and Temperature Effects
  - Saugata Ghose, Enabling Realistic Studies of Modern Multi-Queue SSD Devices
- FMS 2017
  - Aya Fukami, Improving Chip-Off Forensic Analysis for NAND Flash
  - Saugata Ghose, Vulnerabilities in MLC NAND Flash Memory Programming
- FMS 2016
  - Onur Mutlu, ThyNVM: Software-Transparent Crash Consistency for Persistent Memory
  - Onur Mutlu, Large-Scale Study of In-the-Field Flash Failures
  - Yixin Luo, Practical Threshold Voltage Distribution Modeling
  - Saugata Ghose, Write-hotness Aware Retention Management
- FMS 2015
  - Onur Mutlu, Read Disturb Errors in MLC NAND Flash Memory
  - Yixin Luo, Data Retention in MLC NAND Flash Memory
- FMS 2014
  - Onur Mutlu, Error Analysis and Management for MLC NAND Flash Memory

Our Flash Memory Works (I)

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  - Yu Cai, Erich F. Haratsch, Onur Mutlu, and Ken Mai, Error Patterns in MLC NAND Flash Memory: Measurement, Characterization, and Analysis, DATE 2012.
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Our Flash Memory Works (II)

- **3D NAND flash memory error analysis**
  - Yixin Luo, Saugata Ghose, Yu Cai, Erich F. Haratsch, and Onur Mutlu, Improving 3D NAND Flash Memory Lifetime by Tolerating Early Retention Loss and Process Variation, SIGMETRICS 2018.
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- **Retention noise study and management**
  - Yu Cai, Gulay Yalcin, Onur Mutlu, Erich F. Haratsch, Adrian Cristal, Osman Unsal, and Ken Mai, Flash Correct-and-Refresh: Retention-Aware Error Management for Increased Flash Memory Lifetime, ICCD 2012.
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Our Flash Memory Works (IV)

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- **Program and erase noise study**
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- Persistent memory
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Referenced Papers and Talks

- **All are available at**
  - https://safari.ethz.ch/publications/
  - https://www.ece.cmu.edu/~safari/talks.html

- **And, many other previous works on**
  - Challenges and opportunities in memory
  - NAND flash memory errors and management
  - Phase change memory as DRAM replacement
  - STT-MRAM as DRAM replacement
  - Taking advantage of persistence in memory
  - Hybrid DRAM + NVM systems
  - NVM design and architecture